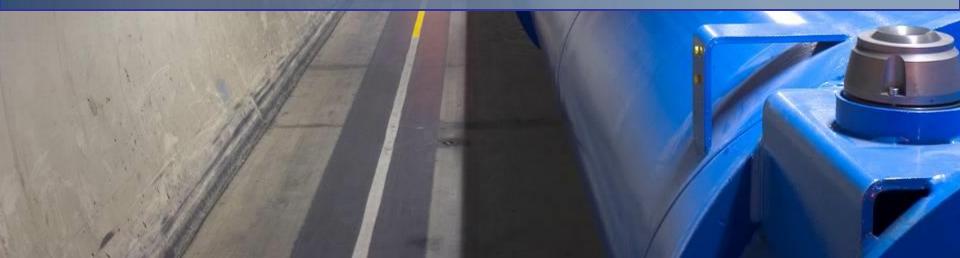




Beam Interlock System Hardware Implementation



A.Dinius AB/PO/IEE - BIS Audit 18th September 2006







- the different modules and their function have been explained
- those modules need mechanical support, power, cabling, etc.....
- objective is to cater for all Beam Interlock applications
- modular setup as from first hardware developments
- work not harder but smarter
- reduced number of types of modules
- fewer spare parts and easier to maintain
- not a revolution but evolution to current design
- in order to improve the EMC the "packaging" has to be part of the development



First designs - 1/3



3U Interface Crate



- integrated Back-Panel with Burndy connectors
- Beam Interface card for current loops
- linked with cable to "Matrix" in VME crate
- Beam-1 and Beam-2 on individual PCBs
- redundant power supplies
- power supply card
- modular set-up (add as necessary



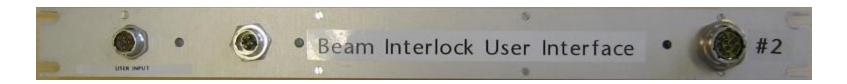




First designs - 2/3



1U User Interface



- compact design
- no lose wiring
- signals to Interface Crate via current loops
- powered from 3U Interface Crate





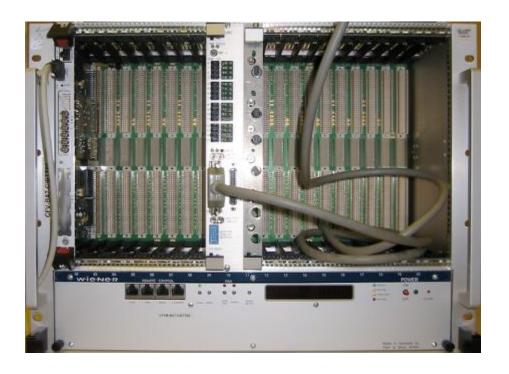
First designs - 3/3



VME crate

- CERN standard Front end Configuration
- "Core" board got signals via 25pin cables
- separate Optical board





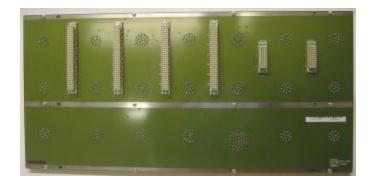


Towards an "All in One" crate



Backpanels





- supports the Burndy connectors for User Interfaces
- Developed 2 types: CIBPL and CIBPS
- different gender and size connectors to avoid patching errors
- sandwich construction
- 8 layer PCB, electrically tested
- avoids cabling errors
- no functional test, visual inspection only
- excellent EMC properties
- Permit-A & Permit-B on individual layers of the PCB
- many ground planes





The "BIS" VME crate - 1/3



8U and 11U models of VME crate



CIBP (LHC Version) Beam Interlock System

V1.0

IN 2 Brann 1

IN 2 Brann 2

UNMASKABLE — BOTH BEAM

UNMASKABLE — BOTH BEAM

IN 3 Brann 2

IN 10 Brann 2

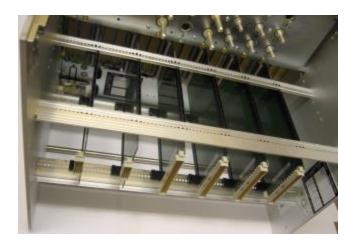
IN 10 Brann 2

IN 10 Brann 2

IN 10 Brann 3

IN

- AB/CO standard Front end Configuration
- introduced 11U model with redundant PSUs
- added card-cage at the back with Extenders
- supports the Backpanel





The "BIS" VME crate - 2/3

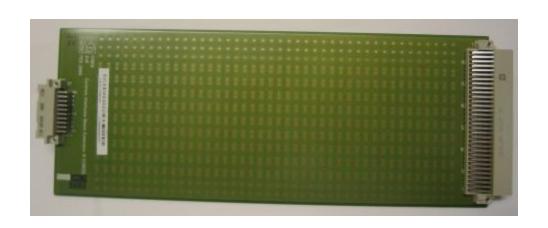


Extenders in the card-cage

- signal paths between VME-P2 and Backpanels
- 3U, 8 layer PCB, electrically tested
- avoids cabling errors
- no functional test, visual inspection only
- excellent EMC properties
- Beam-1 & Beam-2 on individual Extenders
- many ground planes

CIBEA - 3x32pin connector

CIBEB - 3x10pin connector





The "BIS" VME crate - 3/3



Modules in the VME crate



- AB/CO-standard Front-End CPU with Timing RX
- 1 or 2 sets of **CIBM** with **CIBT**
- signal paths via VME-P2
- some modules are "slot-dependant"
- non traditional front panel arrangement
- CIBM has Optical Interface (**CIBO**)
- some crates have CIBG
- possible to "host" boards (e.g. SLP)
- Modular set-up (add as necessary)

CIBT, CIBM, CIBG and CIBO

- manufacturer does functional test
- manufacturer loads FPGA program
- manufacturer does power soak test
- same PCB for CIBM and CIBG



The BIS User Interface

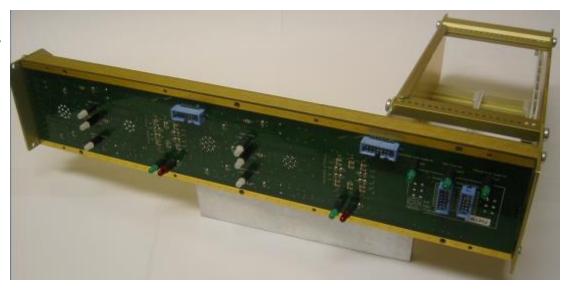


2U Single and Double Beam model

- same PCB for **CIBUS** and **CIBUD**
- sandwich construction
- avoids cabling errors
- manufacturer does functional test
- manufacturer loads FPGA program
- manufacturer does power soak test
- excellent EMC properties
- equipped with redundant PSUs









The User Interface PSUs



Power Supply Units

- 2U models not OEM
- for redundancy 2 **CIBD** / User Interface
- manufacturer does functional test
- manufacturer does power soak test
- excellent EMC properties







- inter-group collaboration proved very profitable
- speedy prototyping enabled quick development cycle
- logical evolution from first trials to current design
- set-up manufacturing contract with industry
- positive feedback from manufacturer
- excellent results from pre-series manufacturing to date (*)
- many modules ready for series manufacturing (*)
- installed equipment performs well
 - (*) CIBUS, CIBUD, CIBD, CIBPL, CIBPS, CIBEA, CIBEB









FIN