BIS software layers at CERN

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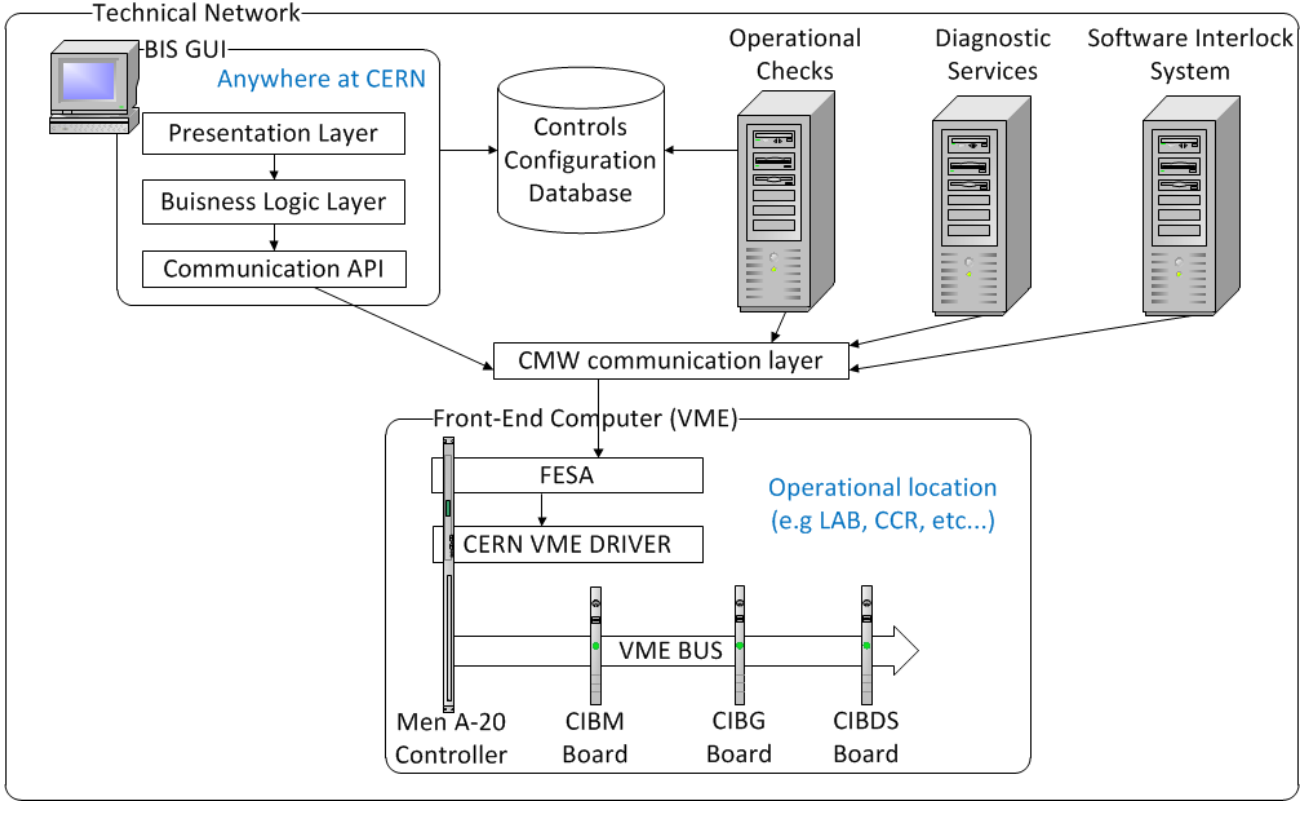
- BIS software vertical slice overview
- Diagnostic and safety services
- Software quality
- Adaptable architecture

Architecture overview



BIS software vertical slice overview

Diagnostic and safety services

Software quality

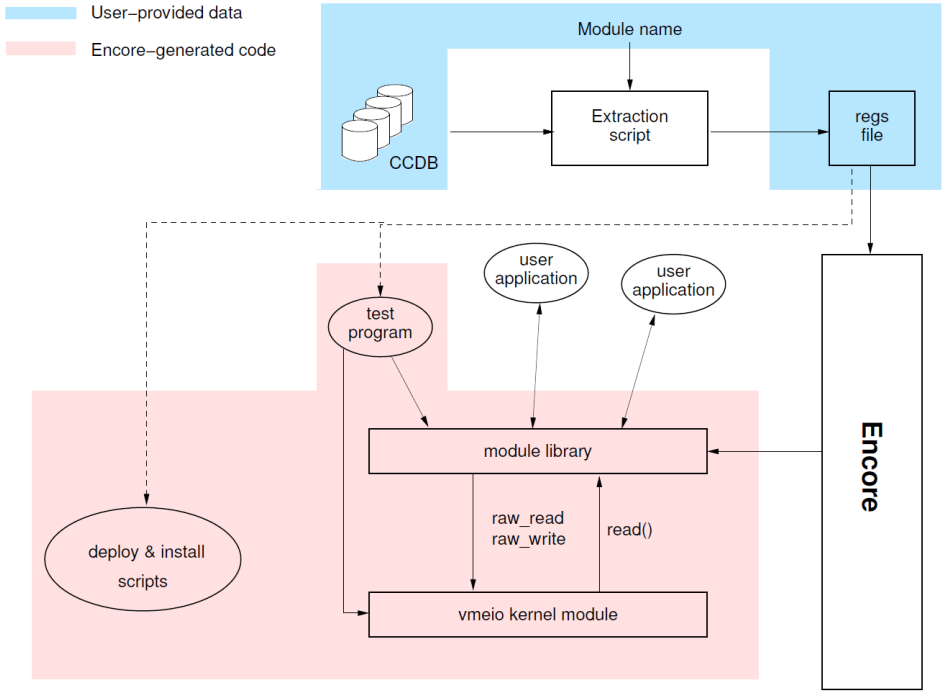
Adaptable architecture

BIS Hardware

- VME crate containing a (Linux based) controller and multiple VME boards.
- Communication is based on the VME bus.
- Controller can talk to the outside world through Ethernet (machine/technical network).
- More details in Stephane presentation.

CERN VME Driver

- Runs on the Linux controller of the VME crate.
- Interface between VME boards and FESA classes.
- Access to hardware devices occurs through two mechanisms:
  - I/O operations over registers
  - Interrupts
- Driver generated from hardware types information stored in the Controls Configuration DB (CCDB).

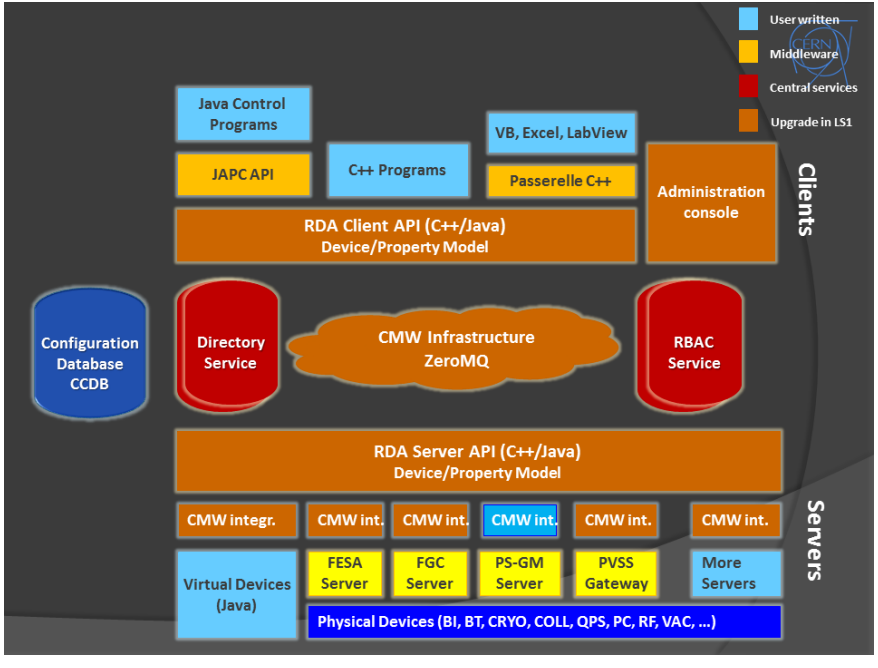


FESA

- FESA = Front End Software Architecture, framework developed at CERN to standardize device access throughout accelerator equipment.
- C++ program running on the Linux controller of the VME crate.
- Interface between the board drivers and the ‘high-level’ software layers.
- Defines a contract (Device Property model) that exposes fields to be acquired or controlled.
- Allows read/write and subscribe operations. Real-time processing of the boards data is synchronized using the accelerators timing system or FESA internal timer.
- For the BIS, no specific logic, only expose the registers with un-decoded raw data.

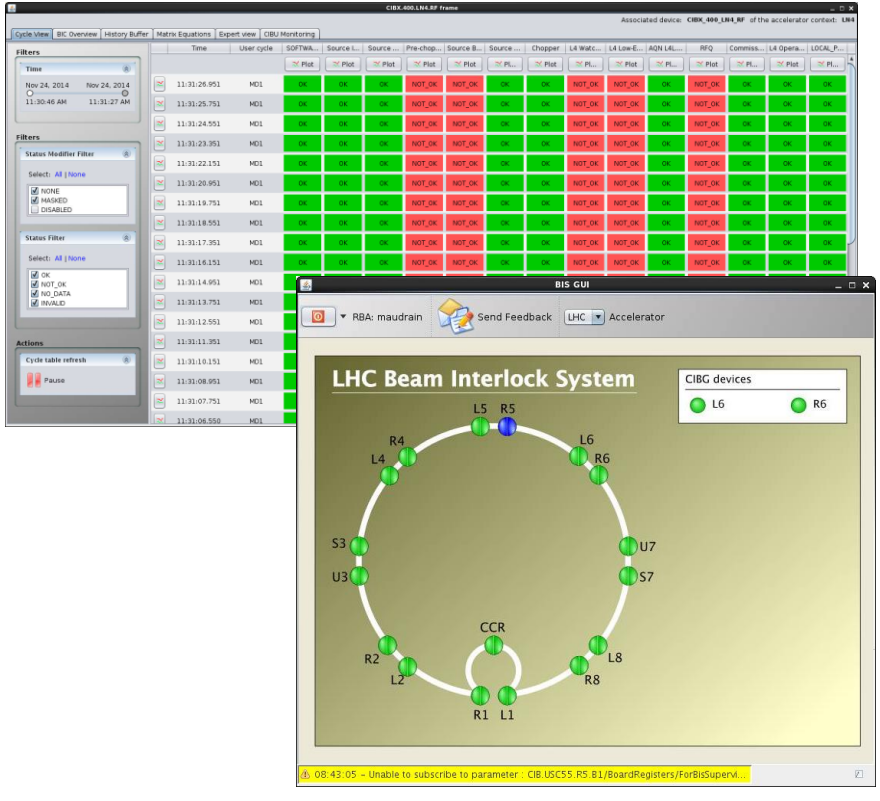
CMW

- Controls MiddleWare (CMW) is the communication infrastructure at CERN based on CORBA/ZeroMQ. Bridge between Java and C++ worlds.

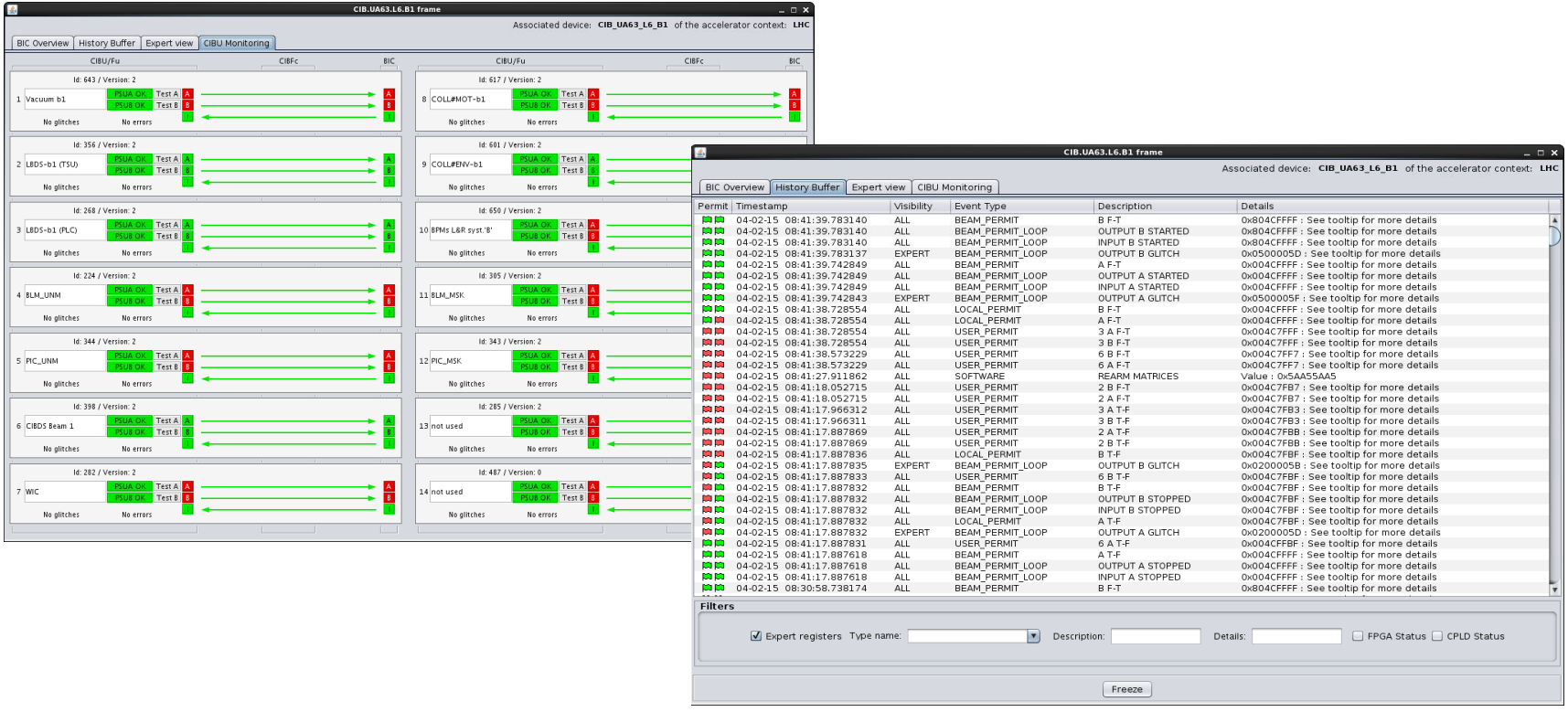


BIS GUI (1/2)

- Main application for monitoring and control of all BICs at CERN.
- Operator/experts panels and commands.
- Timing synchronous monitoring for the cyclic machines (SPS, Booster, Linac4).



BIS GUI (2/2)


CIB.UA63.L6.B1 frame
Associated device: CIB_UA63_L6_B1 of the accelerator context: LHC
BIC Overview
History Buffer
Expert view
CIBU Monitoring
CIBU/Fu
CIBFc
BIC
Id: 643 / Version: 2
1 Vacuum b1
Id: 617 / Version: 2
8 COLL#MOT-b1
Id: 356 / Version: 2
2 LBDS-b1 (TSU)
Id: 601 / Version: 2
9 COLL#ENV-b1
Id: 268 / Version: 2
3 LBDS-b1 (PLC)
Id: 650 / Version: 2
10 BPMs L&R syst.'B'
Id: 224 / Version: 2
4 BLM_UNM
Id: 305 / Version: 2
11 BLM_MSK
Id: 344 / Version: 2
5 PIC_UNM
Id: 343 / Version: 2
12 PIC_MSK
Id: 398 / Version: 2
6 CIBDS Beam 1
Id: 285 / Version: 2
13 not used
Id: 282 / Version: 2
7 WIC
Id: 487 / Version: 0
14 not used
PSUA OK
PSUB OK
Test A
Test B
No glitches
No errors
CIB.UA63.L6.B1 frame
Associated device: CIB_UA63_L6_B1 of the accelerator context: LHC
BIC Overview
History Buffer
Expert view
CIBU Monitoring
Permit
Timestamp
Visibility
Event Type
Description
Details
04-02-15 08:41:39.783140 ALL BEAM_PERMIT B F-T 0x804CFFFF : See tooltip for more details
04-02-15 08:41:39.783140 ALL BEAM_PERMIT_LOOP OUTPUT B STARTED 0x804CFFFF : See tooltip for more details
04-02-15 08:41:39.783140 ALL BEAM_PERMIT_LOOP INPUT B STARTED 0x804CFFFF : See tooltip for more details
04-02-15 08:41:39.783137 EXPERT BEAM_PERMIT_LOOP OUTPUT B GLITCH 0x0500005D : See tooltip for more details
04-02-15 08:41:39.742849 ALL BEAM_PERMIT A F-T 0x004CFFFF : See tooltip for more details
04-02-15 08:41:39.742849 ALL BEAM_PERMIT_LOOP OUTPUT A STARTED 0x004CFFFF : See tooltip for more details
04-02-15 08:41:39.742849 ALL BEAM_PERMIT_LOOP INPUT A STARTED 0x004CFFFF : See tooltip for more details
04-02-15 08:41:39.742843 EXPERT BEAM_PERMIT_LOOP OUTPUT A GLITCH 0x0500005F : See tooltip for more details
04-02-15 08:41:38.728554 ALL LOCAL_PERMIT B F-T 0x004CFFFF : See tooltip for more details
04-02-15 08:41:38.728554 ALL LOCAL_PERMIT A F-T 0x004CFFFF : See tooltip for more details
04-02-15 08:41:38.728554 ALL USER_PERMIT 3 A F-T 0x004C7FFF : See tooltip for more details
04-02-15 08:41:38.728554 ALL USER_PERMIT 3 B F-T 0x004C7FFF : See tooltip for more details
04-02-15 08:41:38.573229 ALL USER_PERMIT 6 B F-T 0x004C7FF7 : See tooltip for more details
04-02-15 08:41:38.573229 ALL USER_PERMIT 6 A F-T 0x004C7FF7 : See tooltip for more details
04-02-15 08:41:27.911862 ALL SOFTWARE REARM MATRICES Value : 0x5AA55AA5
04-02-15 08:41:18.052715 ALL USER_PERMIT 2 B F-T 0x004C7FB7 : See tooltip for more details
04-02-15 08:41:18.052715 ALL USER_PERMIT 2 A F-T 0x004C7FB7 : See tooltip for more details
04-02-15 08:41:17.966312 ALL USER_PERMIT 3 A T-F 0x004C7FB3 : See tooltip for more details
04-02-15 08:41:17.966311 ALL USER_PERMIT 3 B T-F 0x004C7FB3 : See tooltip for more details
04-02-15 08:41:17.887869 ALL USER_PERMIT 2 A T-F 0x004C7FBB : See tooltip for more details
04-02-15 08:41:17.887869 ALL USER_PERMIT 2 B T-F 0x004C7FBB : See tooltip for more details
04-02-15 08:41:17.887836 ALL LOCAL_PERMIT B T-F 0x004C7FBF : See tooltip for more details
04-02-15 08:41:17.887835 EXPERT BEAM_PERMIT_LOOP OUTPUT B GLITCH 0x0200005B : See tooltip for more details
04-02-15 08:41:17.887833 ALL USER_PERMIT 6 B T-F 0x004C7FBF : See tooltip for more details
04-02-15 08:41:17.887832 ALL BEAM_PERMIT B T-F 0x004C7FBF : See tooltip for more details
04-02-15 08:41:17.887832 ALL BEAM_PERMIT_LOOP OUTPUT B STOPPED 0x004C7FBF : See tooltip for more details
04-02-15 08:41:17.887832 ALL BEAM_PERMIT_LOOP INPUT B STOPPED 0x004C7FBF : See tooltip for more details
04-02-15 08:41:17.887832 ALL LOCAL_PERMIT A T-F 0x004C7FBF : See tooltip for more details
04-02-15 08:41:17.887832 EXPERT BEAM_PERMIT_LOOP OUTPUT A GLITCH 0x0200005D : See tooltip for more details
04-02-15 08:41:17.887831 ALL USER_PERMIT 6 A T-F 0x004CFFBF : See tooltip for more details
04-02-15 08:41:17.887618 ALL BEAM_PERMIT A T-F 0x004CFFFF : See tooltip for more details
04-02-15 08:41:17.887618 ALL BEAM_PERMIT_LOOP OUTPUT A STOPPED 0x004CFFFF : See tooltip for more details
04-02-15 08:41:17.887618 ALL BEAM_PERMIT_LOOP INPUT A STOPPED 0x004CFFFF : See tooltip for more details
04-02-15 08:30:58.738174 ALL BEAM_PERMIT B F-T 0x804CFFFF : See tooltip for more details
Filters
Expert registers
Type name:
Description:
Details:
FPGA Status
CPLD Status
Freeze

BIS software vertical slice overview

Diagnostic and safety services

Software quality

Adaptable architecture

Controls configuration database

- Stores static BIS reference configuration (BIS input names, connection type to user, etc…).
- Used mainly by the pre-operational checks to verify consistency with the hardware.

Select	* Device Name	* Channel Nb	* Used	* Short Name	Hardware Connection Type	Long Name	Rack	Cibu Id	Additional Info	Mech. Contacts
	CIB.UA67.R6.B2	1	YES	Vacuum b2	7 - Connected to a CIBUD	Vacuum valves beam-2	VY13=UA67	ID000632		NO
	CIB.UA67.R6.B2	2	YES	LBDS-b2 (TSU)	6 - Connected to a CIBUS	TSU part of the Dumping System for Beam-2	MYDGP08=UA6	ID000357		NO
	CIB.UA67.R6.B2	3	YES	LBDS-b2 (PLC)	6 - Connected to a CIBUS	PLC part of the Dumping System for Beam-2	MYDGP08=UA6	ID000292	original CIBU (ID#266)	NO
	CIB.UA67.R6.B2	4	NO	not used						NO
	CIB.UA67.R6.B2	5	YES	PIC_UNM	6 - Connected to a CIBUS	Essential Circuits at right side	CYCIP02=UA67	ID000277		NO
	CIB.UA67.R6.B2	6	YES	CIBDS Beam 2	6 - Connected to a CIBUS	CIBDS Beam 2	CYCIB01=UA67	ID000399		NO
	CIB.UA67.R6.B2	7	NO	not used						NO
	CIB.UA67.R6.B2	8	YES	BPMs L&R syst.'A'	7 - Connected to a CIBUD	Normal system ('A') BPMs L & R for Beam-2	BY07=SR6	ID000625		NO
	CIB.UA67.R6.B2	9	YES	FMCM_RMSD-b2	7 - Connected to a CIBUD	Fast Magnet Current change Monitor (CIF.UA67.RMSDB2)	CIBU in BIC cra	ID000646		NO
	CIB.UA67.R6.B2	10	YES	BTV-b2	7 - Connected to a CIBUD	Screens Beam-2	BY01=US65	ID000611		NO
	CIB.UA67.R6.B2	11	NO	not used						NO
	CIB.UA67.R6.B2	12	YES	PIC_MSK	6 - Connected to a CIBUS	Auxiliary Circuits at right side	CYCIP02=UA67	ID000279		NO
	CIB.UA67.R6.B2	13	NO	not used		Unused b2-channel of the position interlocking of			Warning: TCDQ-b2 system is	NO
	CIB.UA67.R6.B2	14	NO	not used		Unused b2-channel of the BETS of the TCDQ (beam-1)				NO

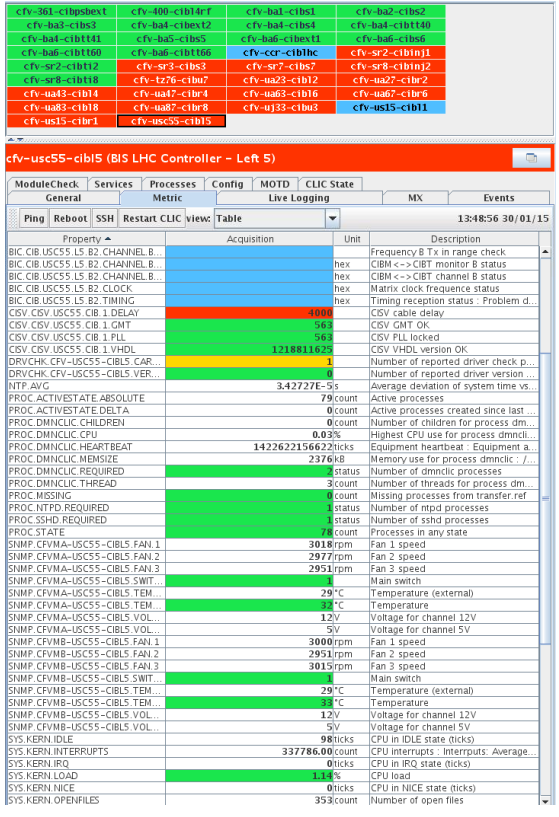
Diagnostic services

- Record of all BIS boards history buffers in the Logging DB to be accessible later on to replay operational states and analyse certain events. Acquisition every second.
- Record BIS history buffer and other information on configurable events in the Post-Mortem System: e.g. beam dump, etc. Used then in the post-operational checks.

Operational checks

- Pre-operational :
  - using the LHC sequencer to run a Java program to verify certain configuration or current states of the BIS before operation.
  - Operation/next cycle can be inhibited.
- Post-operational:
  - with Post Mortem to analyse the BIS buffers around a beam dump and determine potential problems related to the system.
  - Operation/next cycle can be inhibited.

Continuous Monitoring



- DiaMon framework to monitor the FEC state.
- During-operation: using the DiaMon framework, to assert certain values of the BIS boards register and trigger different severity messages.

Software Interlock System

- Can interlock each BIC in the LHC through a dedicated software input.
- Can inhibit operation if additional interlocking constraints are not met (typically for more complex/less critical/redundant verifications like power-converters statuses, LHC access, etc…).
- Timeout to inhibit operation if the SIS connection to the BIS is lost.

BIS software vertical slice overview

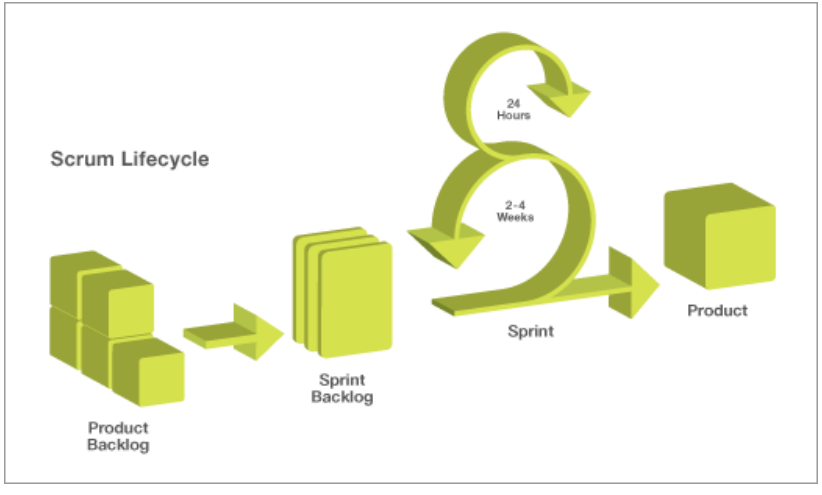
Diagnostic and safety services

Software quality

Adaptable architecture

Scrum

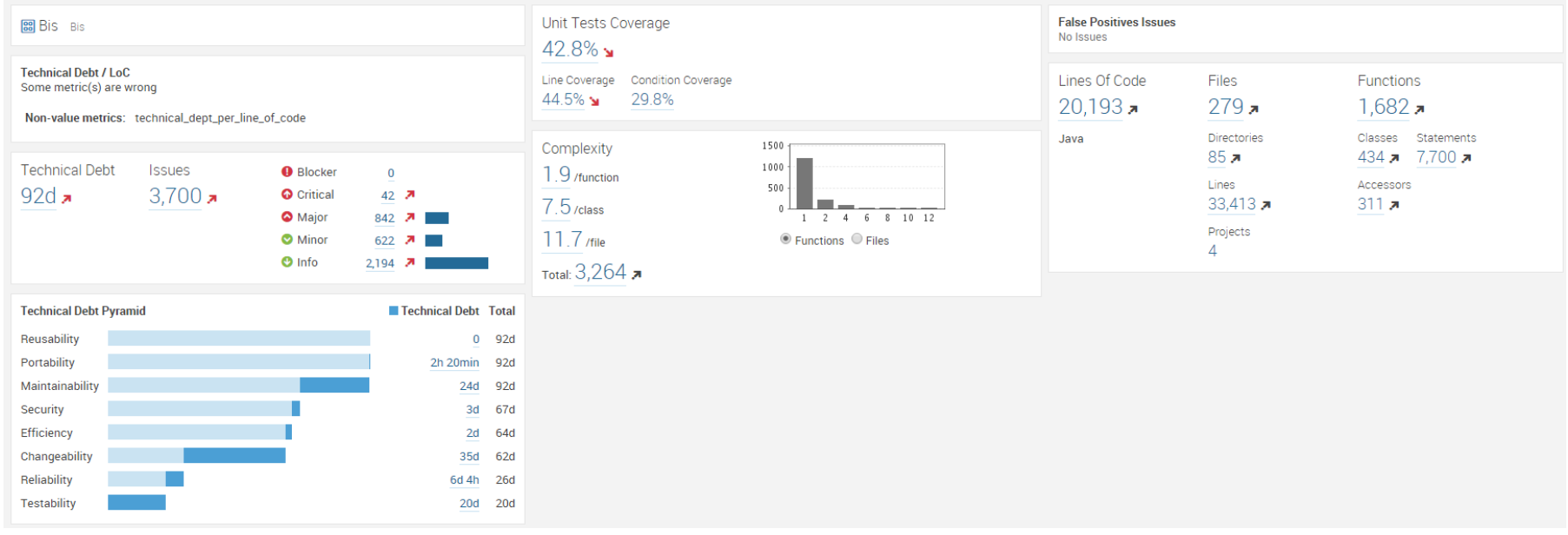
- **Individuals and interactions** over Processes and tools
- **Working software** over Comprehensive documentation
- **Customer collaboration** over Contract negotiation
- **Responding to change** over Following a plan



Quality tools (1/2)

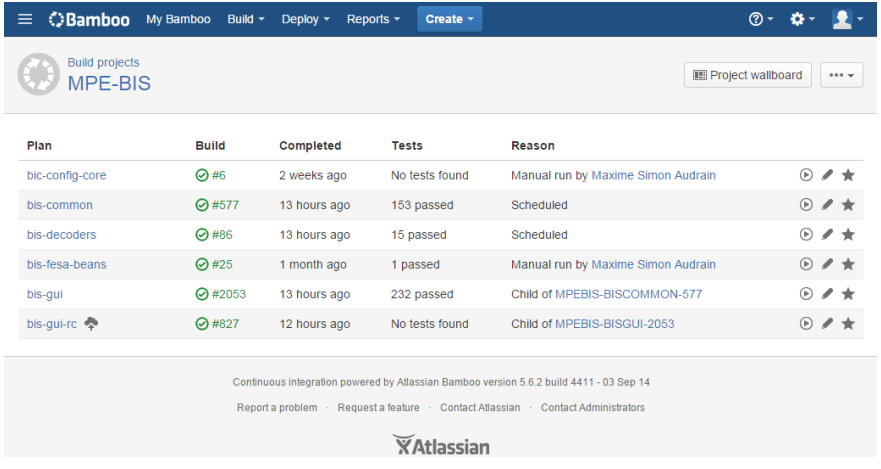
- Sonarqube for quality metrics,
  - Distribution of quality profiles to developer machines
- Eclipse workstation configuration with Eclipse SDC:
  - Static code checkers configuration,
  - Code coverage plug-ins,
  - Code generation plug-ins.

Quality tools (2/2)



Continuous delivery

- Using Bamboo and Gradle to ensure all-time delivery capability.
- Product tested and released each time new code is added.
- Release candidate build runs the acceptance tests to ensure the product is deployable.
- Deployment plan -> “Click to deploy”



BIS software vertical slice overview

Diagnostic and safety services

Software quality

Adaptable architecture

Adaptable architecture (1/4)

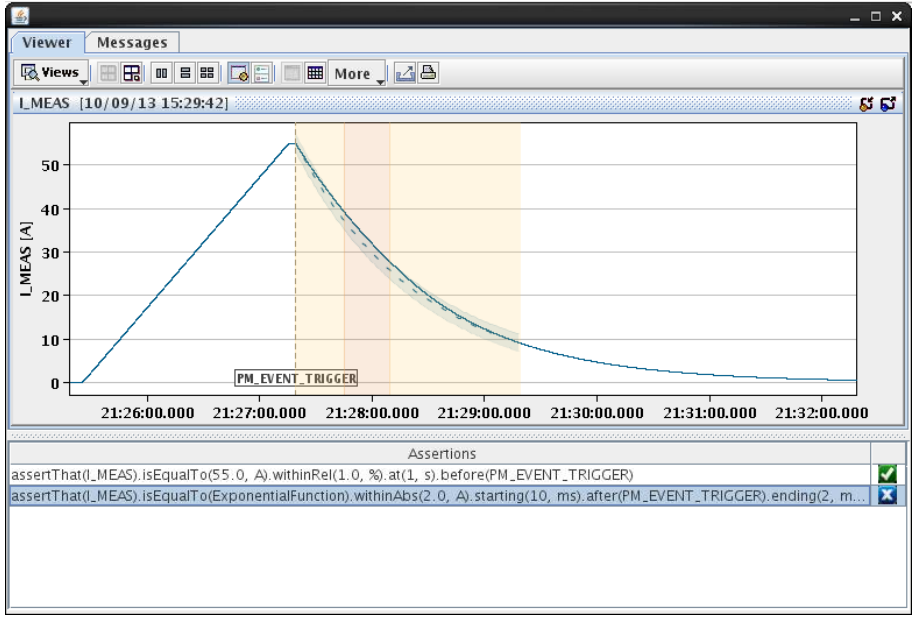
- VME driver
  - CERN version -> EPICS version
- FESA
  - EPICS module or Real-Time Java or other C++ implementation
  - Genericity from board type.
- CMW -> EPICS MiddleWare

Adaptable architecture (2/4)

- BIS GUI will need some adaptation to select a communication API according to the context: ESS, CERN
- Role Based Access -> EPICS Security module?
- CCDB
  - any data source: DB, CSV, etc..
- Logging Service
  - Any continuous acquisition service backed by a “write once read many” storage: e.g. Cassandra, etc…

Adaptable architecture (3/4)

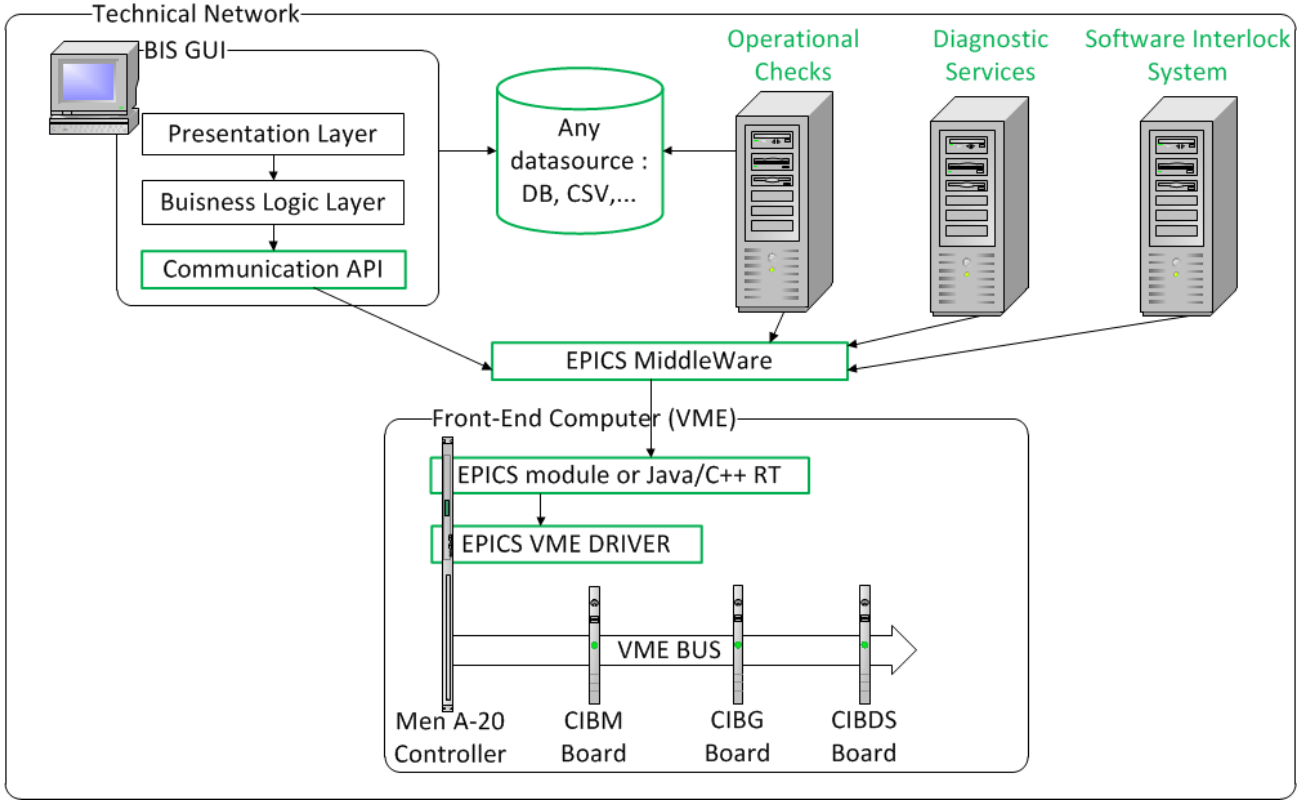
- Pre-Op
  - Use EPICS sequencer?
  - Need communication adaptation (EPICS MW)
  - Re-use or complement logic
- Post-op
  - Could use PM data collection (PM tightly coupled to CMW)
  - Analysis framework required -> eDSL



Adaptable architecture (4/4)

- Continuous monitoring
  - DiaMon can be replaced by any free and open source solution: Nagios, Icinga, Shinken.
- Software Interlock System
  - CERN core with ESS specific modules?
  - Can be re-implemented.

New architecture overview



Outlook

- Complete CERN infrastructure for BIS supervision and diagnostic
- Partly reusable and/or adaptable
- Interested for collaboration!

Thank you for your attention

- Do you have any questions?