500 MSPS status

Outline

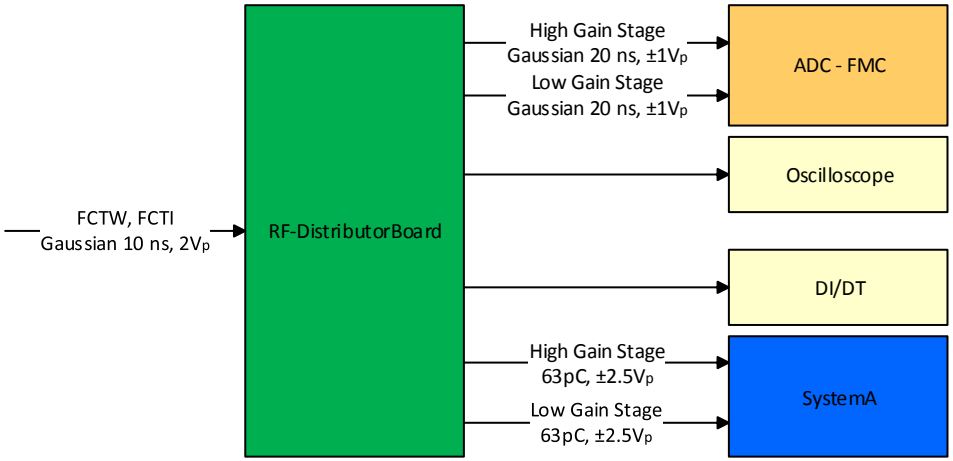
- Roadmap up to now
- RF-distributor
- ADC board
- VFC-HPC integration
  - The JESD204 Rx block
  - Results
- Commercial options
- Summary

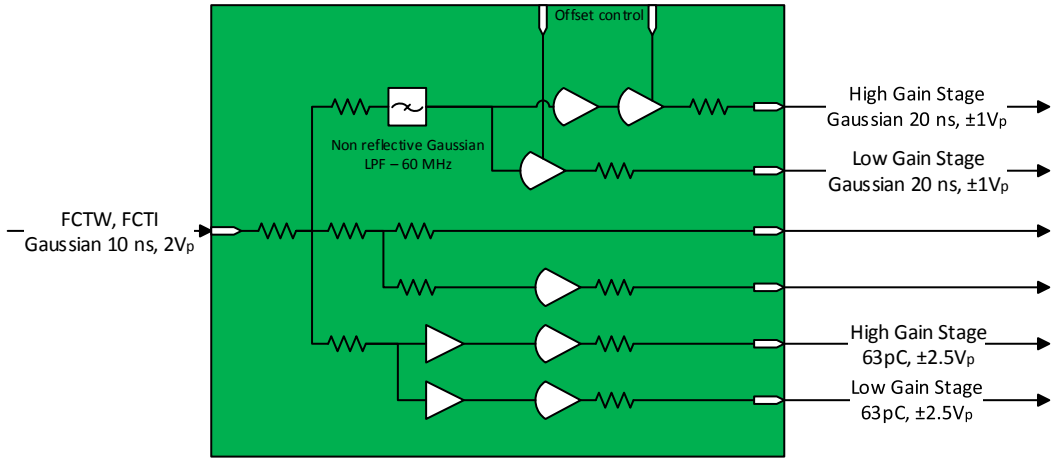
Roadmap up to now

- From simulations:
  - ~17 ns Gaussian pulse
  - 500 MSPS, ENOB ~ 10.5, DC coupled
  - To get an accuracy < 1% for
- Market survey => FMC-500 from Innovative, but the board never existed…
- Decide to move to a development board from AD with the AD9680 ADC => AD9680-EVM:
  - 300 MSPS – 1 GSPS
  - ~10.8 ENOB (@ 10 MHz)
  - AC coupled
  - Serial JESD204 data transmission
  - Received by mid November
- Signal conditioning needed to tune the signal timing and work with safe voltage ranges for the sampling system => Rf-Distributor board

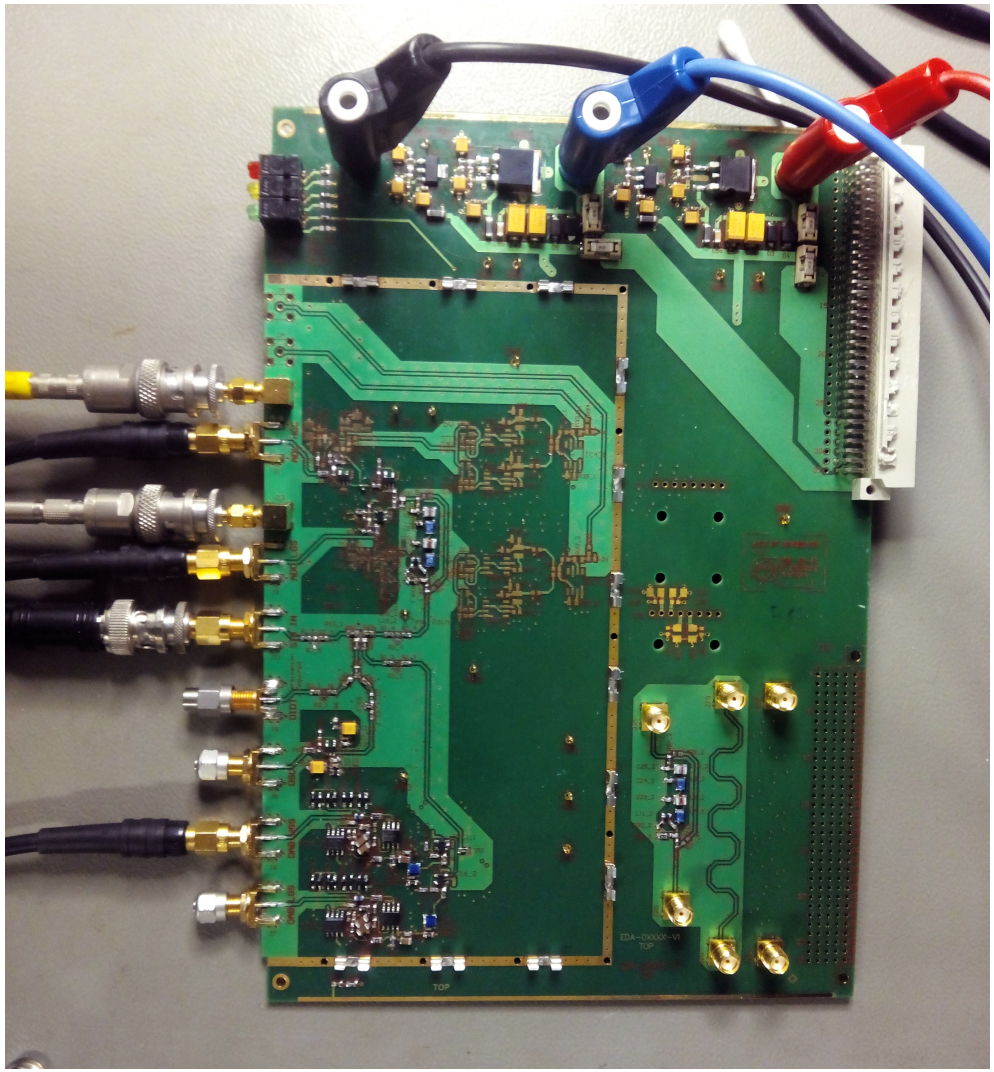
RF-Distributor

- ADC-FMC outputs:
  - Non reflective Gaussian filter with 55 MHz BW
  - Output voltages tuned to work safely with the Innovative FMC-500 analog input stage (± 1Vp)
  - Offset control available
- System A output similar to the old one, but with some modifications:
  - Changed clamping diodes
  - Input buffer changed



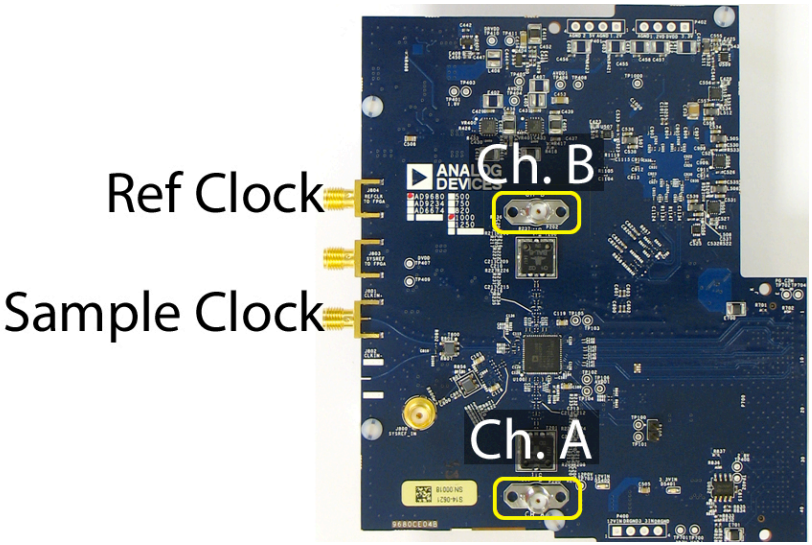


Rf-Distributor

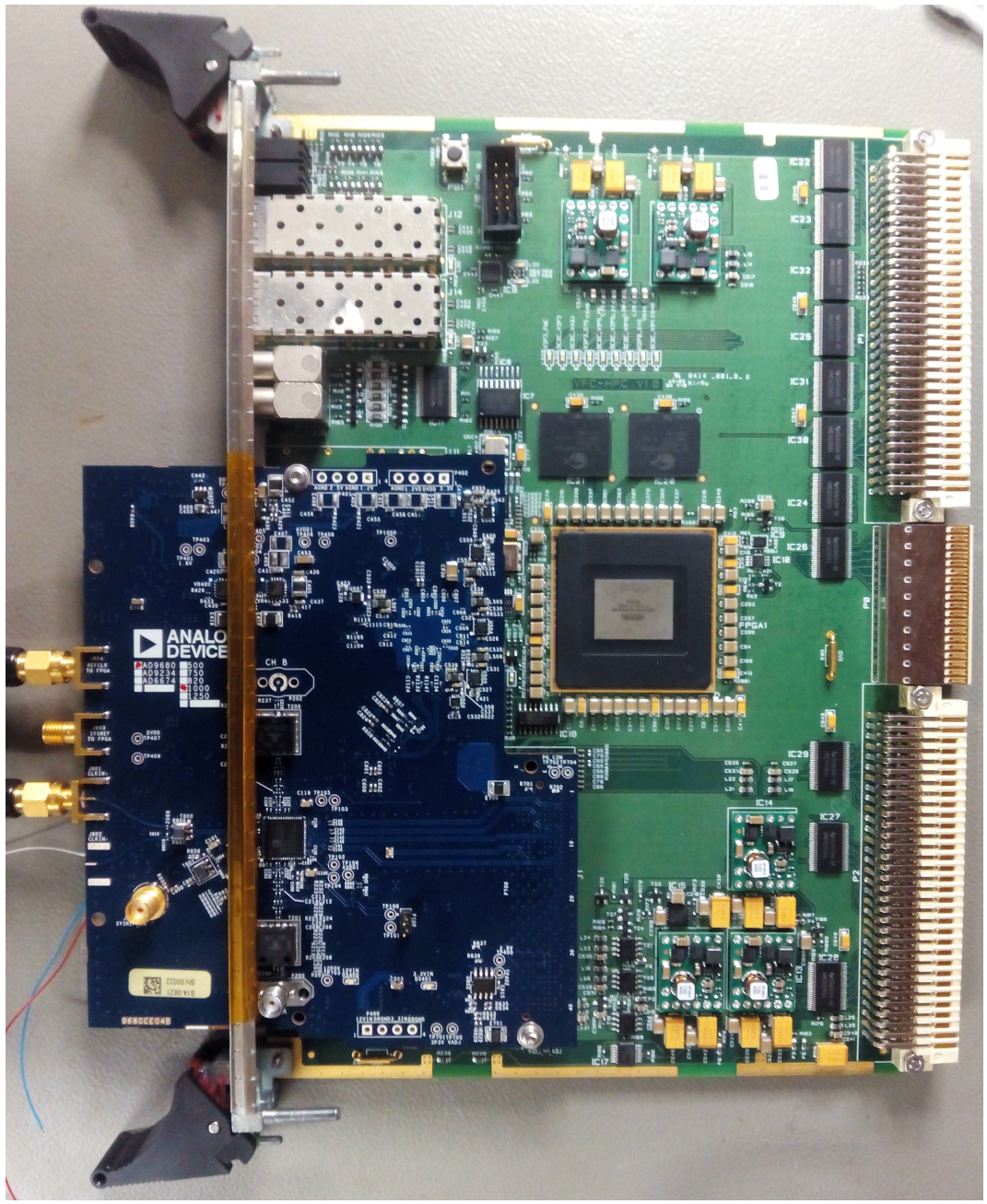


- V1 built and tested:
  - Scattering parameters
  - Pulse shape in time domain
  - Linearity
  - Noise
  - External offset control
- Some minor errors found
- Fixes done and V2 being assembled

ADC-Board



- Needs two external source synchronous low jitter clocks:
  - Sample Clock = 500 MHz (to AD9680)
  - Ref Clock = 125 MHz (to FPGA)
- Serial data output in 4 lanes (JESD204 protocol)



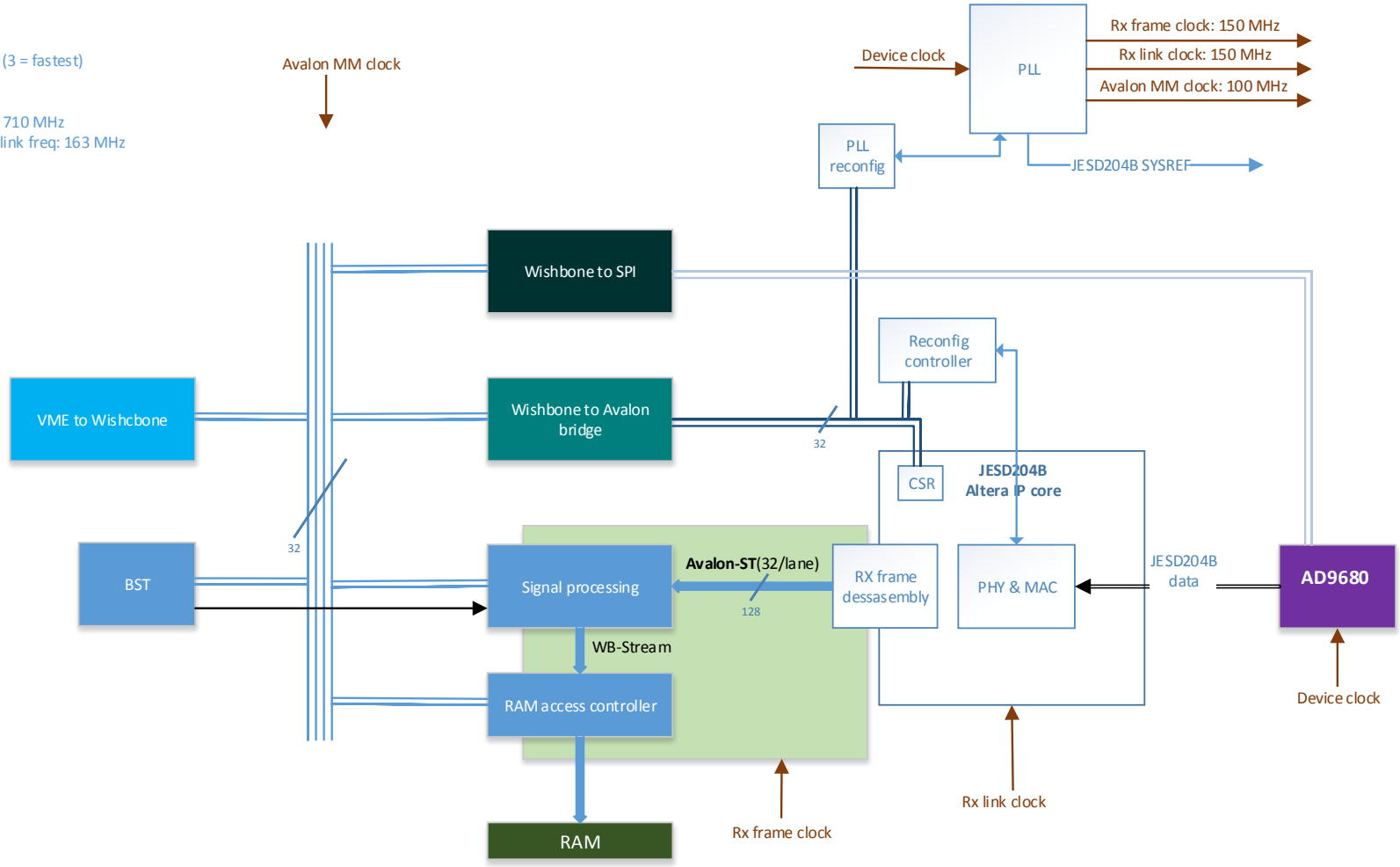
Overview of the system

Arria V GX (5AGXMB1G4F40C4N)

- 5A: Arria V
- GX: 6 Gbps transceiver
- M: 1 hard PCIe and 2 hard memory controllers
- B1: 300K logic elements
- G: 18 transceivers
- 4: Transceiver speed grade 6.5536 Gbps
- F: FBGA package
- 40: 1517 pins
- C: Commercial
- 4: Speed grade 4 (3 = fastest)
- N: Lead-free

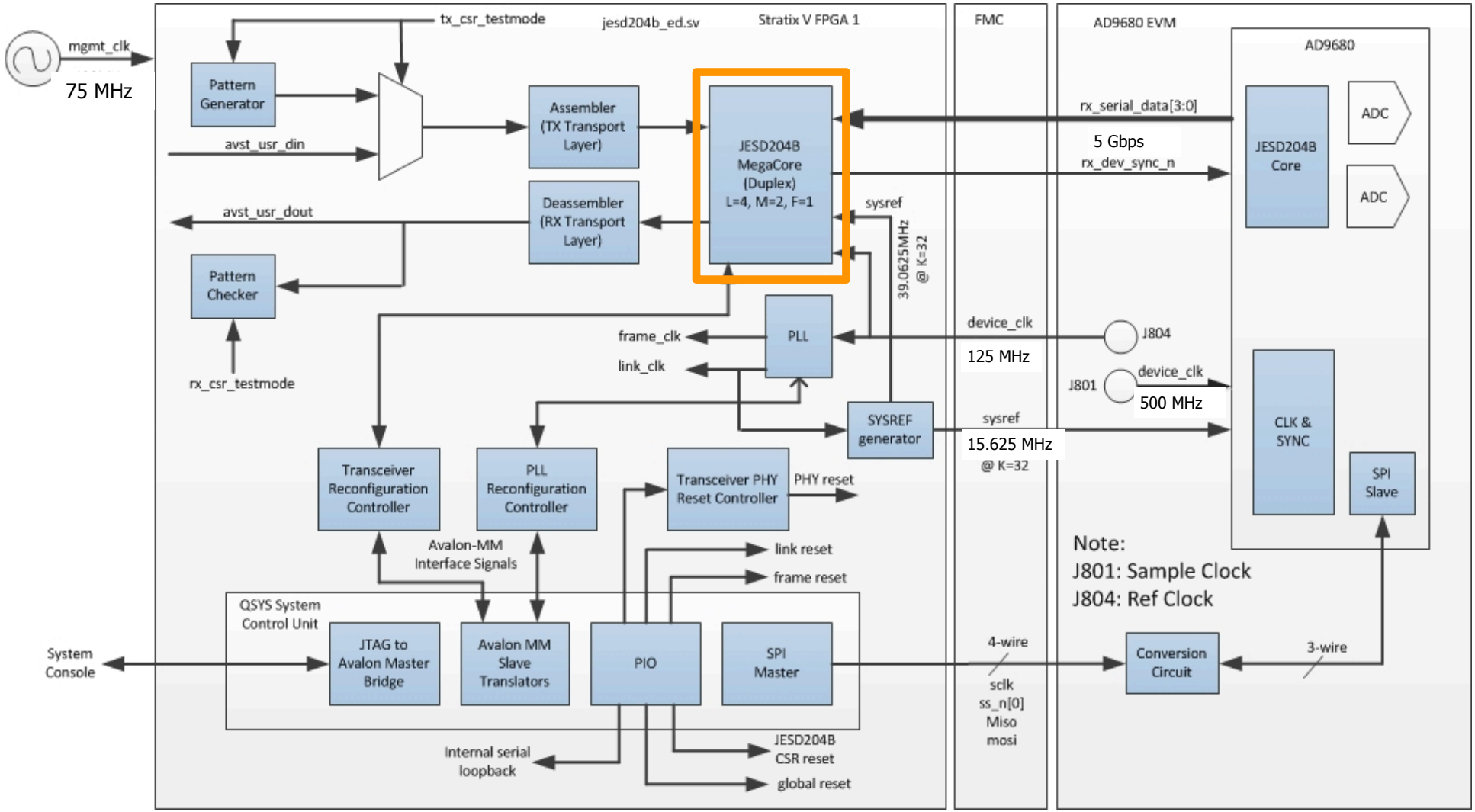
- PLL input Fmax = 710 MHz
- Transceiver max link freq: 163 MHz

- 1510xM10Kbit



VFC-HPC integration – JESD204

- Adapt project from Altera for the AD9680 ADC using a Stratix V: change clock frequencies, rebuild all the IP cores for the Arria V, modify pinout and add some pieces of code



VFC-HPC integration – JESD204

- I got quite jammed because I was using a schematic with a wrong pinout…
- And in fact, the wrong-old pinout was better to accommodate the GX transceivers
- With the new one the Duplex core doesn't fit => had to modify the code => no internal loopback to test the deserialization disentangling machinery
- In addition one fuse was blown…

Wrong pinout

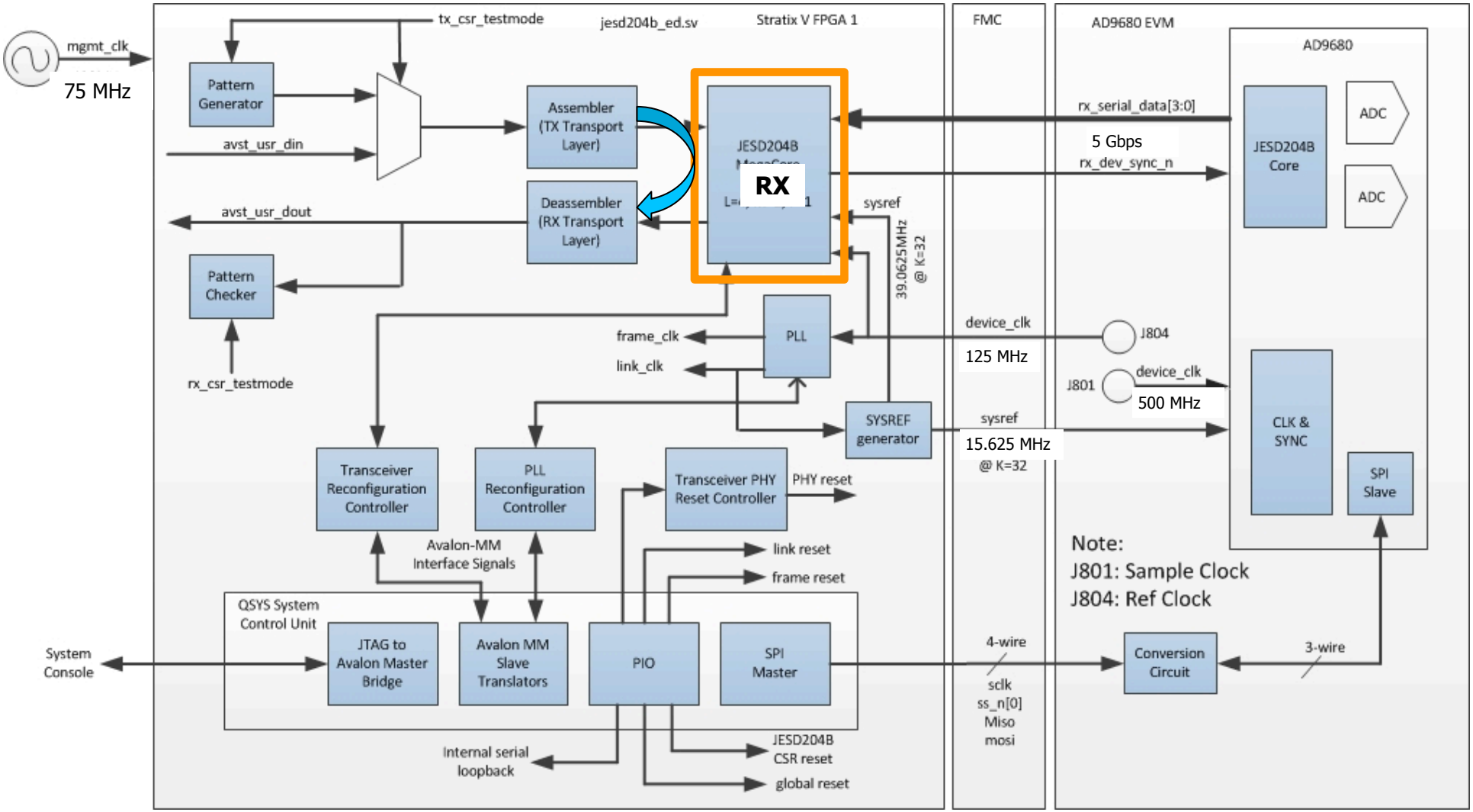
	AD39	GXB_RX_L7P,GXB_REFCLK_L7P
	AD38	GXB_RX_L7N,GXB_REFCLK_L7N
FMC_DpM2C_P9	AB39	GXB_RX_L8P,GXB_REFCLK_L8P
FMC_DpM2C_N9	AB38	GXB_RX_L8N,GXB_REFCLK_L8N
FMC_DpM2C_P8	AU1	GXB_RX_R0P,GXB_REFCLK_R0P
FMC_DpM2C_N8	AU2	GXB_RX_R0N,GXB_REFCLK_R0N
FMC_DpM2C_P7	U1	GXB_RX_R10P,GXB_REFCLK_R10P
FMC_DpM2C_N7	U2	GXB_RX_R10N,GXB_REFCLK_R10N
FMC_DpM2C_P6	R1	GXB_RX_R11P,GXB_REFCLK_R11P
FMC_DpM2C_N6	R2	GXB_RX_R11N,GXB_REFCLK_R11N
FMC_DpM2C_P5	AR1	GXB_RX_R1P,GXB_REFCLK_R1P
FMC_DpM2C_N5	AR2	GXB_RX_R1N,GXB_REFCLK_R1N
FMC_DpM2C_P4	AN1	GXB_RX_R2P,GXB_REFCLK_R2P
FMC_DpM2C_N4	AN2	GXB_RX_R2N,GXB_REFCLK_R2N
FMC_DpM2C_P3	AE1	GXB_RX_R6P,GXB_REFCLK_R6P
FMC_DpM2C_N3	AE2	GXB_RX_R6N,GXB_REFCLK_R6N
FMC_DpM2C_P2	AC1	GXB_RX_R7P,GXB_REFCLK_R7P
FMC_DpM2C_N2	AC2	GXB_RX_R7N,GXB_REFCLK_R7N
FMC_DpM2C_P1	AA1	GXB_RX_R8P,GXB_REFCLK_R8P
FMC_DpM2C_N1	AA2	GXB_RX_R8N,GXB_REFCLK_R8N
FMC_DpM2C_P0	W1	GXB_RX_R9P,GXB_REFCLK_R9P
FMC_DpM2C_N0	W2	GXB_RX_R9N,GXB_REFCLK_R9N

Actual pinout

	AD38	GXB_RX_L7P,GXB_REFCLK_L7P
FMC_DpM2C_P9	AB39	GXB_RX_L7N,GXB_REFCLK_L7N
FMC_DpM2C_N9	AB38	GXB_RX_L8P,GXB_REFCLK_L8P
FMC_DpM2C_P5	AU1	GXB_RX_L8N,GXB_REFCLK_L8N
FMC_DpM2C_N5	AU2	GXB_RX_R0P,GXB_REFCLK_R0P
FMC_DpM2C_P0	U1	GXB_RX_R0N,GXB_REFCLK_R0N
FMC_DpM2C_N0	U2	GXB_RX_R10P,GXB_REFCLK_R10P
FMC_DpM2C_P1	R1	GXB_RX_R10N,GXB_REFCLK_R10N
FMC_DpM2C_N1	R2	GXB_RX_R11P,GXB_REFCLK_R11P
FMC_DpM2C_P6	AR1	GXB_RX_R11N,GXB_REFCLK_R11N
FMC_DpM2C_N6	AR2	GXB_RX_R1P,GXB_REFCLK_R1P
FMC_DpM2C_P4	AN1	GXB_RX_R1N,GXB_REFCLK_R1N
FMC_DpM2C_N4	AN2	GXB_RX_R2P,GXB_REFCLK_R2P
FMC_DpM2C_P7	AE1	GXB_RX_R2N,GXB_REFCLK_R2N
FMC_DpM2C_N7	AE2	GXB_RX_R6P,GXB_REFCLK_R6P
FMC_DpM2C_P3	AC1	GXB_RX_R6N,GXB_REFCLK_R6N
FMC_DpM2C_N3	AC2	GXB_RX_R7P,GXB_REFCLK_R7P
FMC_DpM2C_P8	AA1	GXB_RX_R7N,GXB_REFCLK_R7N
FMC_DpM2C_N8	AA2	GXB_RX_R8P,GXB_REFCLK_R8P
FMC_DpM2C_P2	W1	GXB_RX_R8N,GXB_REFCLK_R8N
FMC_DpM2C_N2	W2	GXB_RX_R9P,GXB_REFCLK_R9P
		GXB_RX_R9N,GXB_REFCLK_R9N

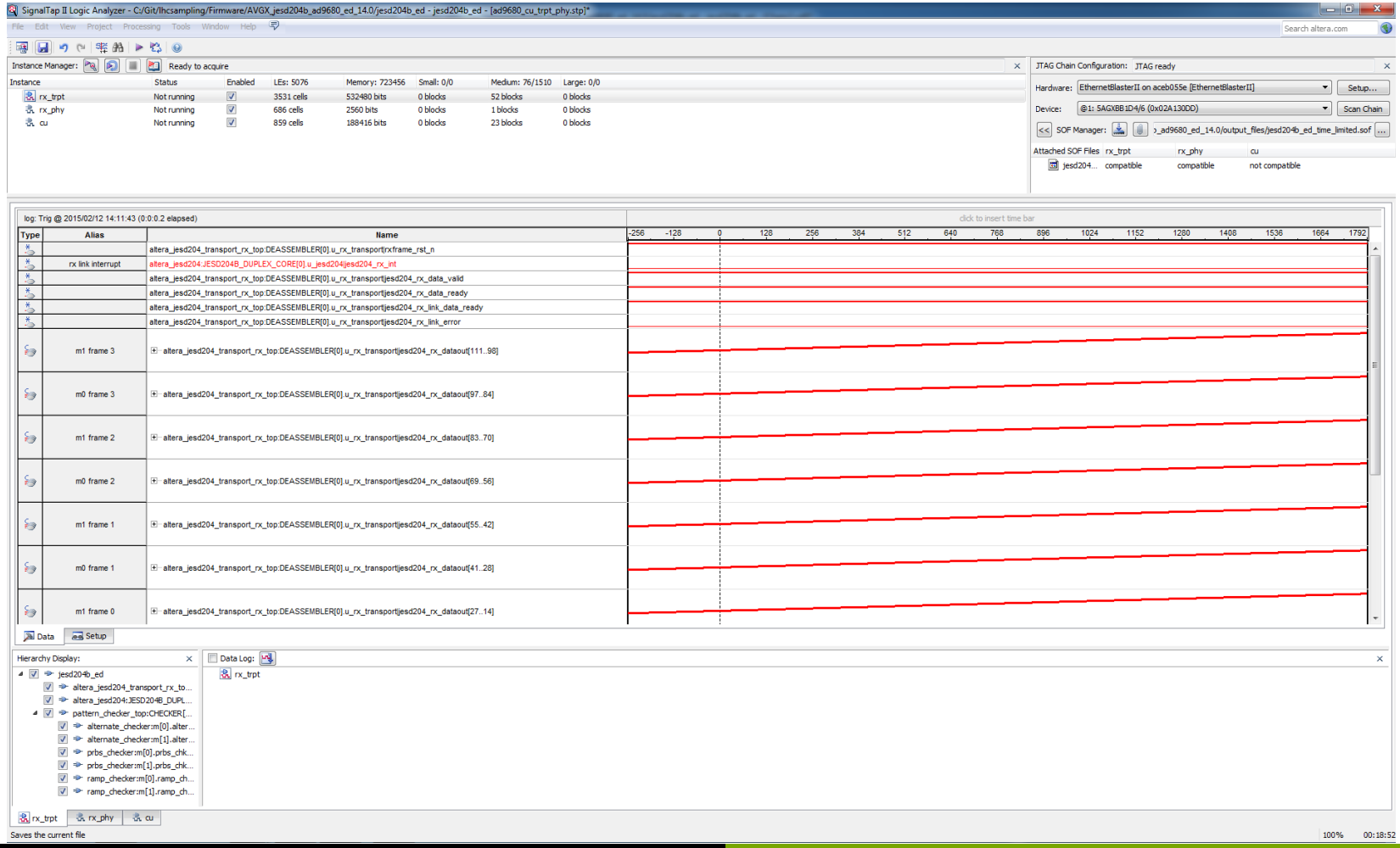
VFC-HPC integration – JESD204

- Loop-back modified. This has some consequences…



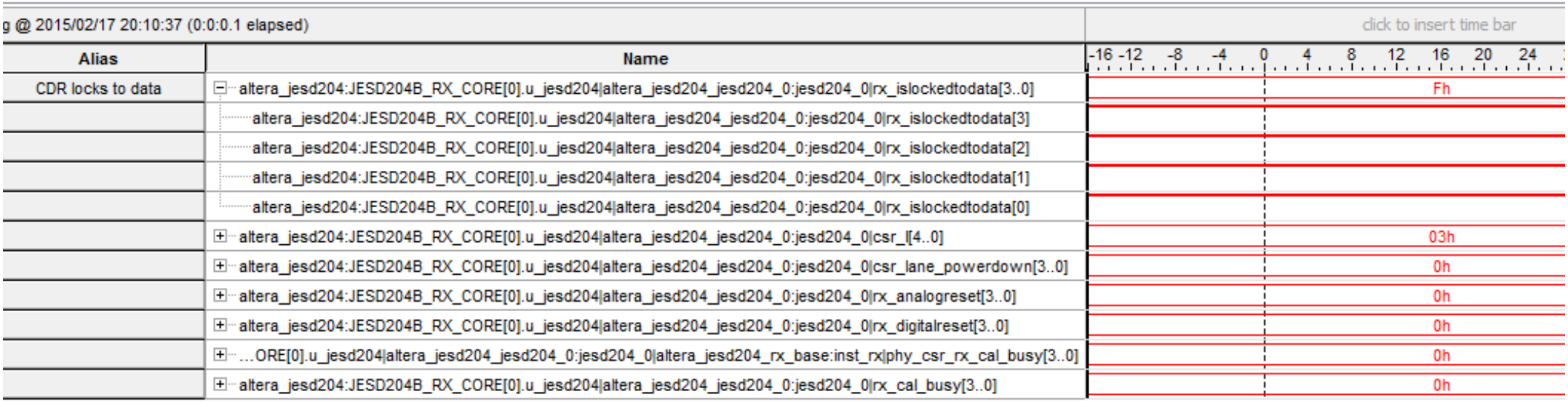
Firs results

- They really showed me that I keep being a naive dreamer… Things never work in the firs trial, despite it may seem so…
- Data at 500 MSPS, “ramp” test pattern. It looks nice…, but cautiousness led me to verify in detail the link status, and surprise!!…



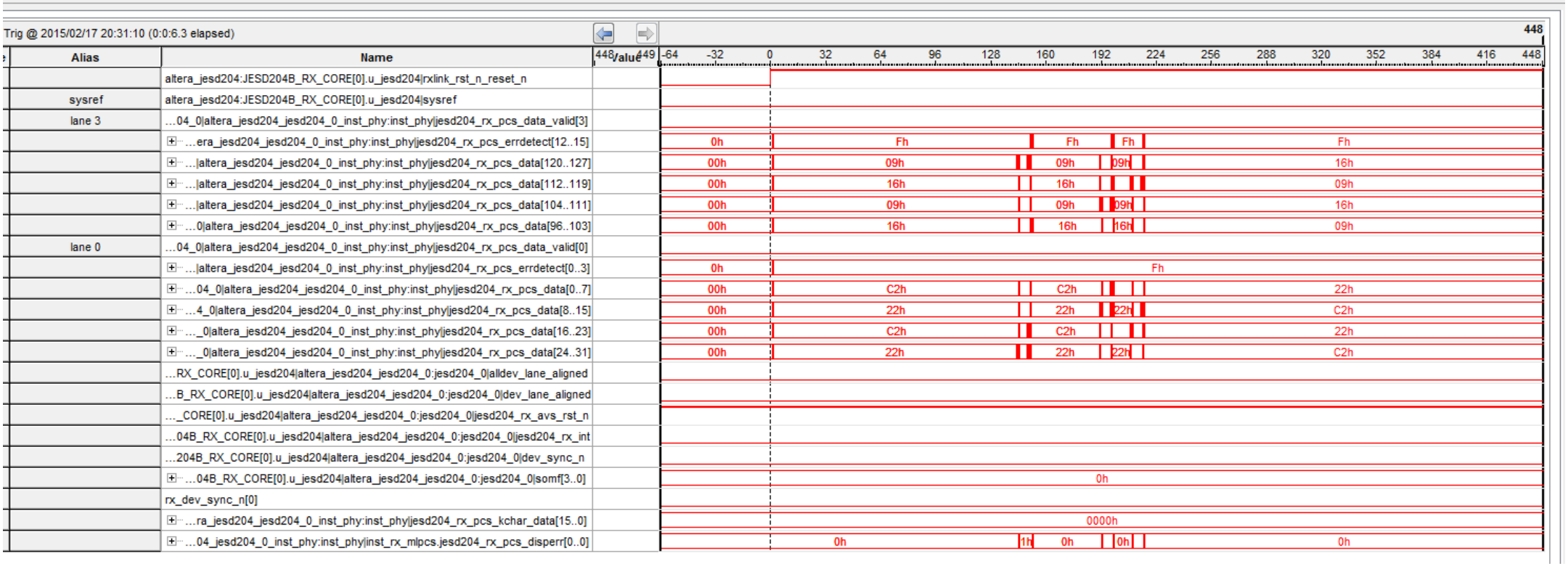
Firs results

- The physical layer seems to work



Firs results

- But the link layer doesn't.



- How is it that I could see the ramp?? Well I had a bug in the code and the internal loop was by default enabled => At least we know that the Transport layer does work ☺
- The source of the problem not identified yet… and not easy. The Duplex core would have helped a lot here…

- Now we are using the development board, but for the future we should look for a commercial FMC mezzanine:
  - Innovative (UK) => latest news is FMC-1000 for March. It houses the AD9680. The RF-Distributor outputs were designed to fit with their analog input requirements.
  - Delphi engineering (US) => reply from few days ago: "Delphi is quoting 16 week delivery on orders we are receiving now for the quad channel, 1.0 Gs/s 14 bit ADC FMC using the AD9680 ADC from ADI."

- On the other hand, Innovative claims that they already have since very recently an FMC-500 with parallel readout.
  - I'm not going to express my opinion about this…

Summary

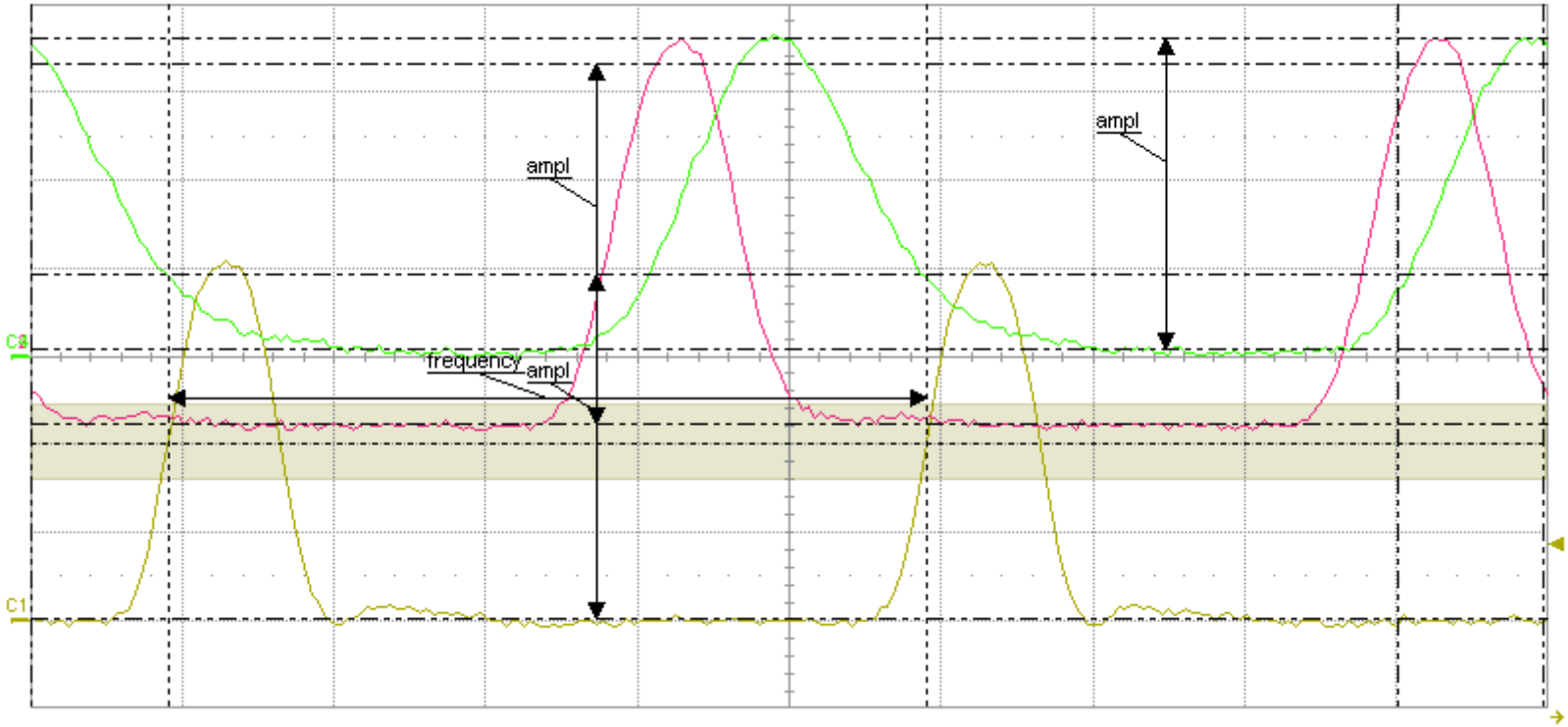
- The RF-Distributor to be tested soon, and with some luck it will work properly.
- Still work to do in the JESD204 link synchronization block. A lot. I'm debugging it getting some support from Altera, but any help is welcome. This part is essential for the system to work like a charm…
- In addition I had a bunch of ideas on how to do the signal processing that I should document. Already started time ago, but no time to finish it…
- Purchase decision to be taken:
  - Cross-check again the technical details (analog and digital signals)
  - And pray to have one before summer…
- Due to the bad experience with mismatched version of documents, maybe we should really think about an unified methodology of working using SVN or Git.

- New Fellowship, Jiri Kral, is taking over these tasks.

Thank you for your attendance

BACKUP

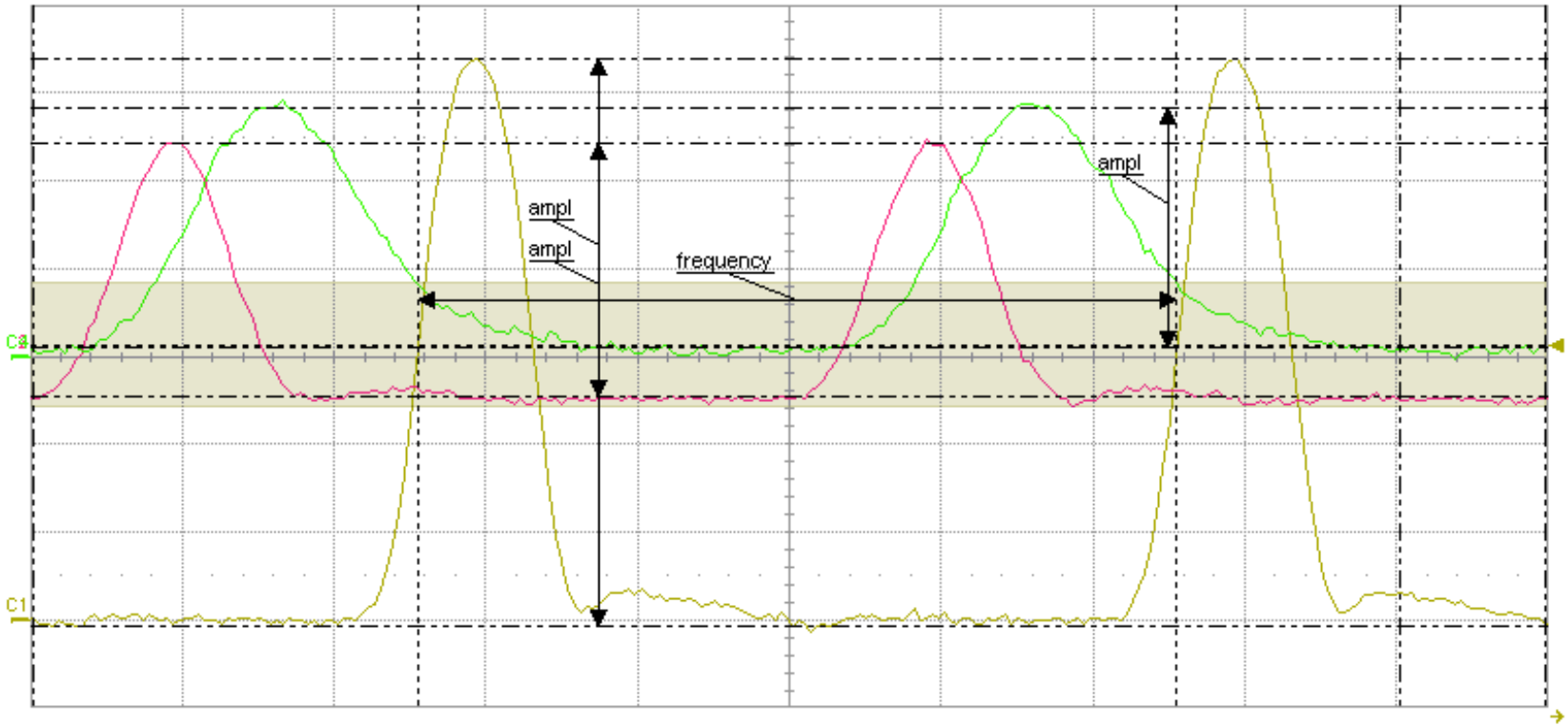
❑ 2V input, dab_lgs, dimfss_lgs



Measure	P1:ampl(C1)	P2:area(C1)	P3:ampl(C2)	P4:area(C2)	P5:ampl(C4)	P6:area(C4)	P7:width(C4)	P8:freq(C1)
value	1.962 V	15.2775 nVs	820.0 mV	2.1849 nVs	177.1 mV	2.55222 nVs	6.368 ns	40.028 MHz
mean	2.01616 V	15.37233 nVs	862.122 mV	2.172630 nVs	172.903 mV	2.559366 nVs	6.45233 ns	40.01955 MHz
min	1.754 V	15.1911 nVs	549.5 mV	2.0889 nVs	143.4 mV	2.53974 nVs	6.224 ns	39.892 MHz
max	2.096 V	15.6263 nVs	915.2 mV	2.2502 nVs	185.6 mV	2.57654 nVs	7.125 ns	40.118 MHz
sdev	53.10 mV	63.237 pVs	32.096 mV	36.668 pVs	3.776 mV	6.0377 pVs	90.09 ps	34.35 kHz
num	1.276e+3	1.276e+3	1.276e+3	1.276e+3	1.276e+3	1.276e+3	1.276e+3	1.276e+3
status	✔	✔	✔	✔	✔	✔	✔	✔

C1 DC1M 500 mV/div -1.500 V ofst | C2 DC50 200 mV/div 0.0 mV ofst | C4 DC50 50.0 mV/div 0.0 mV ofst | Timebase 29.0 ns 5.00 ns/div 250 S 5.0 GS/s | Trigger C1 DC Normal 435 mV Edge Positive

- 1V, 10dB att, dab_hgs, dimfss_hgs



Measure	P1:ampl(C1)	P2:area(C1)	P3:ampl(C2)	P4:area(C2)	P5:ampl(C4)	P6:area(C4)	P7:width(C4)	P8:freq(C1)
value	323 mV	2.50211 nVs	144.3 mV	-124.80 pVs	27.37 mV	417.968 pVs	6.293 ns	40.051 MHz
mean	318.06 mV	2.499573 nVs	147.157 mV	-125.4121 pVs	28.138 mV	417.4114 pVs	6.32027 ns	40.00896 MHz
min	268 mV	2.47651 nVs	102.7 mV	-131.51 pVs	22.2 mV	407.280 pVs	6.000 ns	39.935 MHz
max	330 mV	2.52323 nVs	153.6 mV	-118.72 pVs	30.1 mV	430.127 pVs	7.342 ns	40.092 MHz
sdev	8.97 mV	6.8606 pVs	3.977 mV	1.7367 pVs	943 µV	3.48886 pVs	96.68 ps	25.68 kHz
num	1.122e+3	1.122e+3	1.122e+3	1.122e+3	1.122e+3	1.122e+3	2.244e+3	1.122e+3
status	⚠	✔	✔	✔	✔	✔	✔	⚠

C1 DC1M 50.0 mV/div -150.0 mV | C2 DC50 50.0 mV/div 0.0 mV ofst | C4 DC50 10.0 mV/div 0.00 mV ofst | Timebase 38.0 ns 5.00 ns/div 250 S 5.0 GS/s | Trigger C1 DC Norm. 155.5 mV Edge Positive

❑ Spectrum analyzer

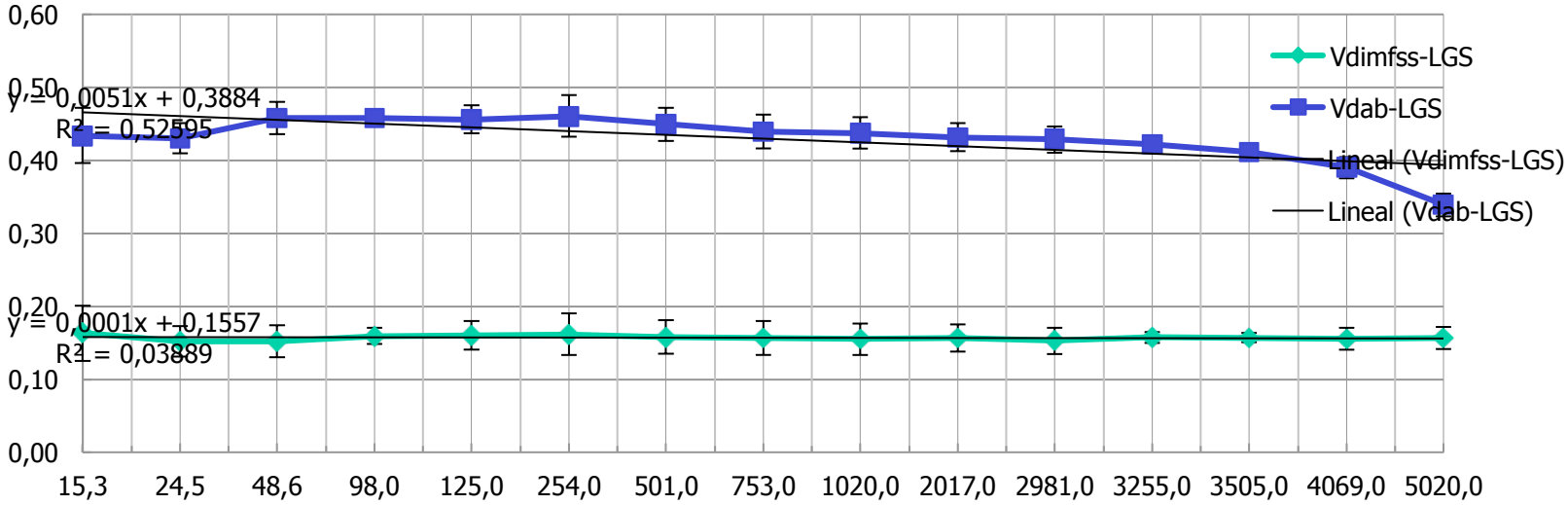
Spectrum analyzer noise figure: ~ -152 dBm

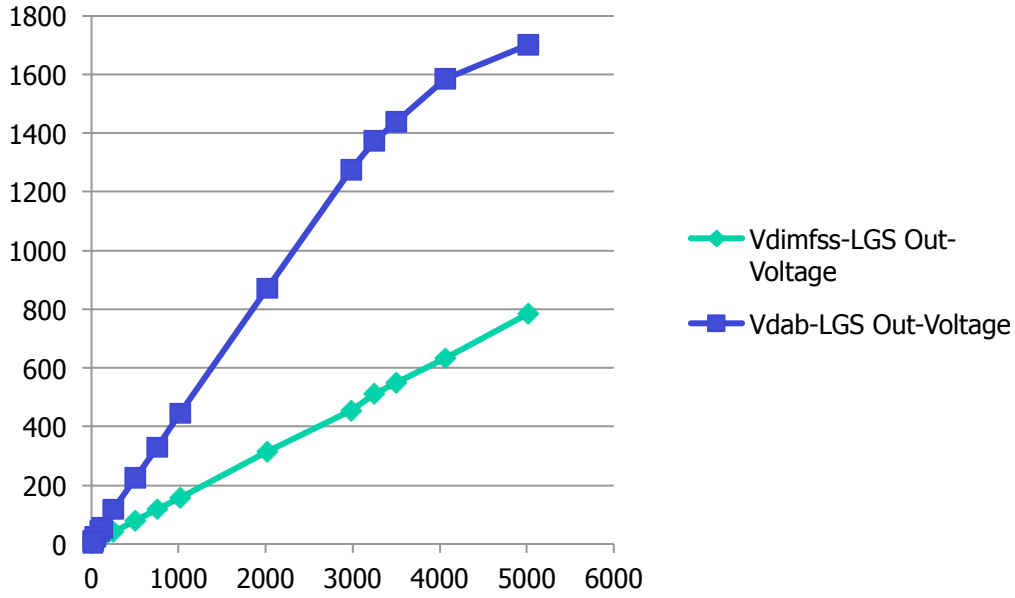
Measurements, no shield, not all lines loaded

Output	"@ 60MHz"	"@ 200MHz"	"@ 600MHz"		"@ 60MHz"	"@ 200MHz"	"@ 600MHz"
Dimfss-HighGainStage	-137,8	-138,1	-149,8		28,806	27,828	7,236
Dimfss-LowGainStage	-155,7	-154,6	-151,8		3,668	4,164	5,748
Dab-HighGainStage	-126,9	-129,2	-142,2		101,038	77,533	17,357
Dab-LowGainStage	-144,5	-146,5	-152,5		13,319	10,58	5,303
			dBm/Hz				nV/sqrt(Hz)

Resonance: 933 MHz

Linearity tests Low Gain Stage





Linearity tests High Gain Stage