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# Upgrade of the ALICE Inner Tracking System

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L. Musa - CERN

*CLIC Tracker Technology Meeting  
CERN, 05 March, 2015*

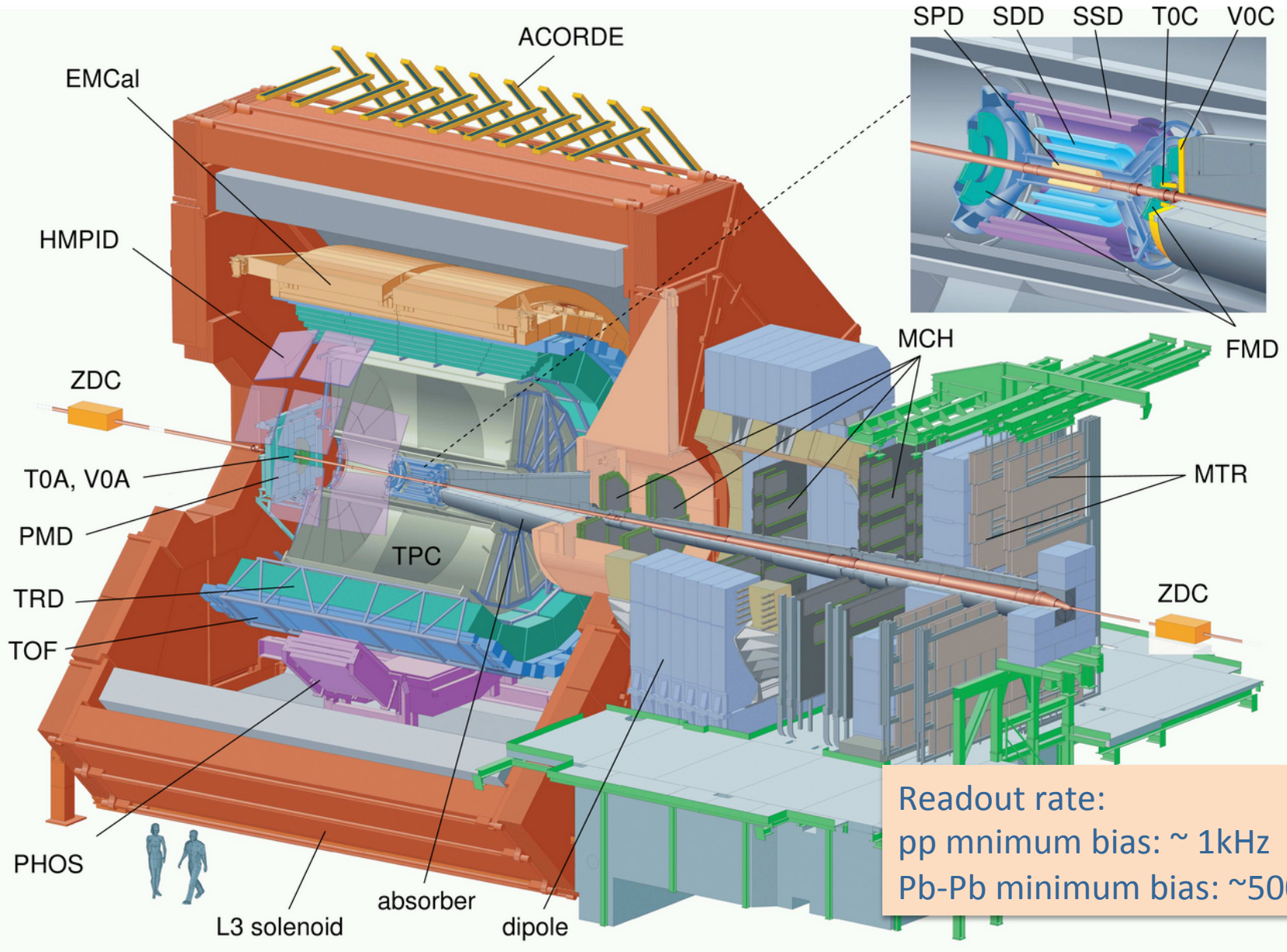
# Upgrade of the ALICE Inner Tracking System

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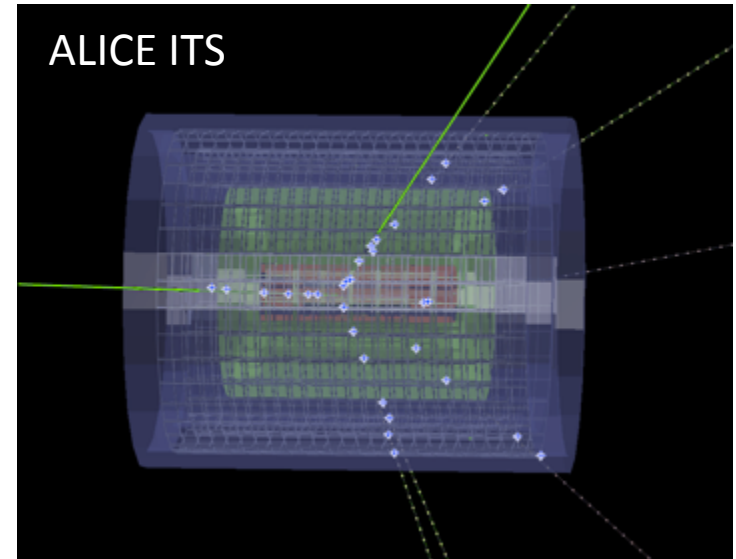
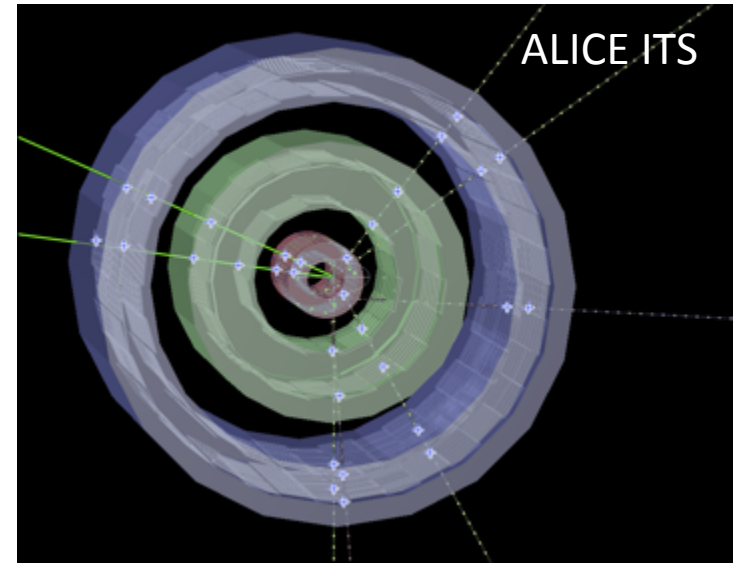
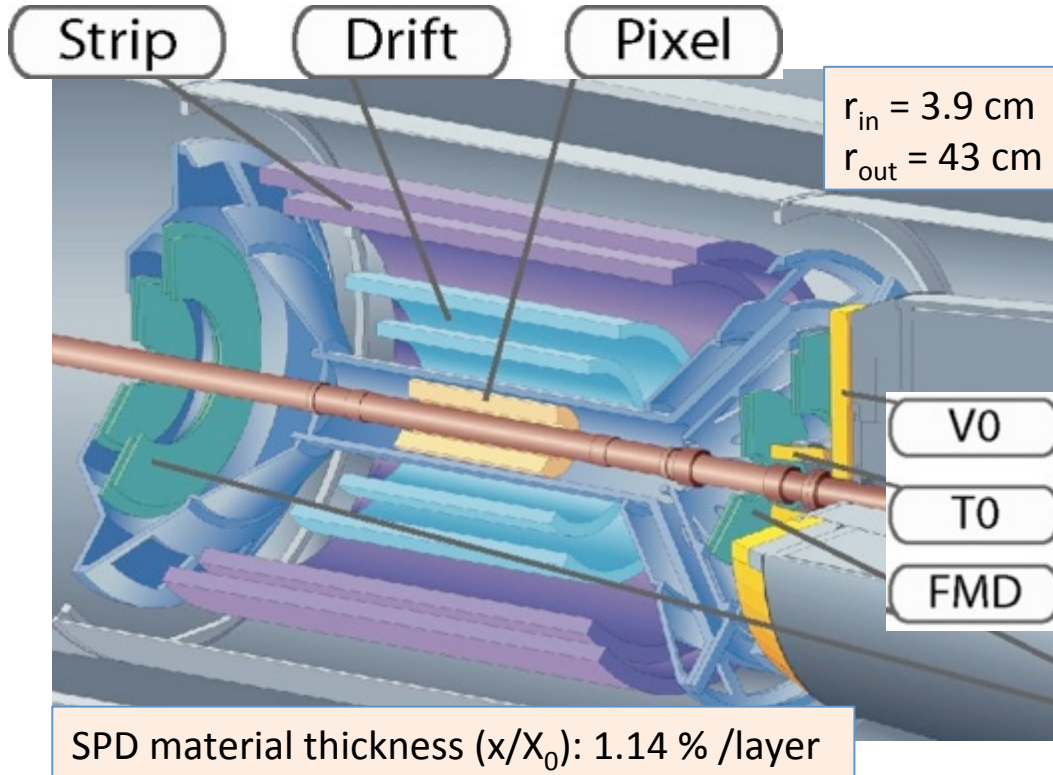
## OUTLINE

- ⦿ ALICE current set-up
- ⦿ Upgrade motivations and objectives
- ⦿ ITS upgrade layout and main components
- ⦿ Detector simulated performance: some examples

# The Current ALICE Detector



# The Current ALICE Inner Tracking System

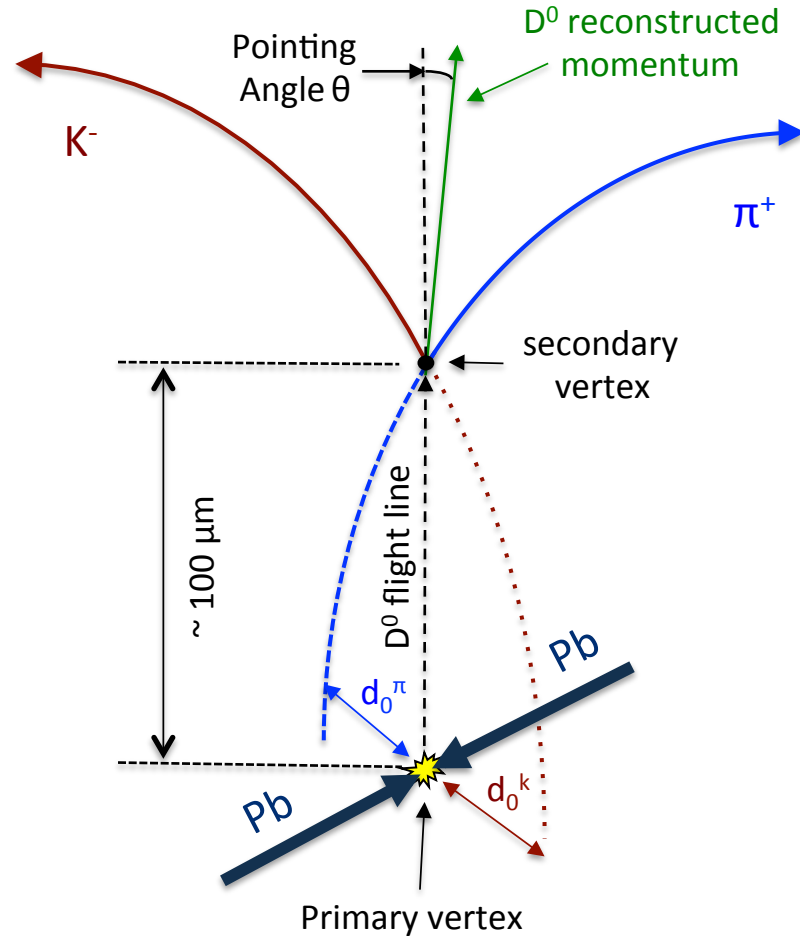


## Current ITS

6 concentric barrels, 3 different technologies

- 2 layers of silicon pixel (SPD)
- 2 layers of silicon drift (SDD)
- 2 layers of silicon strips (SSD)

## Example: $D^0$ meson



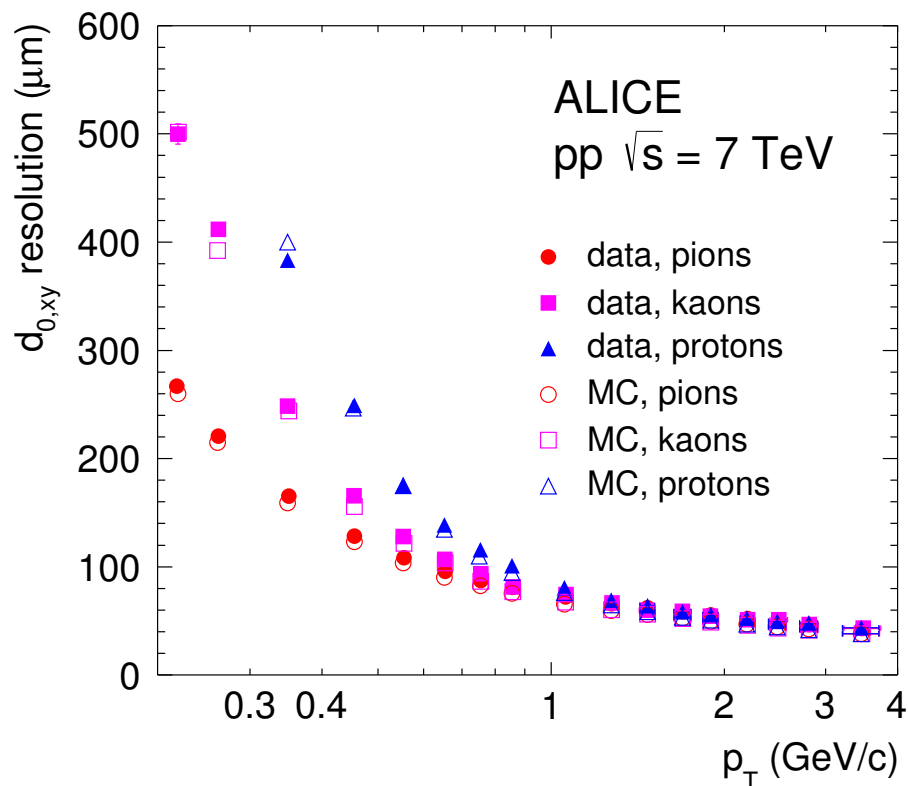
## Open charm

Particle	Decay Channel	$c\tau$ ( $\mu\text{m}$ )
$D^0$	$K^- \pi^+$ (3.8%)	123
$D^+$	$K^- \pi^+ \pi^+$ (9.5%)	312
$D_s^+$	$K^+ K^- \pi^+$ (5.2%)	150
$\Lambda_c^+$	$p K^- \pi^+$ (5.0%)	60

How precisely is  $d_0$  measured with the current ITS detector?

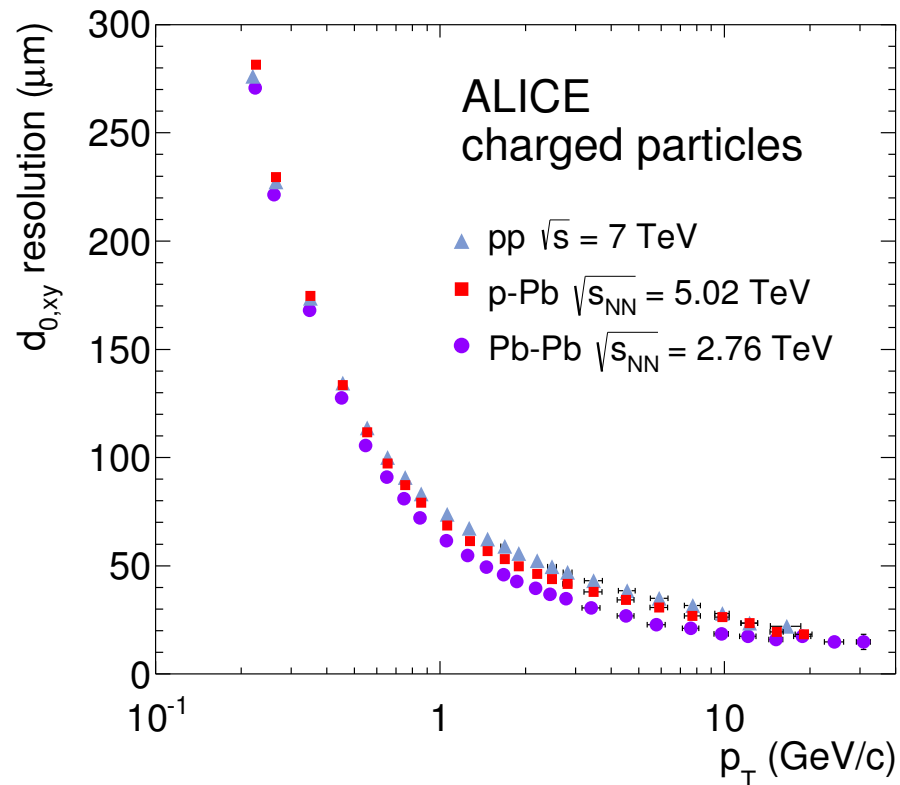
Analysis based on decay topology and invariant mass technique

Very good MC description



ALICE, Int. J. Mod. Phys. A29 (2014) 1430044

Very weak dependence on the colliding system



ALICE, Int. J. Mod. Phys. A29 (2014) 1430044

70  $\mu\text{m}$  at  $p_T = 1$  GeV/c

# What determines the impact parameter resolution

## Vertex projection from two points: a simplified approach (telescope equation)

expectations for the ITS upgraded → pointing resolution =  $(5 \oplus 22\text{GeV}/p \cdot c) \mu\text{m}$

from  
detector  
position  
error

from  
coulomb  
scattering

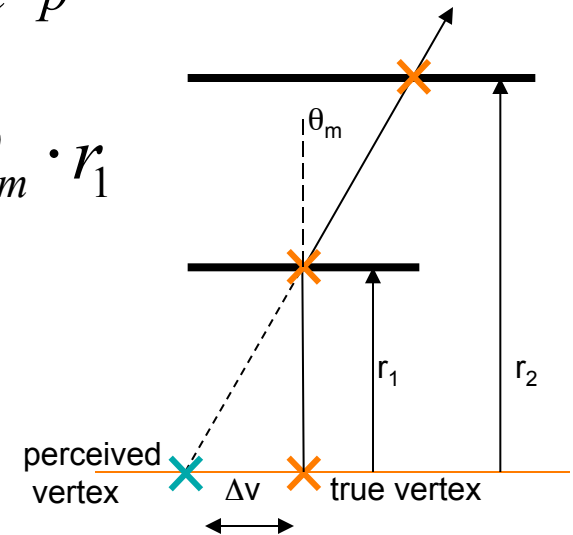
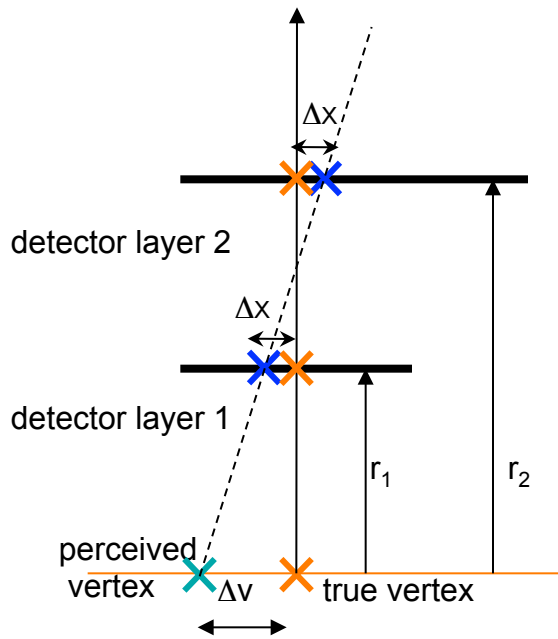
first pixel layer

$$X_0 = 0.3\%$$

$$\Delta v = \Delta x \cdot \sqrt{\frac{r_2^2 + r_1^2}{(r_2 - r_1)^2}}$$

$$\theta_m = \frac{13.6\text{Mev}}{\beta \cdot c \cdot p} \cdot \sqrt{X_0}$$

$$\Delta v = \theta_m \cdot r_1$$



## Minimum bias Pb-Pb at 5.5 Tev

Particle	Eff	$S/ev$	$S/B$	$B'/ev$	trigger / event	$S/nb^{-1}$
$D^0$	0.02	$1.6 \cdot 10^{-3}$	0.03	0.21	0.11	$1.3 \cdot 10^7$
$D_s^+$	0.01	$4.6 \cdot 10^{-4}$	0.01	0.18	0.09	$3.7 \cdot 10^6$
$\Lambda_c$	0.01	$1.4 \cdot 10^{-4}$	$5 \cdot 10^{-5}$	11	0.5	$1.1 \cdot 10^6$
$\Lambda_c (p_t > 2 Gev/c)$	0.01	$0.8 \cdot 10^{-4}$	0.001	0.33	0.16	$0.6 \cdot 10^6$
$B \rightarrow D^0(\rightarrow K^- \pi^+)$	0.02	$0.8 \cdot 10^{-4}$	0.03	$11 \cdot 10^{-3}$	$5 \cdot 10^{-3}$	$0.6 \cdot 10^6$
$B \rightarrow J/\psi(\rightarrow e^+e^-)$	0.1	$1.3 \cdot 10^{-5}$	0.01	$5 \cdot 10^{-3}$	$3 \cdot 10^{-3}$	$1 \cdot 10^5$
$B^+ \rightarrow J/\psi K^+$	0.01	$0.5 \cdot 10^{-7}$	0.01	$2 \cdot 10^{-5}$	$1 \cdot 10^{-5}$	$4 \cdot 10^{-3}$
$B^+ \rightarrow \bar{D}^0 \pi^+$	0.01	$1.9 \cdot 10^{-7}$	0.01	$8 \cdot 10^{-5}$	$4 \cdot 10^{-5}$	$1.5 \cdot 10^3$
$B_s^0 \rightarrow J/\psi \phi$	0.01	$1.1 \cdot 10^{-8}$	0.01	$4.4 \cdot 10^{-6}$	$2 \cdot 10^{-6}$	$9 \cdot 10^1$
$\Lambda_b(\rightarrow \Lambda_c + e^-)$	0.01	$0.7 \cdot 10^{-6}$	0.01	$2.8 \cdot 10^{-4}$	$14 \cdot 10^{-5}$	$5 \cdot 10^3$
$\Lambda_b(\rightarrow \Lambda_c + h^-)$	0.01	$0.7 \cdot 10^{-5}$	0.01	$2.8 \cdot 10^{-3}$	$1.4 \cdot 10^{-3}$	$5 \cdot 10^4$

We assume a trigger efficiency  $\epsilon_{\text{trigger}} = 100\%$

$B'$  = background in the broad invariant mass range (e.g.  $\pm 12\sigma$ )

An IDEAL “charm trigger” would select almost all events



High precision measurements of rare probes at low  $p_T$ , which cannot be selected with a trigger, require a large sample of events recorded on tape

## Target

- Pb-Pb recorded luminosity  $\geq 10 \text{ nb}^{-1} \rightarrow 8 \times 10^{10} \text{ events}$
- pp (@5.5 Tev) recorded luminosity  $\geq 6 \text{ pb}^{-1} \rightarrow 1.4 \times 10^{11} \text{ events}$

Gain a factor **100** in statistics over approved programme

... and significant improvement of vertexing and tracking capabilities

## I. Upgrade the ALICE readout systems and online systems to

- read out all Pb-Pb interactions at a maximum rate of **50kHz** (i.e.  $L = 6 \times 10^{27} \text{ cm}^{-1}\text{s}^{-1}$ ), with a minimum bias trigger
- Perform **online data reduction** based on reconstruction of clusters and tracks (tracking used only to filter out clusters not associated to reconstructed tracks)

## II. Improve vertexing and tracking at low $p_T$

- The upgrade plans entails building

- New, high-resolution, high-rate ITS
- Upgrade of TPC with replacement of MWPCs with GEMs and new pipelined readout electronics
- Upgrade of readout electronics of: TRD, TOF, PHOS and Muon Spectrometer
- Upgrade of the forward trigger detectors and ZDC
- Upgrade of the online systems (DAQ & HLT)
- Upgrade of the offline reconstruction framework

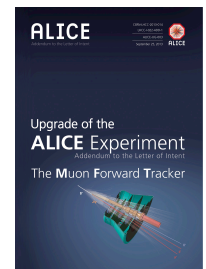
02

- New 5-plane silicon telescope in front of the hadron absorber covering the acceptance of the muon Spectrometer

- It targets 2018/19 (LHC 2<sup>nd</sup> Long Shutdown)



LoI  
Sep 2012



Add. LoI  
Sep 2013

# ITS upgrade design objectives

## 1. Improve impact parameter resolution by a factor of $\sim 3$

- Get closer to IP (position of first layer): 39mm  $\rightarrow$  22mm
- Reduce  $x/X_0$  /layer:  $\sim 1.14\%$   $\rightarrow$   $\sim 0.3\%$  (for inner layers)
- Reduce pixel size: currently  $50\mu\text{m} \times 425\mu\text{m}$   $\rightarrow$   $O(30\mu\text{m} \times 30\mu\text{m})$

## 2. Improve tracking efficiency and $p_T$ resolution at low $p_T$

- Increase granularity:
  - 6 layers  $\rightarrow$  7 layers
  - silicon drift and strips  $\rightarrow$  pixels

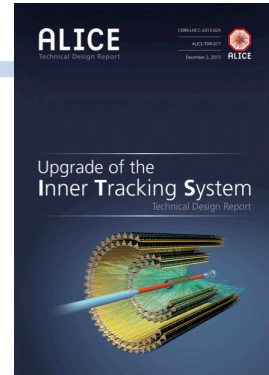
## 3. Fast readout

- readout Pb-Pb interactions at  $> 50$  kHz and pp interactions at  $\sim$  several  $10^5$  Hz (currently limited at 1kHz with full ITS and  $\sim 3$ kHz without silicon drift)

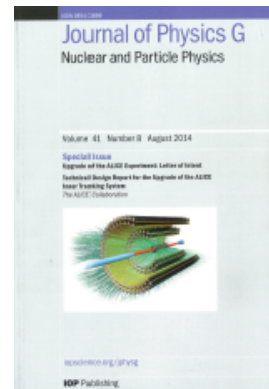
## 4. Fast insertion/removal for yearly maintenance

- possibility to replace non functioning detector modules during yearly shutdown

Install detector during LHCC LS2 (2018-19)



CERN-LHCC-2013-24



*J. Phys. G* (41) 087002

# New ITS Layout



12.5 G-pixel camera  
( $\sim 10 \text{ m}^2$ )

$\eta$  coverage:  $|\eta| \leq 1.22$   
for tracks from 90% most  
luminous region

r coverage:  
23 – 400 mm

Outer layers

Middle layers

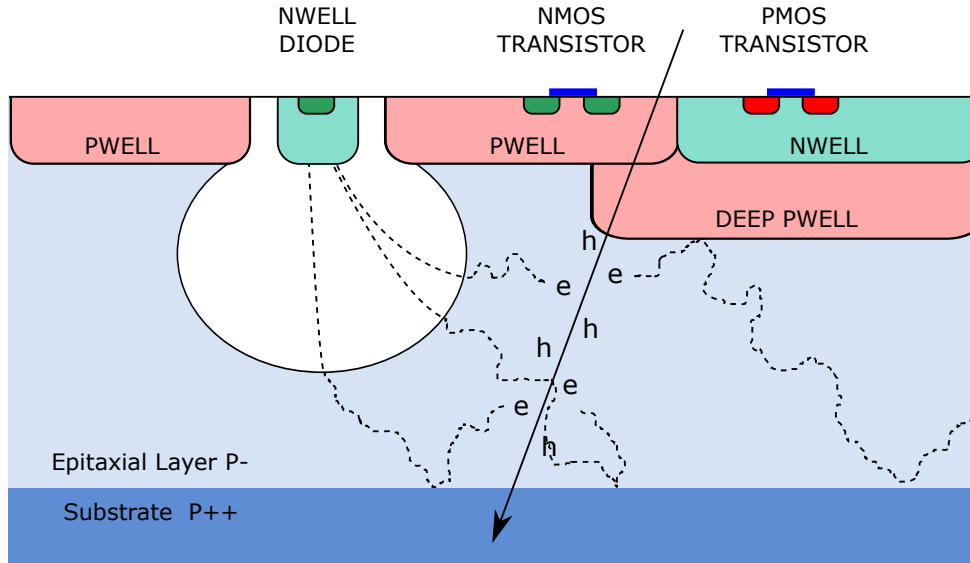
Inner layers

Beam pipe

7 layers of MAPS

700 krad/  $10^{13}$  1 MeV  $n_{eq}$   
includes safety factor 10

## CMOS Pixel Sensor using TowerJazz 0.18 $\mu\text{m}$ CMOS Imaging Process

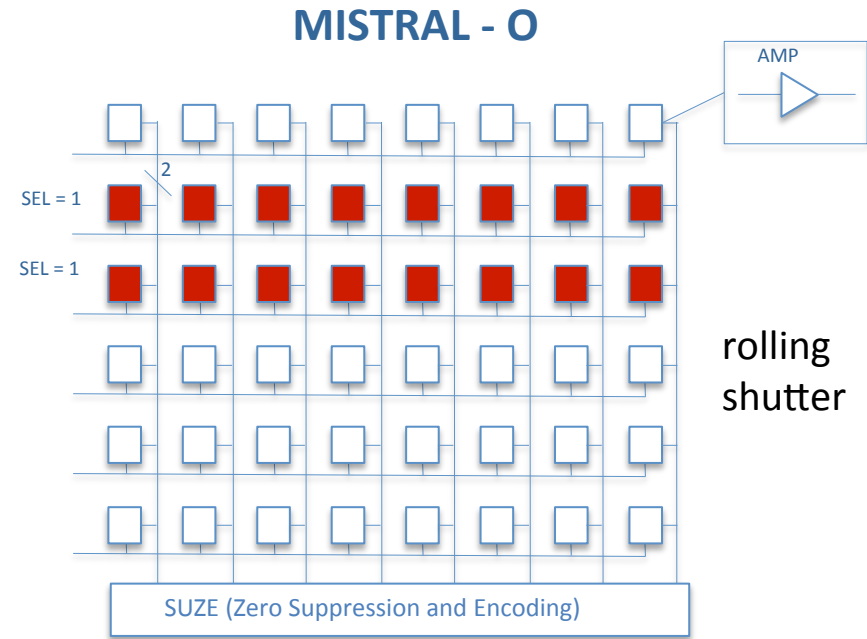
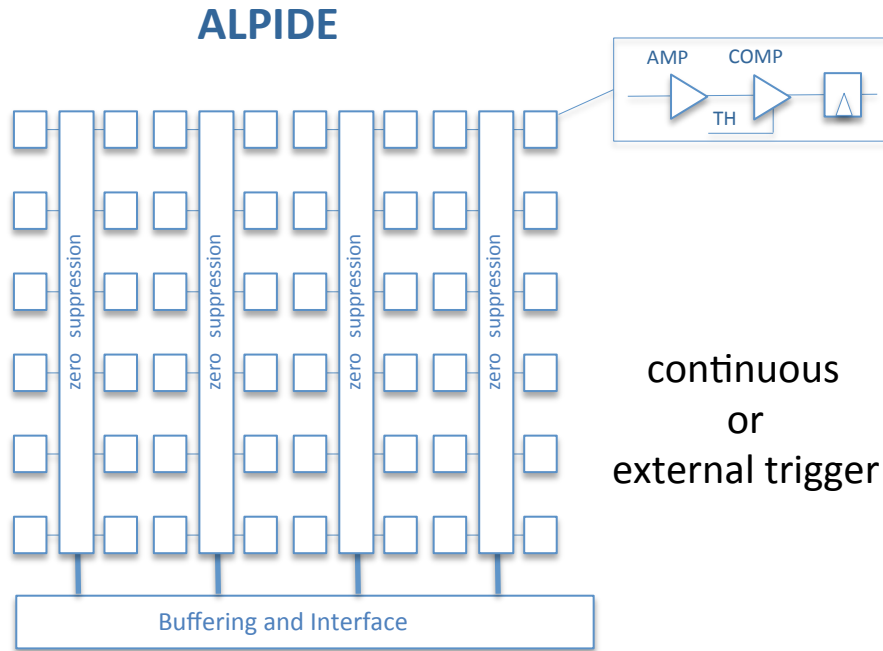


### Tower Jazz 0.18 $\mu\text{m}$ CMOS

- feature size 180 nm
- metal layers 6
- ➔ Suited for high-density, low-power
- Gate oxide 3nm
- ➔ Circuit rad-tolerant

- ▶ High-resistivity ( $> 1\text{k}\Omega\text{ cm}$ ) p-type epitaxial layer (20 $\mu\text{m}$  - 40 $\mu\text{m}$  thick) on p-type substrate
- ▶ Small n-well diode (2-3  $\mu\text{m}$  diameter),  $\sim 100$  times smaller than pixel  $\Rightarrow$  low capacitance
- ▶ Application of (moderate) reverse bias voltage to substrate can be used to increase depletion zone around NWELL collection diode
- ▶ Quadruple well process: deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area

# ITS Pixel Chip – two architectures



Pixel pitch **28 $\mu$ m x 28 $\mu$ m**  
Event time resolution  **$\sim$ 2 $\mu$ s**  
Power consumption **39mW/cm<sup>2</sup>**  
Dead area **1.1 mm x 30mm**

Pixel pitch **36 $\mu$ m x 64 $\mu$ m**  
Event time resolution  **$\sim$ 20 $\mu$ s**  
Power consumption(\*) **97mW/cm<sup>2</sup>**  
Dead area **1.7 mm x 30mm**

ALPIDE and MISTRAL-O have same **dimensions (15mm x 30mm)**, identical physical and electrical interfaces: position of interface pads, electrical signaling, protocol

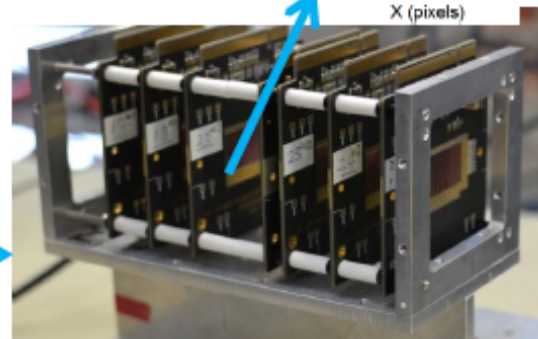
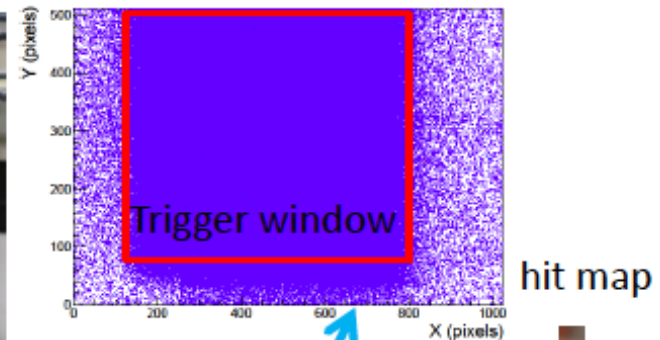
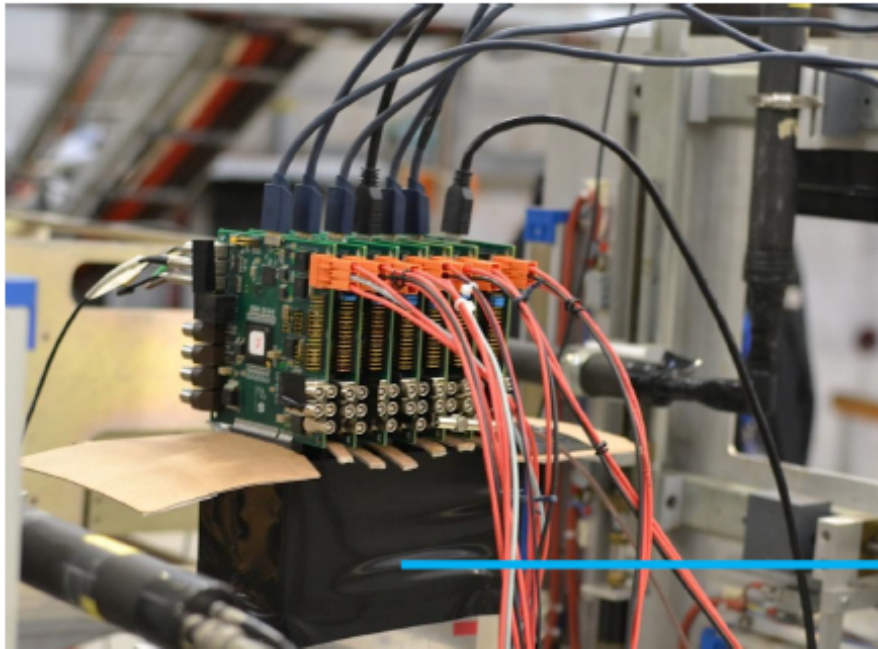
(\*) might further reduce to 73mW/cm<sup>2</sup>

## Intensive test beam campaign

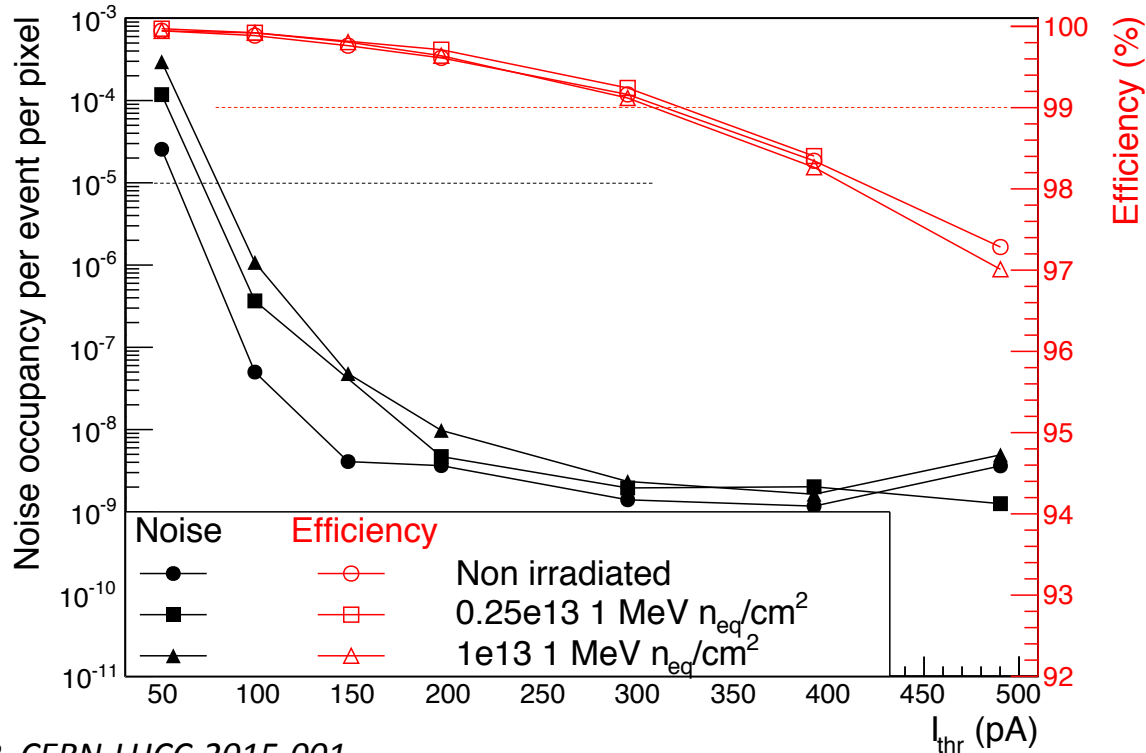
- PS: 5-7 GeV  $\pi^-$
- SPS: 120 GeV  $\pi^-$
- PAL (Korea): 60 MeV  $e^-$
- BTF (Frascati): 450 MeV  $e^-$
- DESY: 5.8 GeV  $e^+$

Scan of main parameters  $\rightarrow$   $\sim$  200 settings

## 7-plane telescope based on pALPIDE-1 chip



## Efficiency and fake hit rate



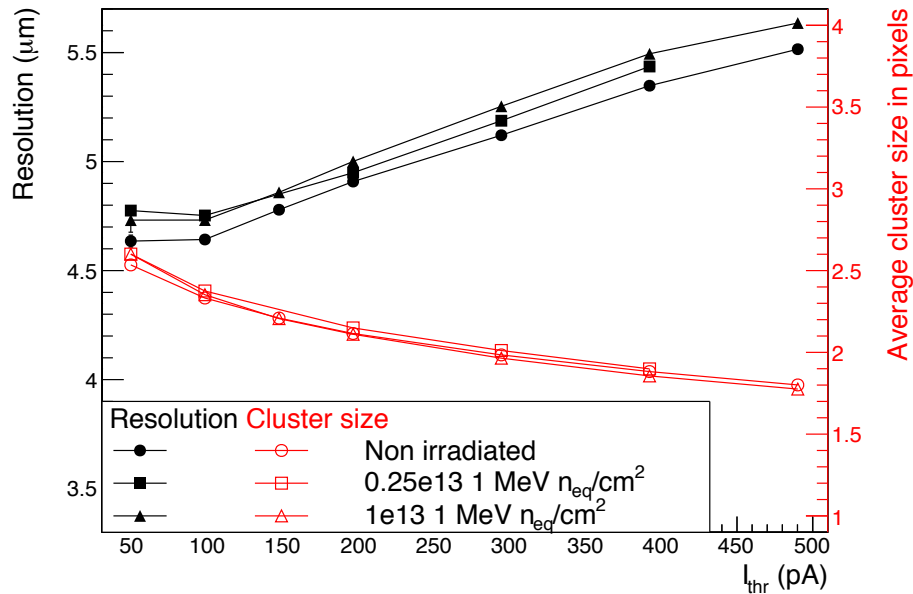
MFT TDR, CERN-LHCC-2015-001

$\lambda_{fake} \ll 10^{-5}$  / event/pixel @  $\epsilon_{det} > 99\%$  ➔ very large margin over design requirements

- Measurements at PS: 5 – 7 GeV  $\pi^-$  September 2014
- Results refer to 50  $\mu$ m thick chips: non irradiated and irradiated with neutrons  $0.25 \times 10^{13}$  and  $10^{13}$  1MeV  $n_{eq} / cm^2$

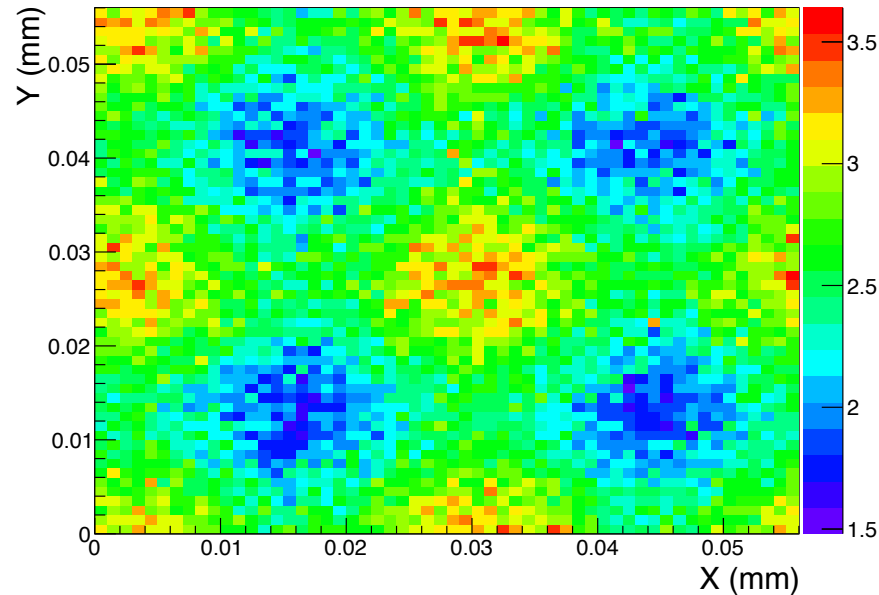


## Spatial resolution



MFT TDR, CERN-LHCC-2015-001

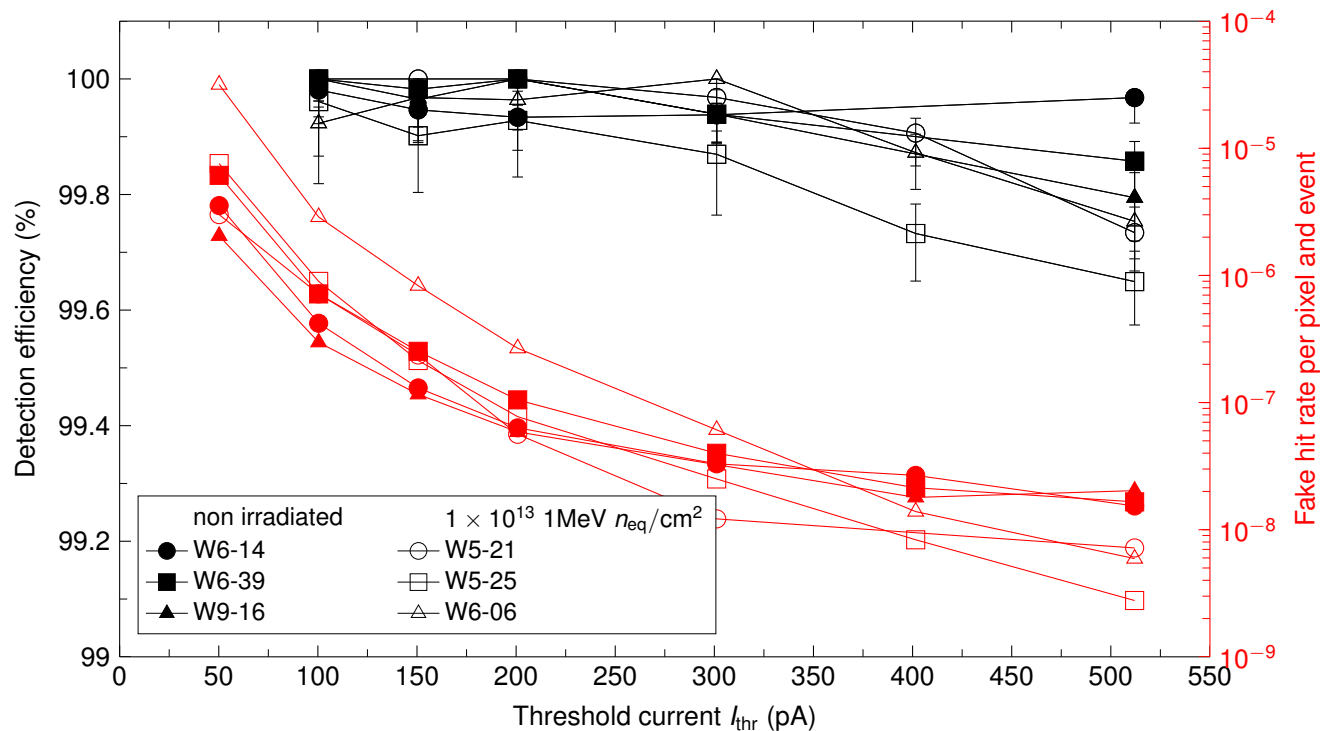
## Cluster size vs. position within pixel



$\sigma_{\text{det}} < 5 \mu\text{m}$  is achieved with sufficient margin of operation

- Measurements at PS: 5 – 7 GeV  $\pi^-$  September 2014
- Results refer to 50  $\mu\text{m}$  thick chips: non irradiated and irradiated with neutrons  $0.25 \times 10^{13}$  and  $10^{13}$  1MeV  $n_{\text{eq}} / \text{cm}^2$

## Efficiency and fake hit rate

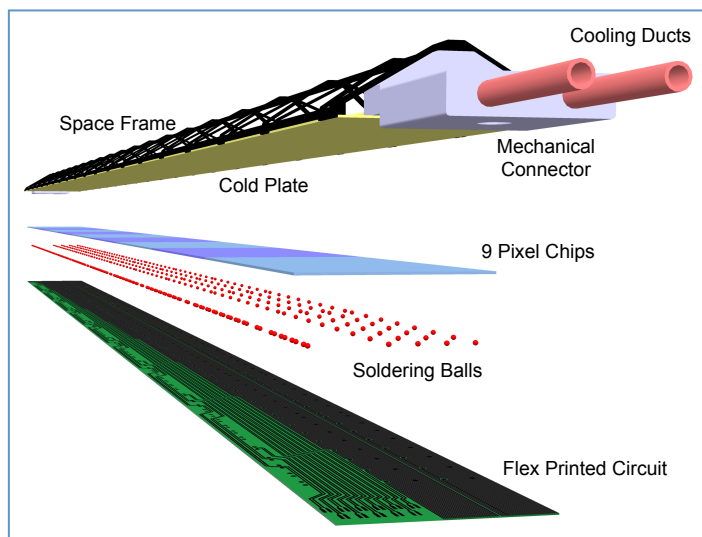
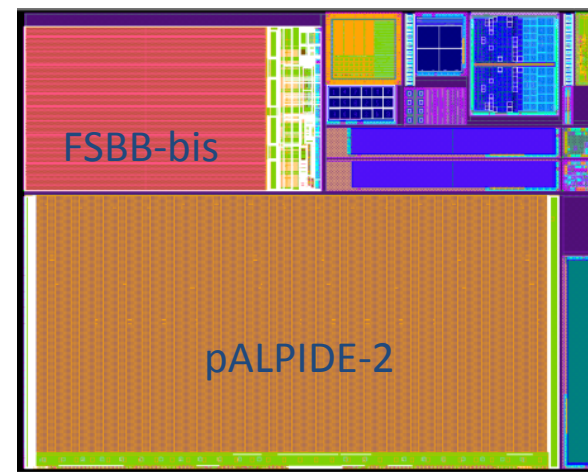


### Improved test-beam data analysis

- Measurements at PS: 5 – 7 GeV  $\pi^-$  December 2014
- Results refer to 50  $\mu\text{m}$  thick chips: 3 non irradiated and 3 irradiated with neutrons

## p-ALPIDE-2: 2<sup>nd</sup> full-scale prototype

- Optimization of some circuit blocks
- **NO high-speed output link** (1.2 Gbit/sec replaced by a 40Mb/s)
- Full Integration in IB and OB Module: main focus in 2015
- **Delivery: mid March**



## p-ALPIDE-3: 3<sup>rd</sup> full-scale prototype

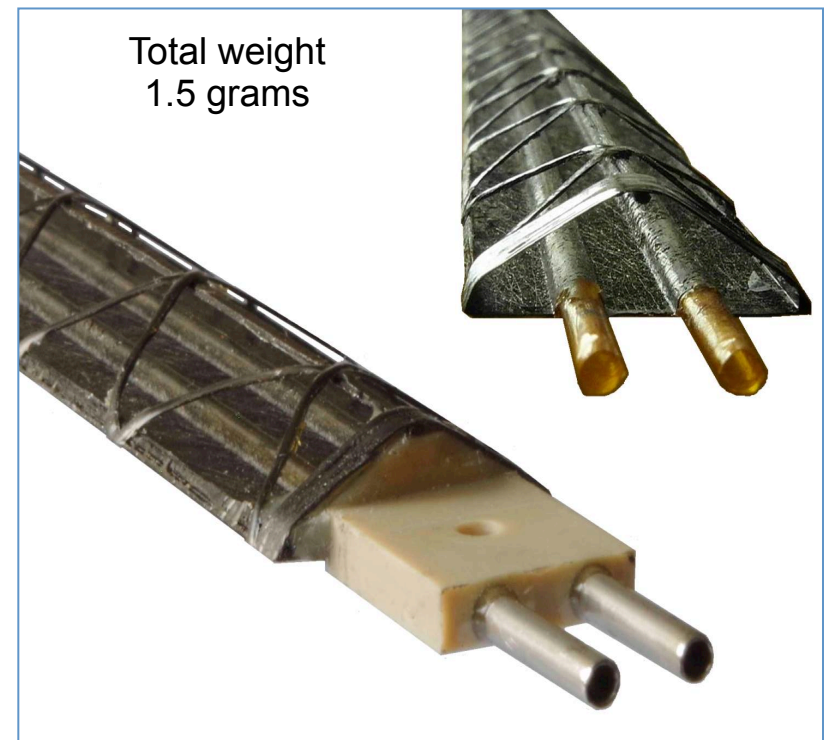
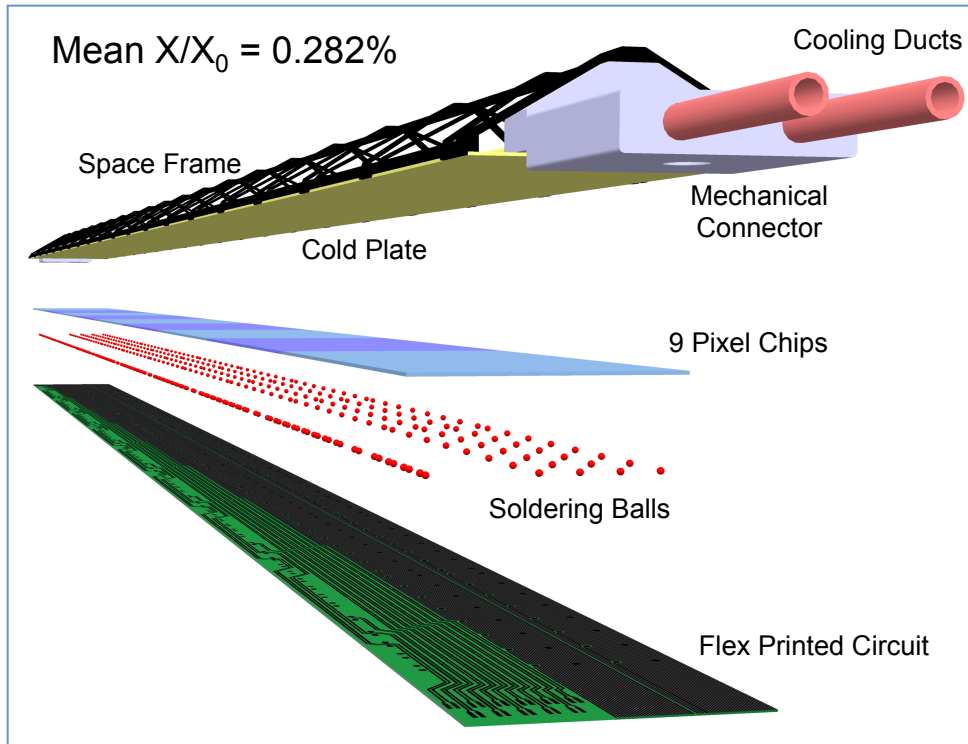
- Contains all final elements
- Submission: April '15      **Delivery: July '15**

## p-ALPIDE-4: pre-series production

- **Submission Dec '15**



# New ITS Layout - Inner Barrel



<Radius> (mm): 23,31,39

Nr. of staves: 12, 16, 20

Nr. of chips/layer: 108, 144, 180

Power density: < 100 mW/cm<sup>2</sup>

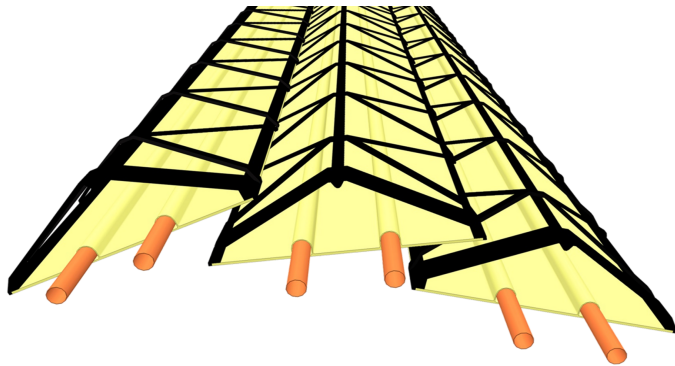
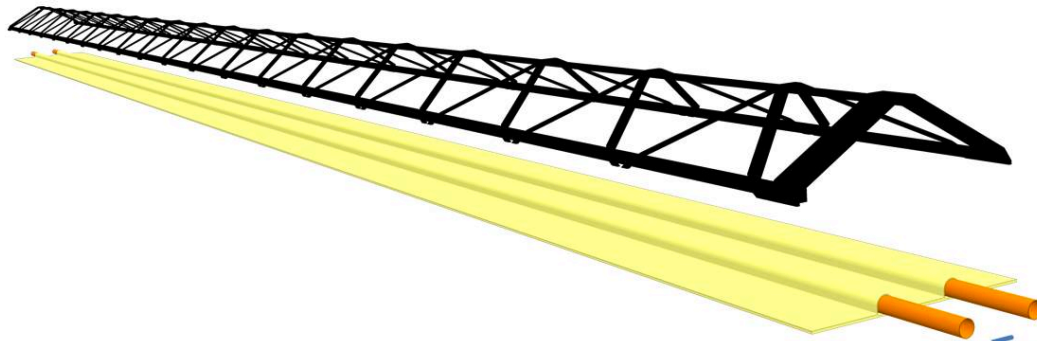
Length in z (mm): 270

Nr. of chips/stave: 9

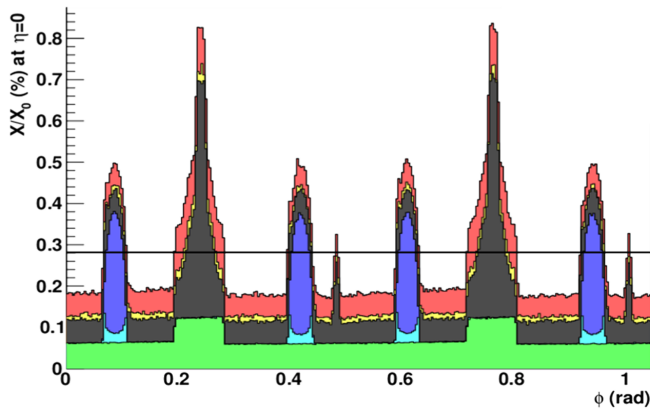
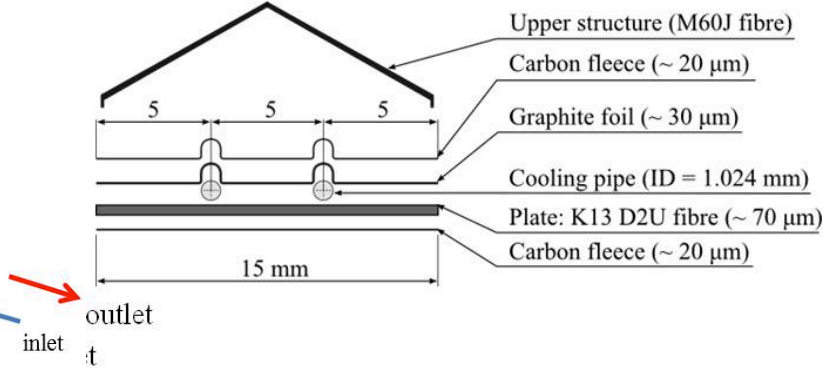
Material thickness:  $\sim 0.3\% X_0$

Throughput (@100kHz): < 80 Mb/s  $\times$  cm<sup>-2</sup>

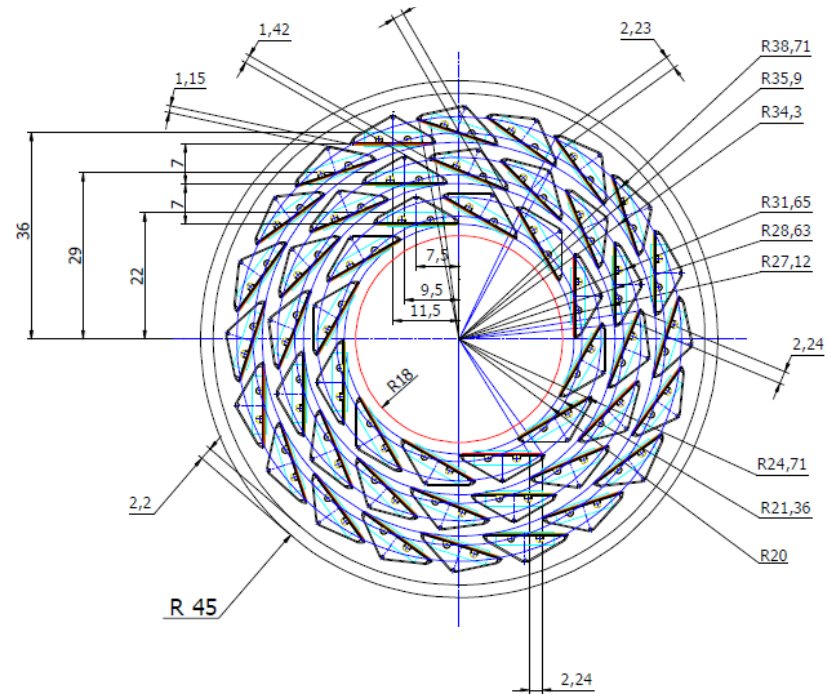
# Inner Barrel – Geometry and material budget



Transversal section:



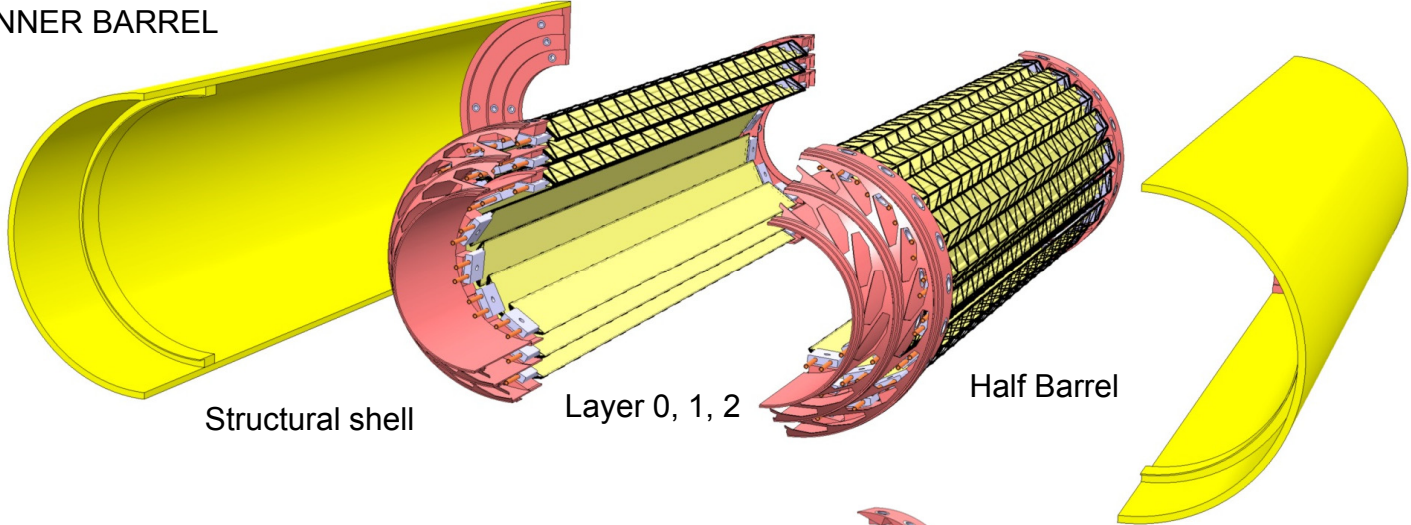
Mean  $X/X_0 = 0.282\%$



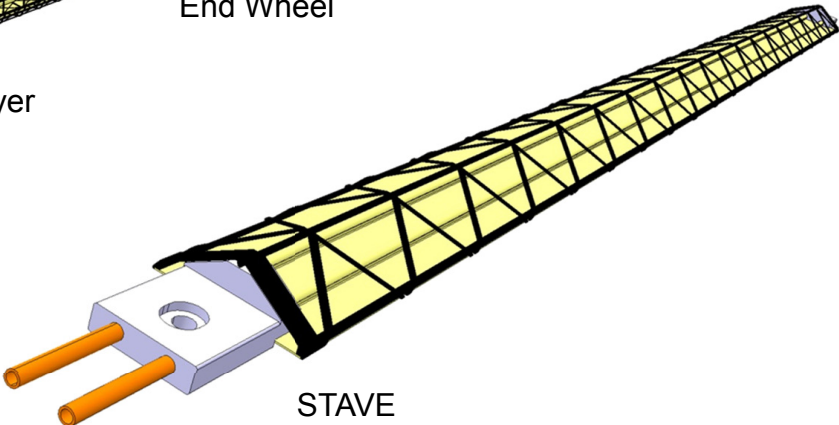
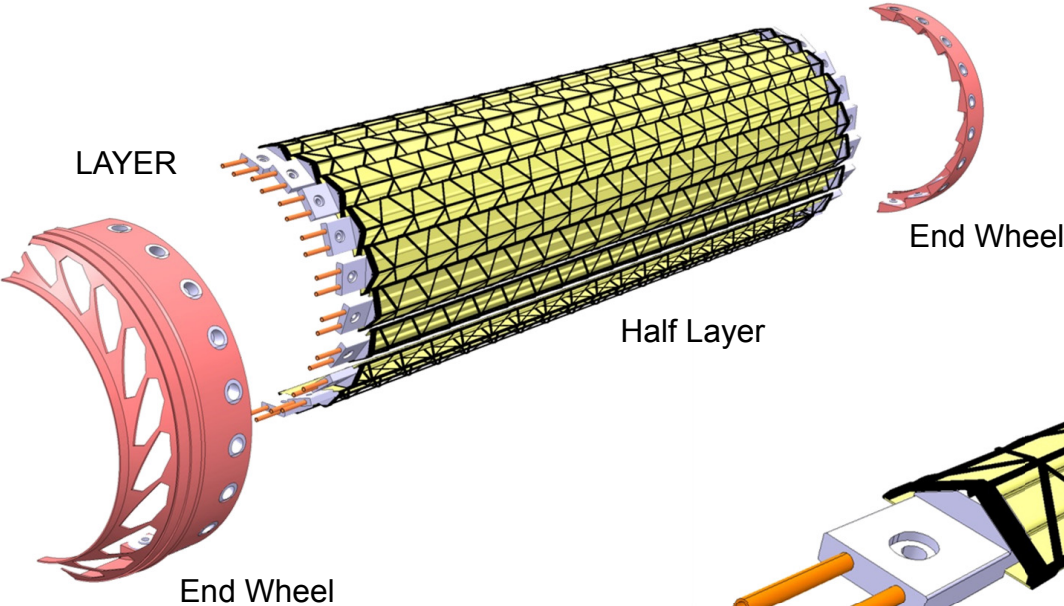
# Inner Barrel



INNER BARREL

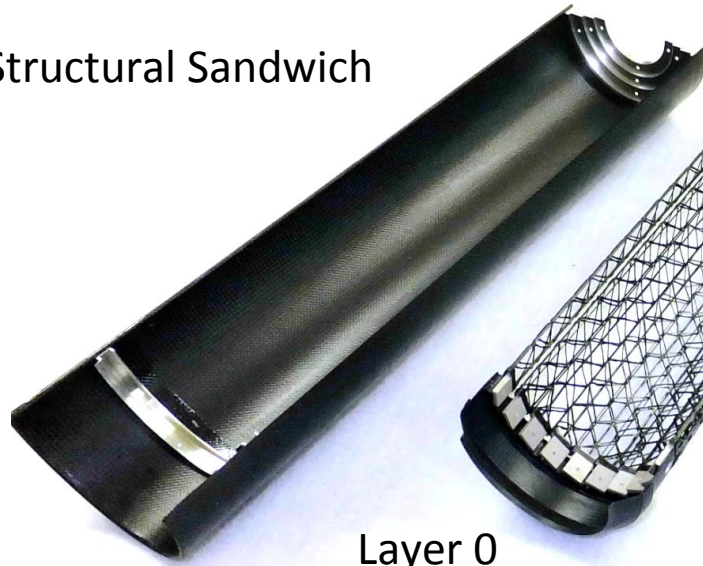


LAYER

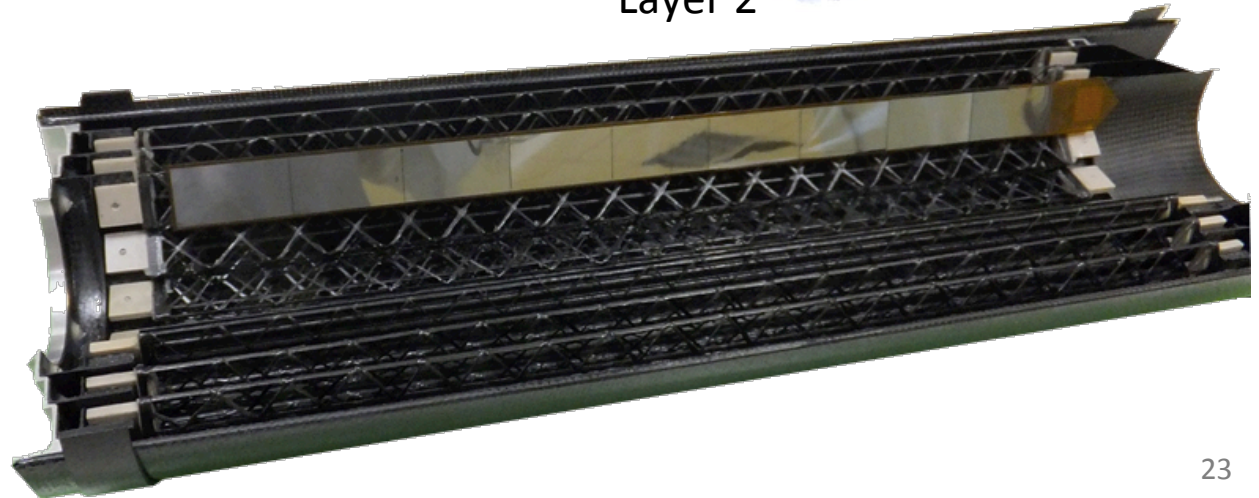


# Inner Barrel – full-scale prototype

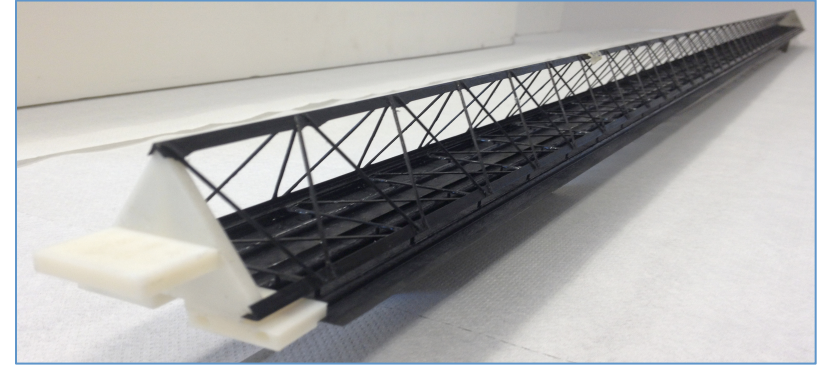
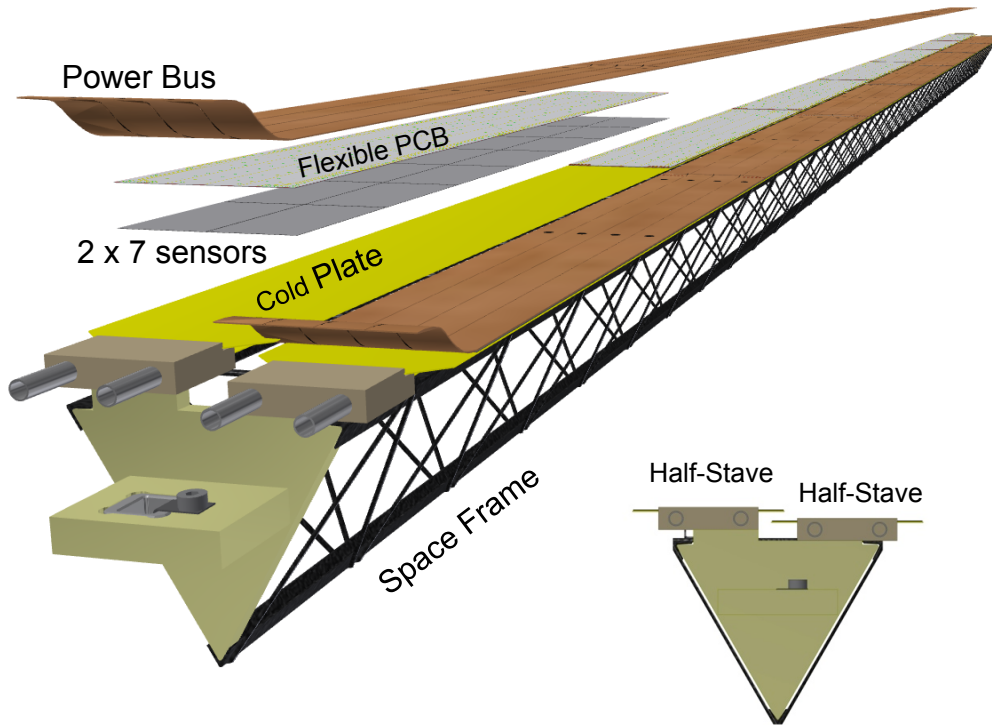
Structural Sandwich



***Prototype***



# Outer Barrel



## Outer Barrel (OB)

<radius> (mm): 194, 247, 353, 405

Nr. staves: 22, 28, 40, 46

Nr. Chips/layer: (ML), (OL)

Power density < 100 mW / cm<sup>2</sup>

Length (mm): 843 (ML), 1475 (OL)

Nr. modules/stave: 4 (ML), 7 (OL)

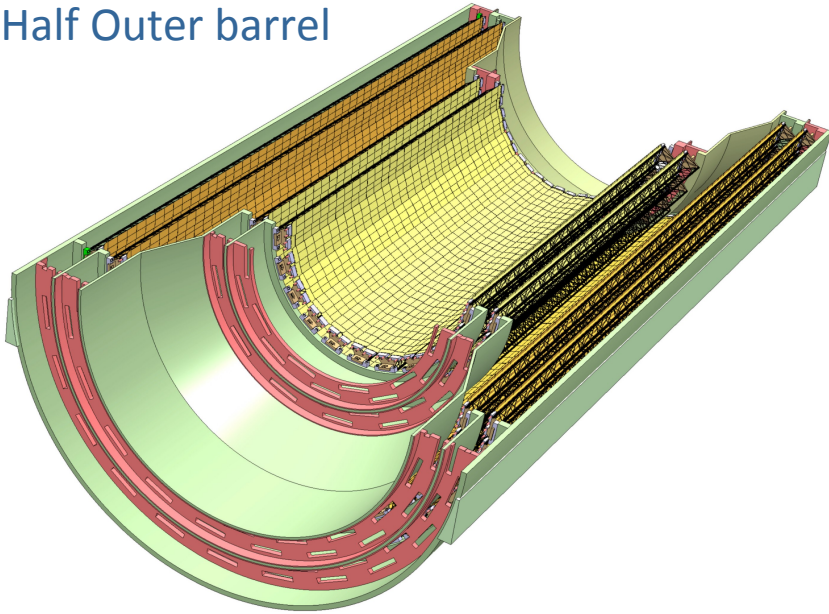
Material thickness: ~ 1% X<sub>0</sub>

Throughput (@100kHz): < 3Mb/s × cm<sup>-2</sup>

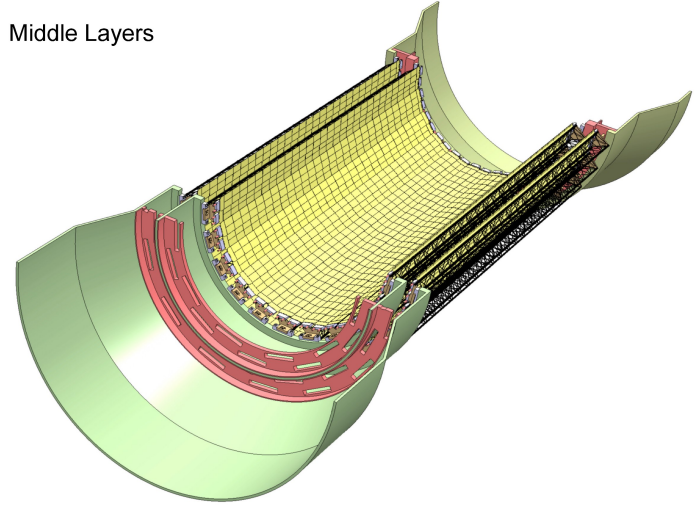


# Outer Barrel Support Structure and Assembly

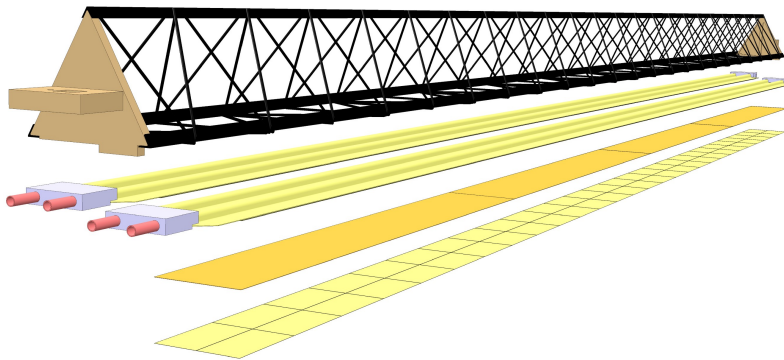
Assembly  
Half Outer barrel



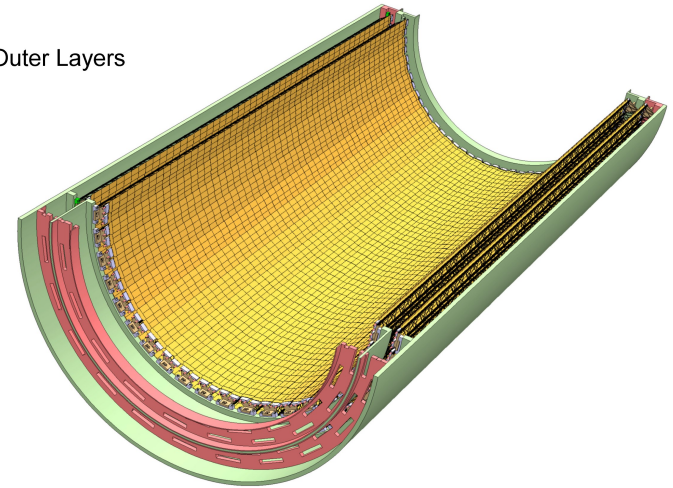
Middle Layers

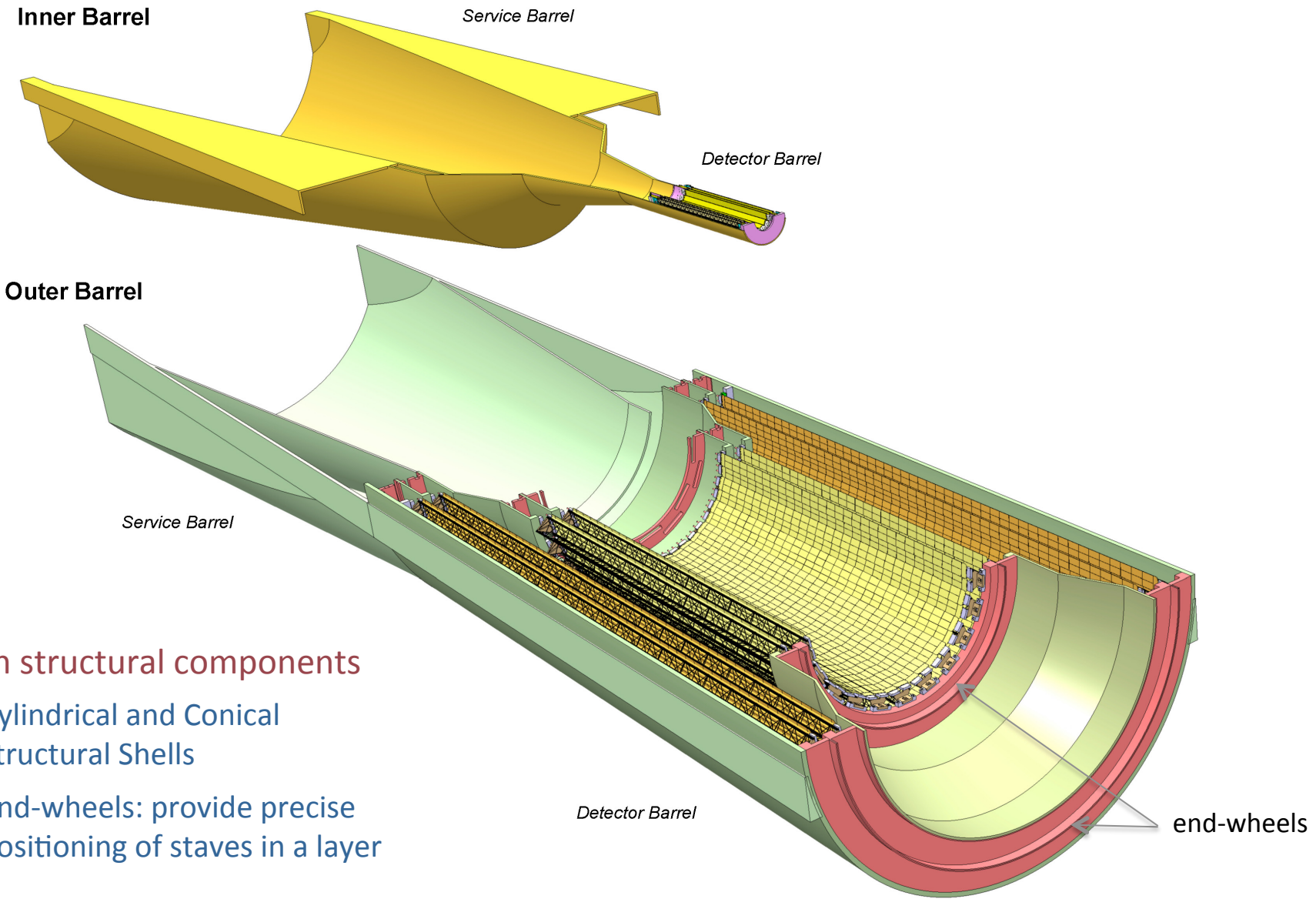


Stave



Outer Layers



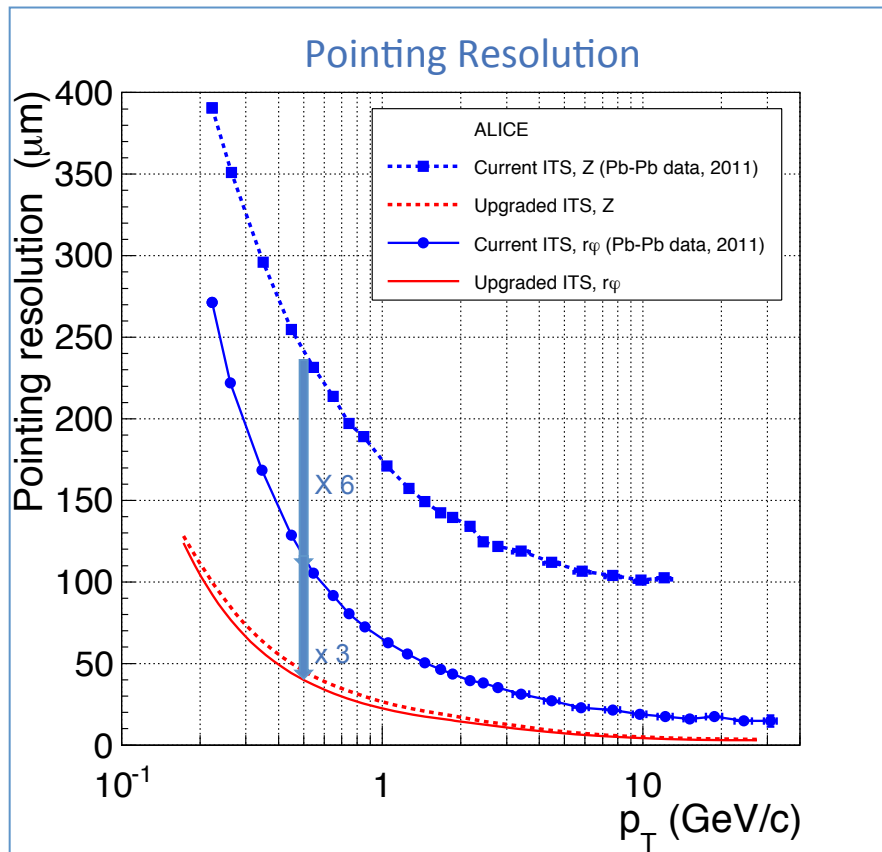


### Main structural components

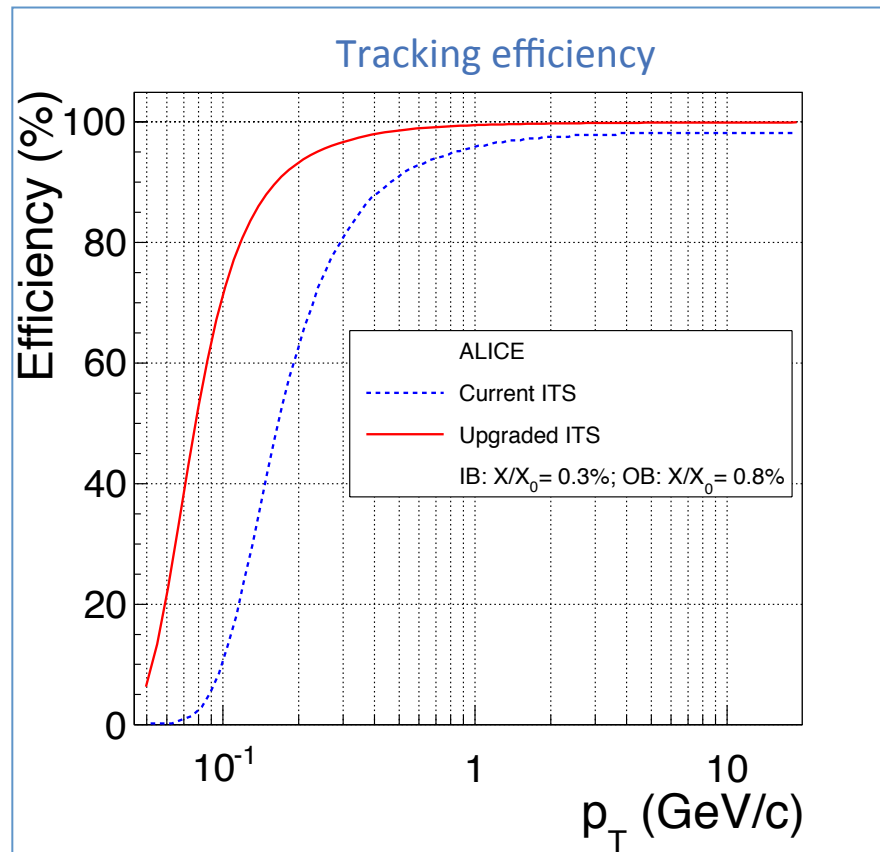
- Cylindrical and Conical Structural Shells
- End-wheels: provide precise positioning of staves in a layer

# Performance of new ITS (MC simulations)

## Impact parameter resolution

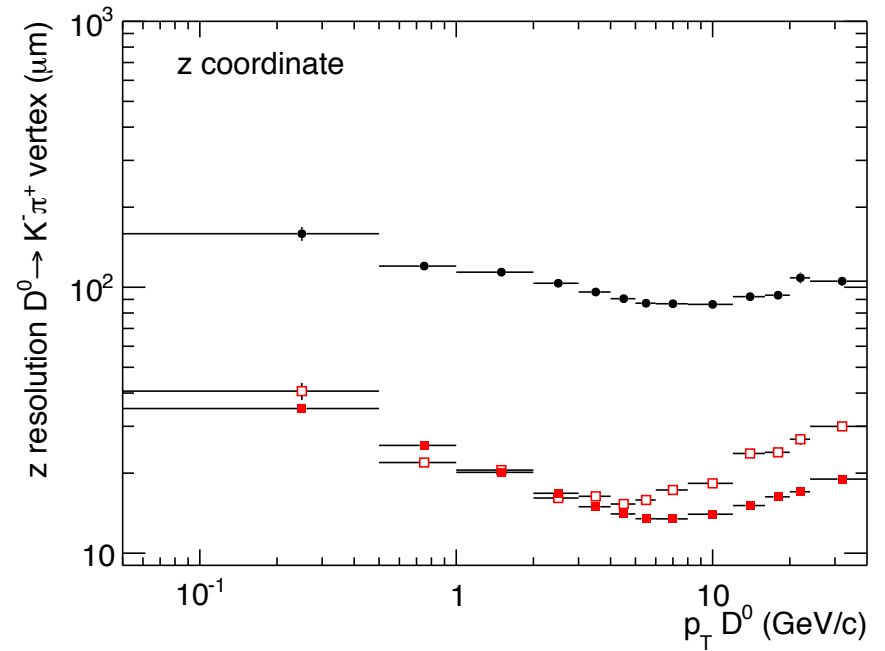
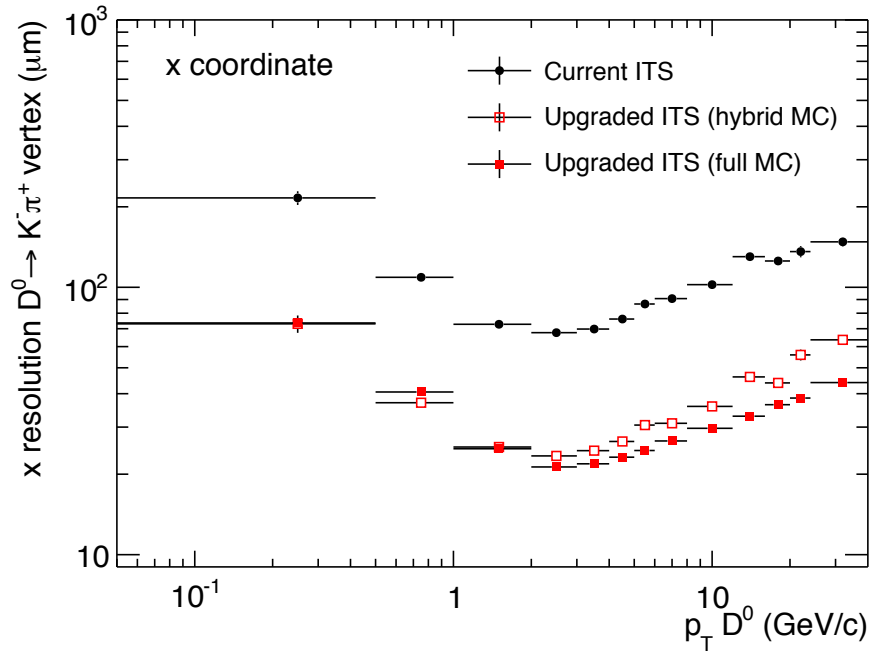


## Tracking efficiency (ITS standalone)



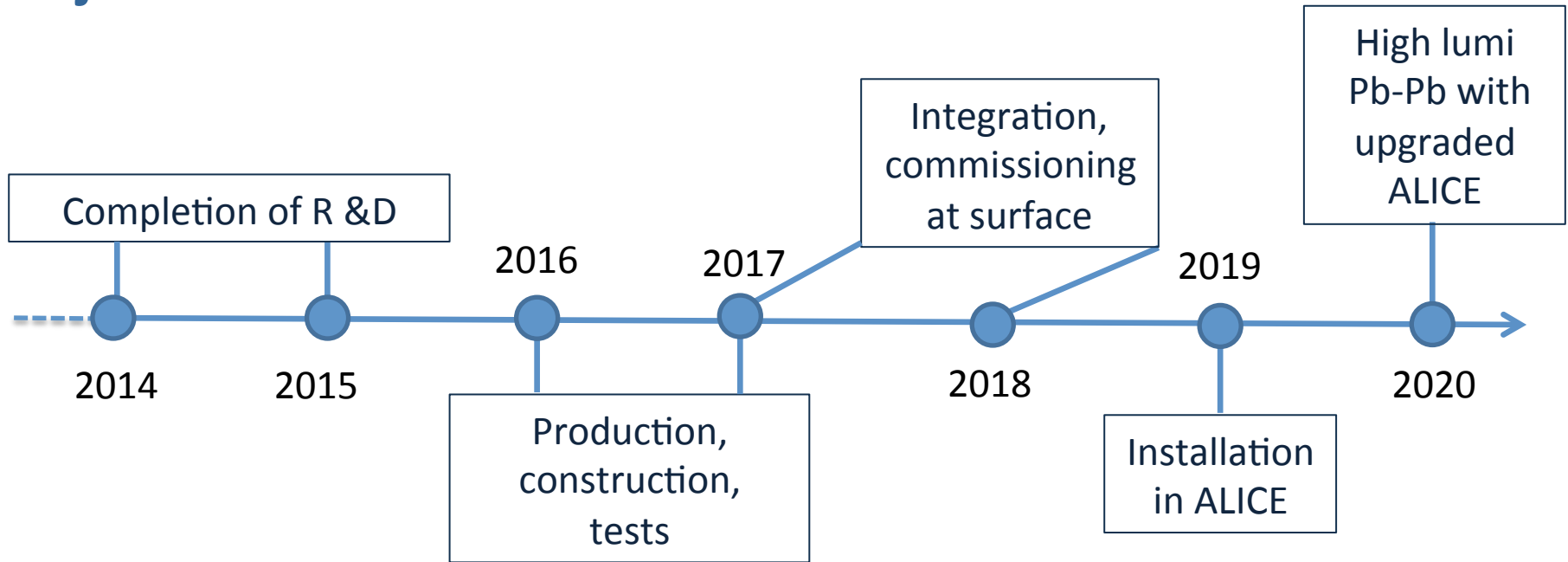
$\sim 40 \mu\text{m}$  at  $p_T = 500 \text{ MeV}/c$

## $D^0 \rightarrow K^- \pi^+$ secondary vertex position resolution



*J. Phys. G (41) 087002*

# Project Timeline and Collaboration



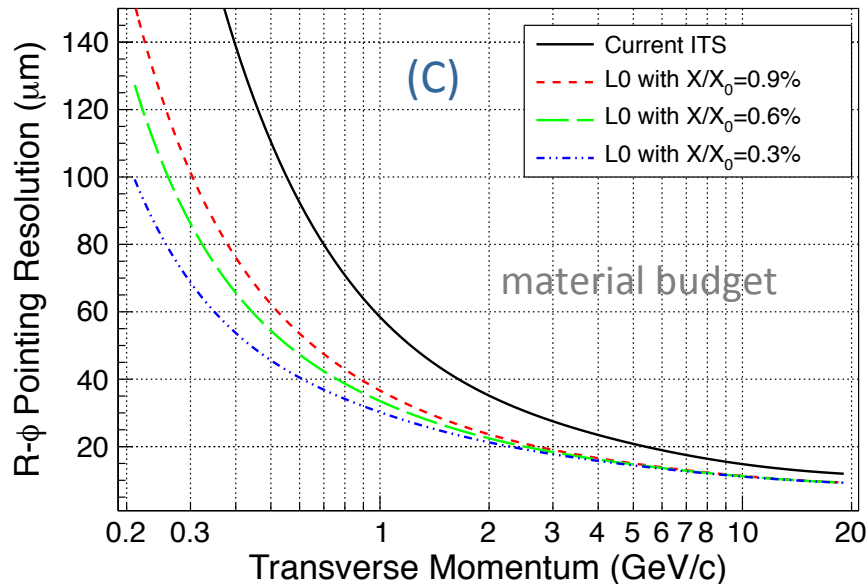
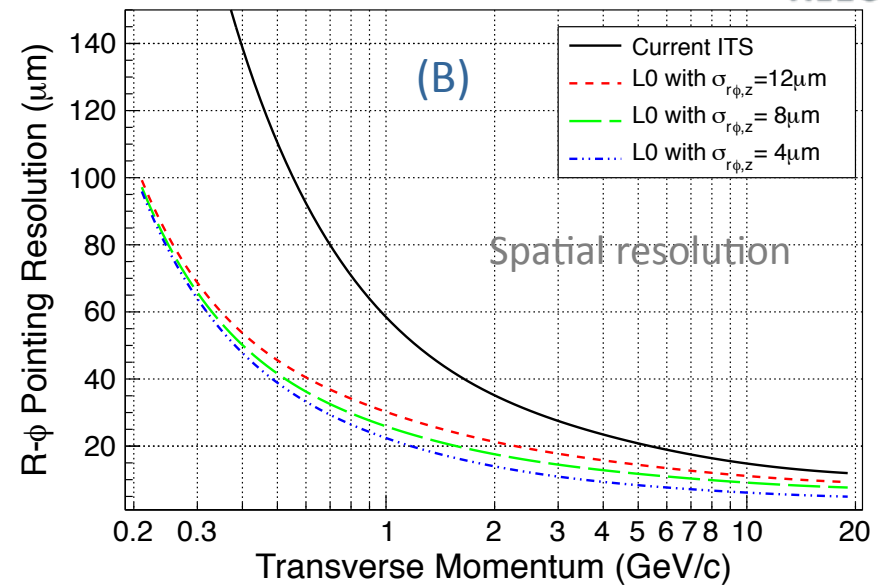
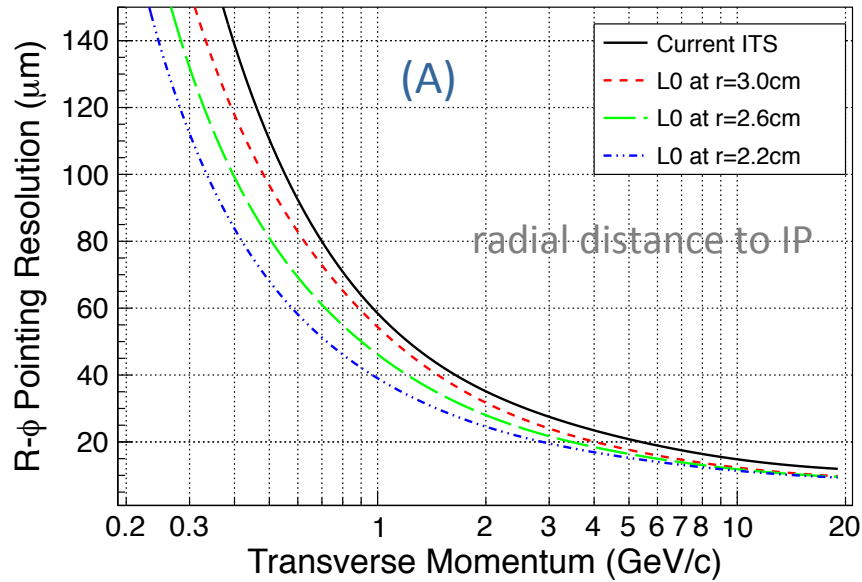
## ALICE ITS Collaboration

CERN, **China** (Wuhan), **Check Republic** (Prague), **France** (Grenoble, Strasbourg), **Italy** (Aless., Bari, Cagliari, Catania, Frascati, Padova, Roma, Trieste, Torino), **Indonesia** (LIPI), **Korea** (Pusan, Inha, Yonsei), **Netherlands** (Nikhef, Utrecht), **Pakistan** (CIIT-Islamabad), **Russia** (St. Petersburg), **Slovakia** (Kosice), **Thailand** (Suranaree, SLRI, TMEC), **UK** (Daresbury, Liverpool, RAL), **Ukraine** (Kharkov), **USA** (Austin, Berkeley)

Institute = participated in current ITS

SPARES

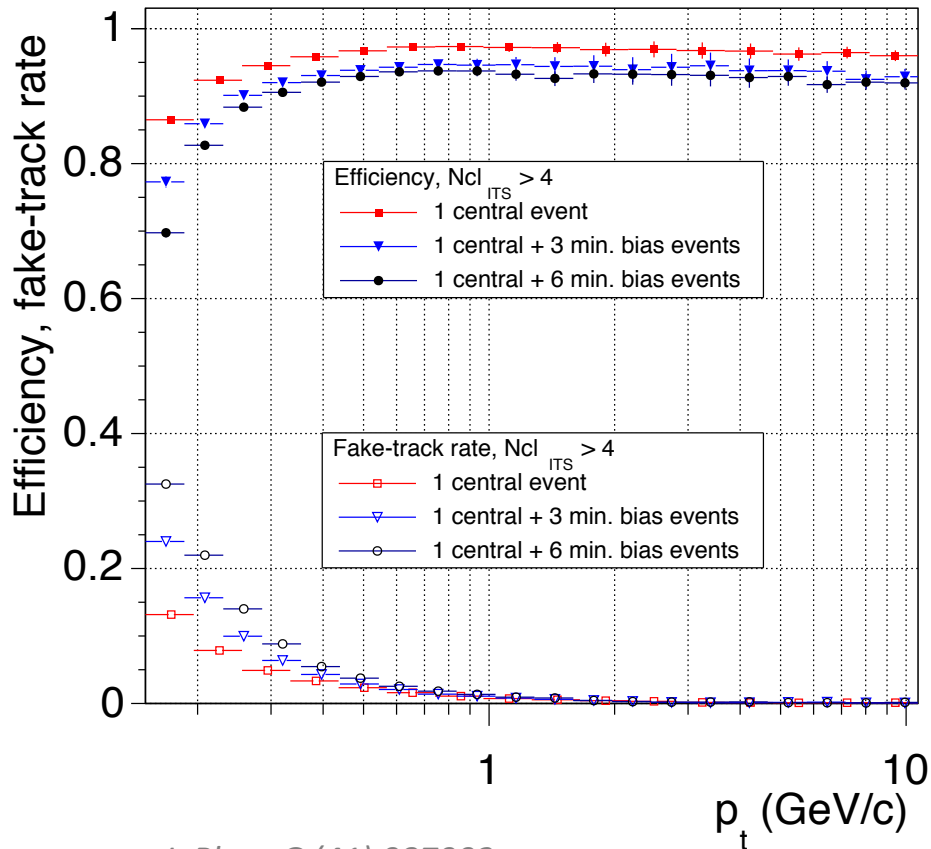
# Impact parameter studies (ALICE ITS Upgrade)



- Current ALICE ITS
  - ✧ radial position of first layer: 39mm
  - ✧  $x/X_0$ : 1.14% per layer
  - ✧ spatial resolution (r-phi): 12  $\mu\text{m}$
- A) current ITS + L0:  $x/X_0 = 0.3\%$ , res.=4 $\mu\text{m}$ ;
- B) current ITS + L0:  $r = 22\text{mm}$ ,  $x/X_0 = 0.3\%$ ;
- C) current ITS + L0:  $r = 22\text{mm}$ ,  $x/X_0 = 0.3\%$ ;

ALICE ITS Upgrade CDR, CERN-LHCC-2012-12

Matching efficiency between the tracks reconstructed in the upgraded ITS and TPC for different values of event pile-up



*J. Phys. G (41) 087002*

The average event pile-up depends on the interaction rate and detector integration time

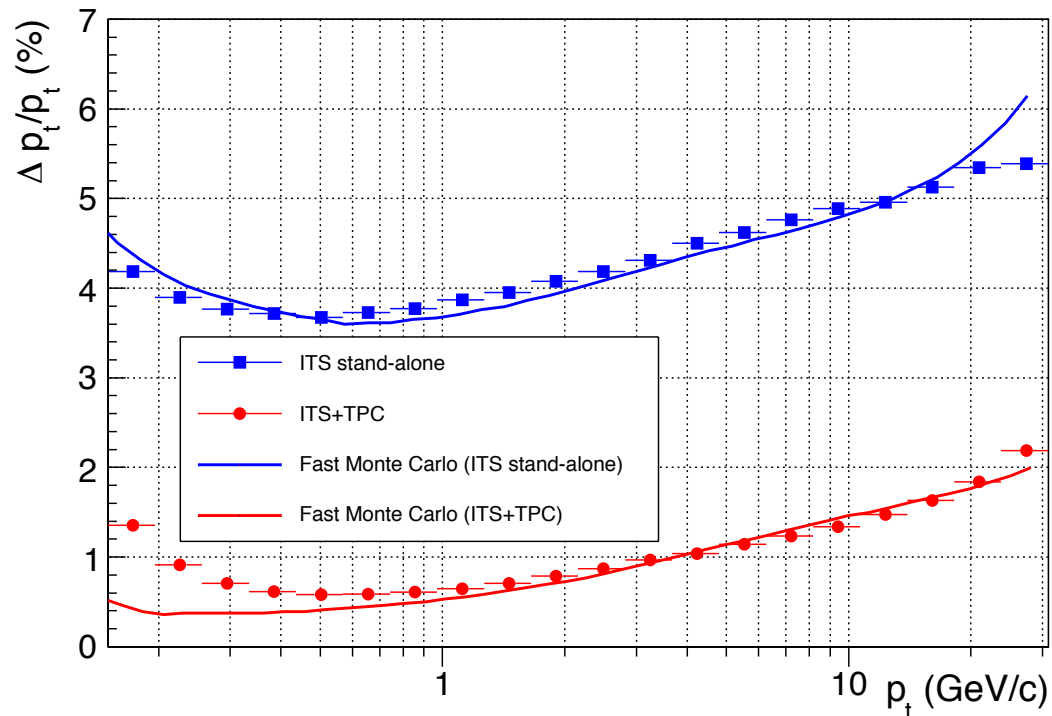
interaction rate 50 kHz  
integration time: 4 – 30  $\mu$ s

For 30  $\mu$ s integration time (worst case design):

$\langle \text{pile-up} \rangle = 1 \text{ central} + 1.5 \text{ min. bias}$



## MOMENTUM RESOLUTION

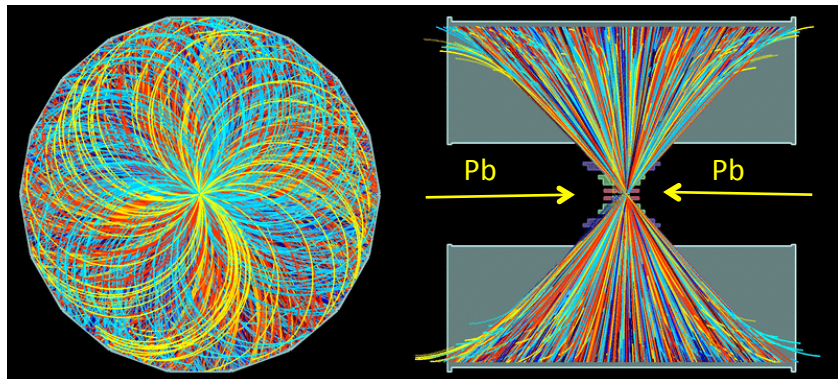


*J. Phys. G (41) 087002*

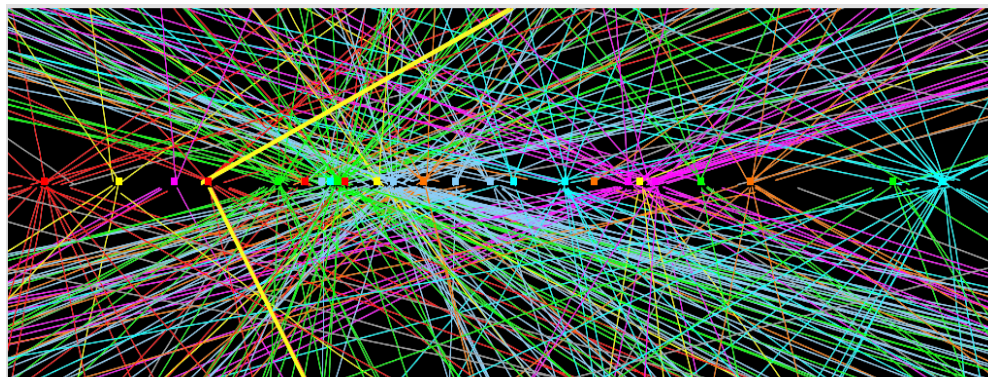
Transverse momentum resolution as function of  $p_T$  for primary charged pions for the upgraded ITS and current ITS. The results are shown for ITS standalone and ITS-TPC combined tracking.

# Why use Silicon Pixels in HEP experiments

Silicon Pixel Detectors are high granularity detectors, which provide unambiguous and precise hit information in a harsh environment close to the interaction point



LHC Pb-Pb collision (ALICE, Sep 2011)

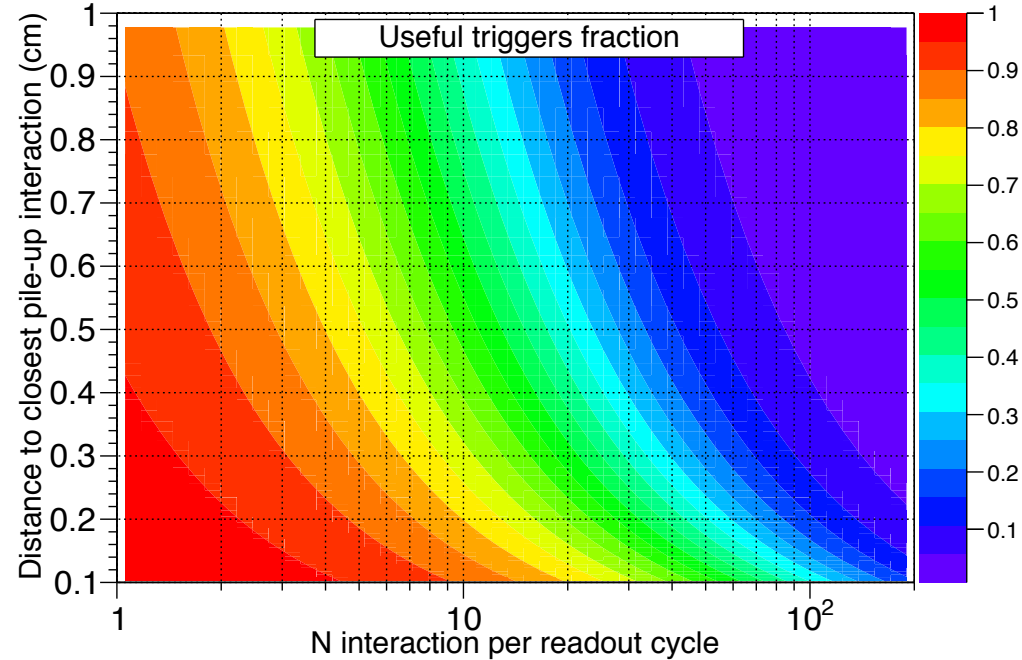
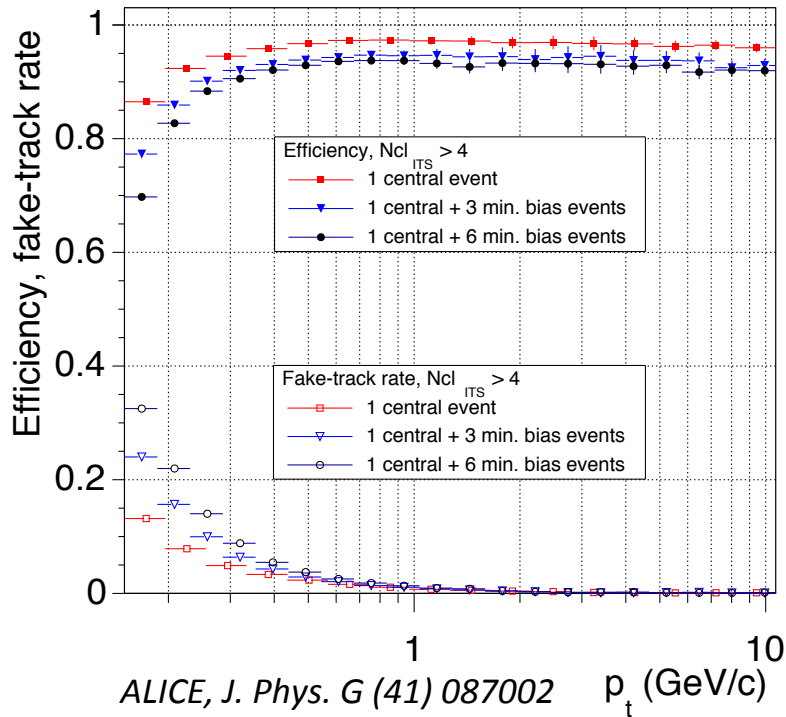


LHC pp collisions: a candidate Z boson event in the dimuon decay with 25 reconstructed vertices. (ATLAS, April 2012)

- Position resolution down to few microns
- Unambiguous hit information in high track density region
- **High resolution** for determination primary and secondary vertex
- **Fast readout**
- High level of **radiation hardness**

# How integration time and pile-up affect performance

## ALICE ITS Upgrade



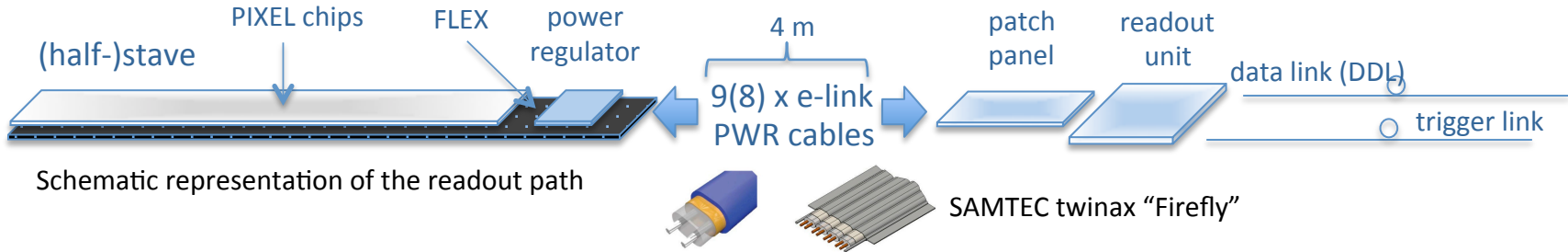
At 50 kHz Pb-Pb interaction rate

$\langle \text{pile-up} \rangle$  @ 20  $\mu\text{s}$  integration time: 1 central + 1 minimum bias

At 200 kHz pp interaction rate

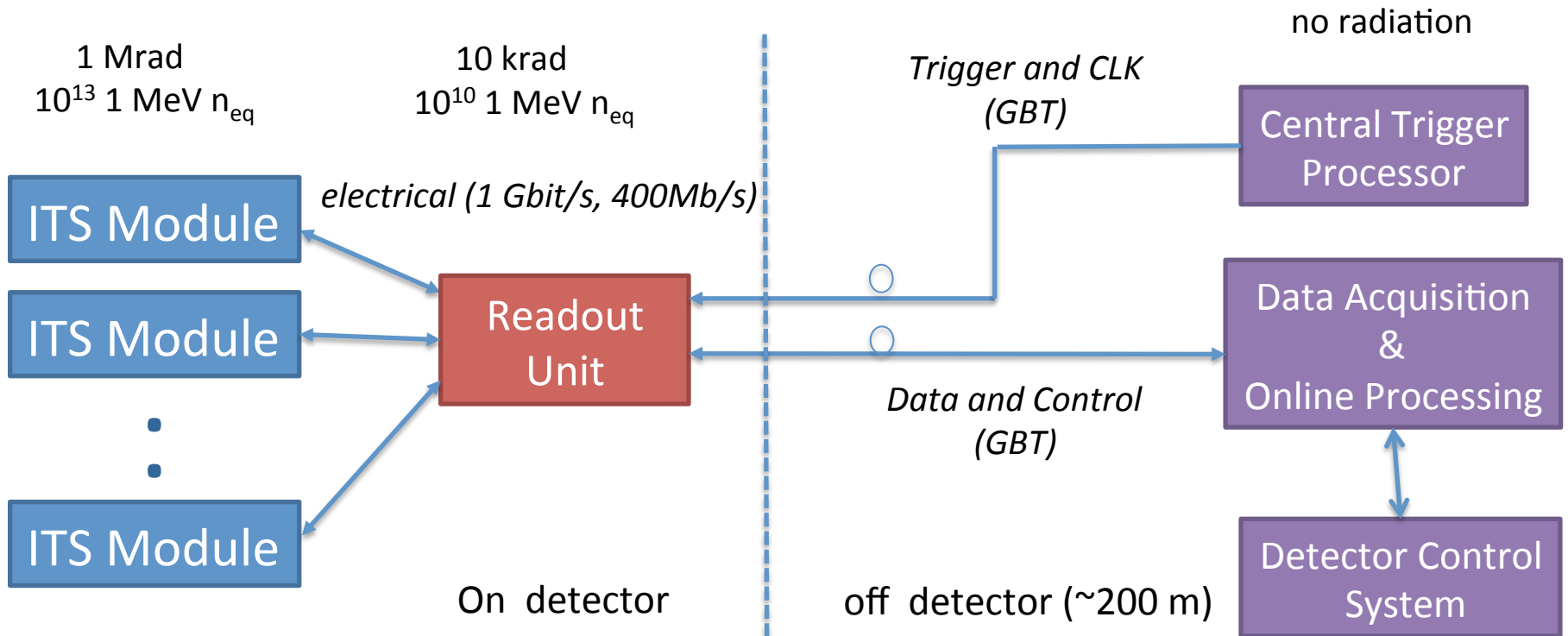
$\langle \text{pile-up} \rangle$  @ 20  $\mu\text{s}$  integration time: 5 interaction

# Readout – general scheme and data throughput



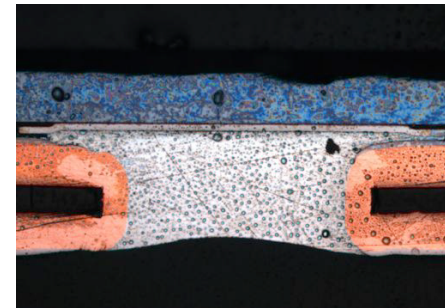
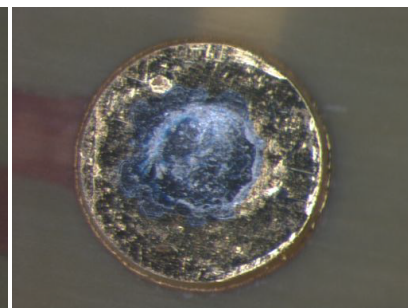
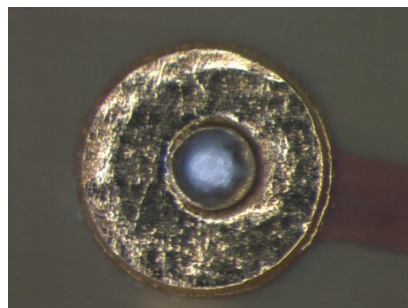
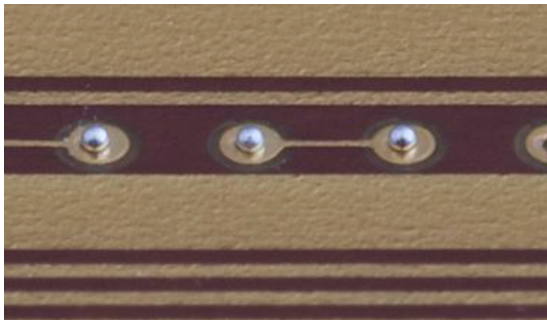
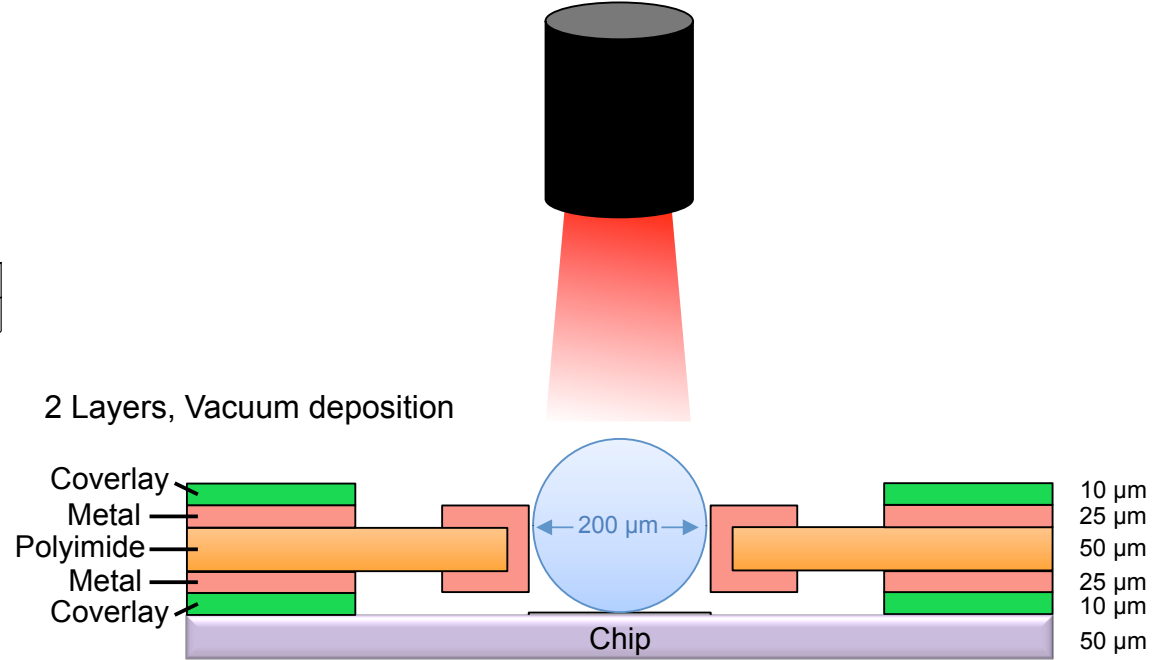
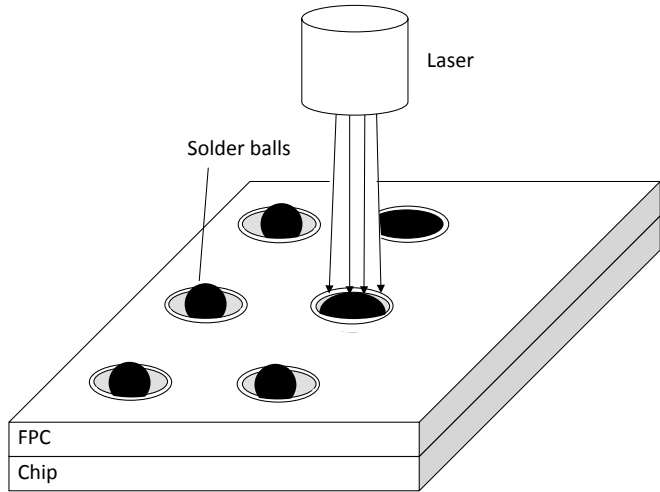
Data throughput 324 Gbit/s  
1008 electrical links

(184 DAQ optical links + n Trigger links)



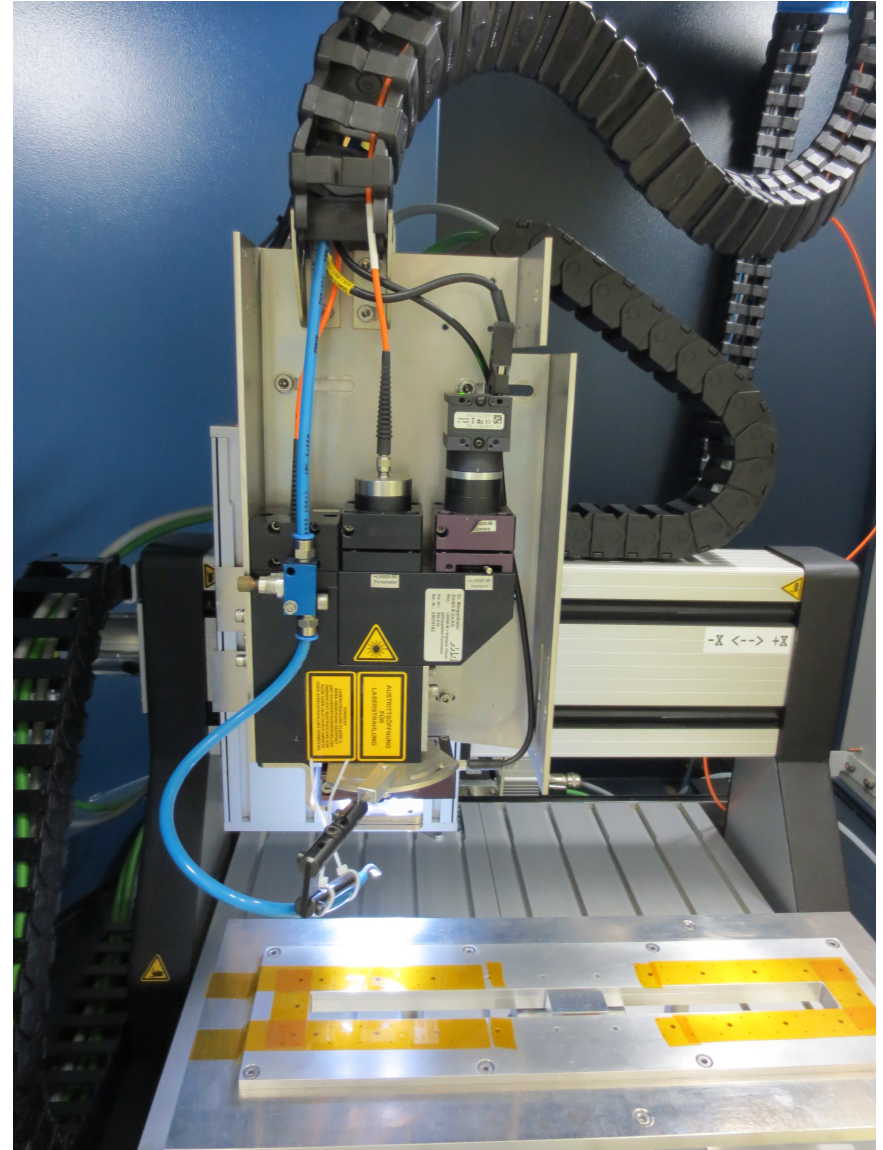
# Chip Assembly – laser soldering

Interconnection of Pixel chip on flexible printed circuit  
Laser soldering (baseline)



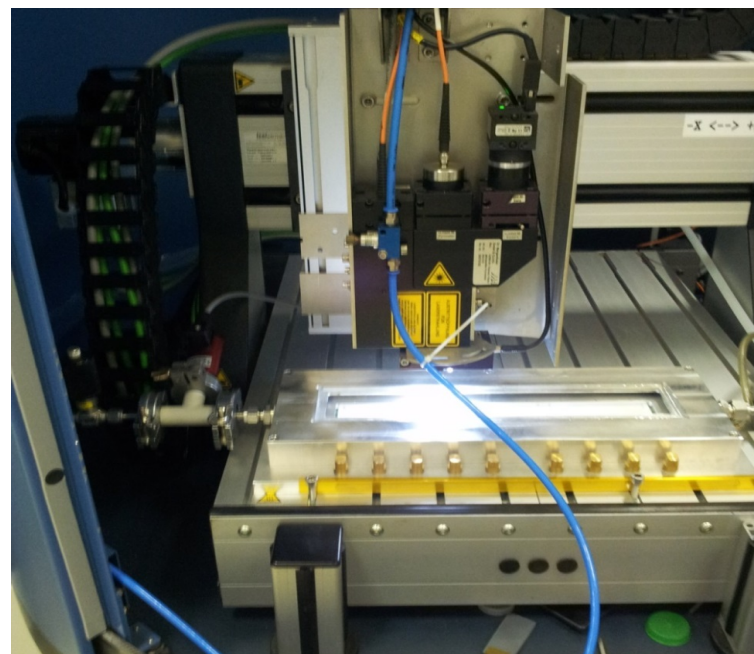
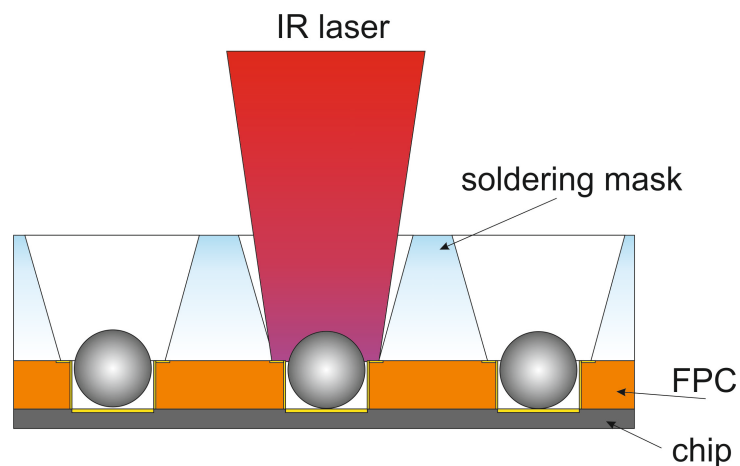
# Chip Assembly – laser soldering

Laser soldering machine (Dr. Mergenthaler GMBH)  
put in service at the CERN ITS Lab (Sep 2013)



## Selective laser soldering

- Interconnection between FPC and chip by flux-less laser soldering of 200  $\mu\text{m}$  diameter Sn/Ag(96.5/3.5) balls (227  $^{\circ}\text{C}$  melting T) in vacuum ( $\leq 10^{-1}$  mbar)
- IR diode laser, 976 nm, 25 W, 50 mm focal length, 250  $\mu\text{m}$  beam spot size
- Laser power modulated by pyrometer, programmable T profile ensures precise limitation of heating
- Soldering mask (in Macor<sup>®</sup> or Rubalit<sup>®</sup>) used to push FPC on chip and guide soldering balls inside FPC vias

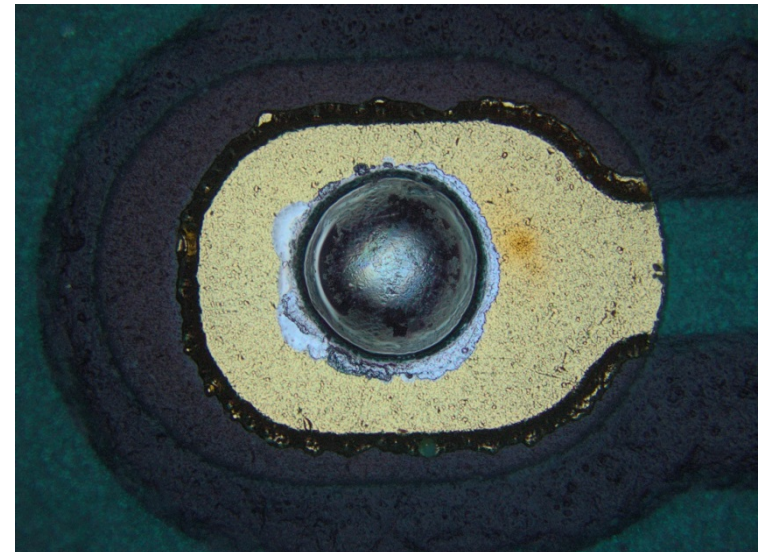
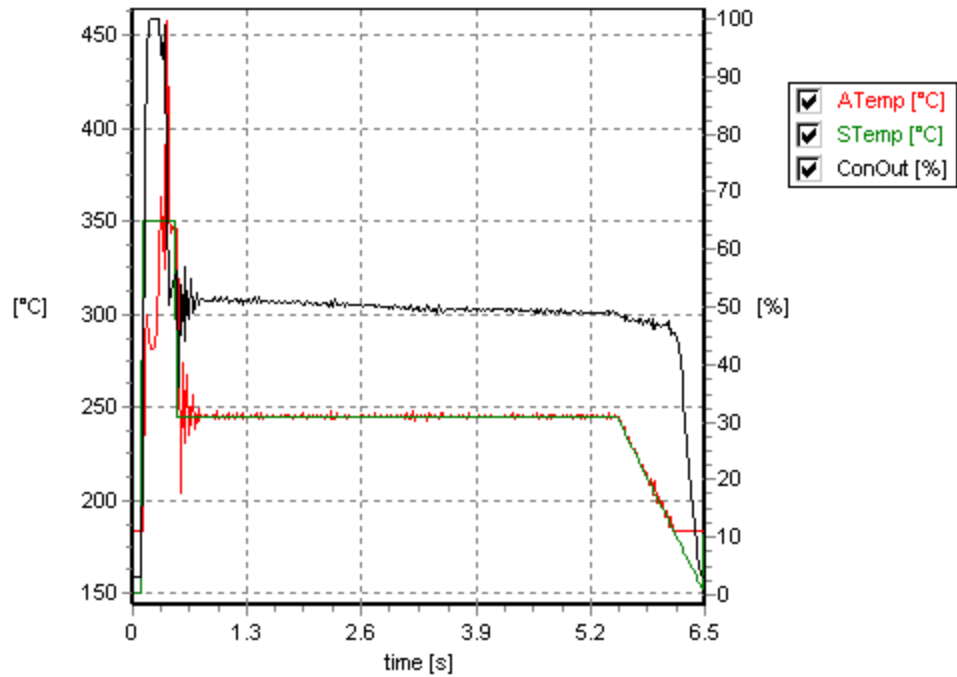


## Good soldering

192.168.0.10: process: 10533 workpiece code: 06102014-SA1

07.10.2014 11:00:38, duration: 6.500 s

PI: 320.01 %s, script: 181, errors: -



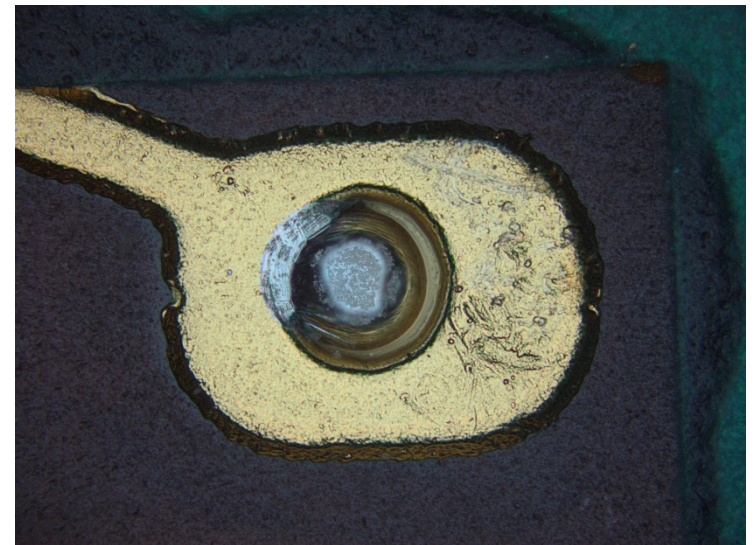
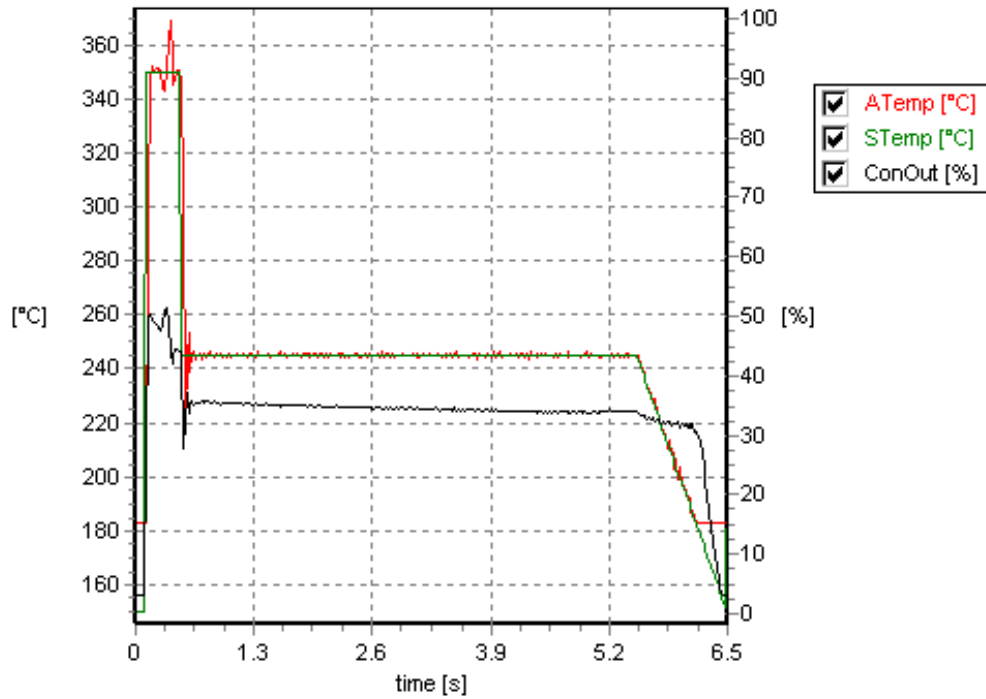


## Bad soldering

192.168.0.10: process: 10532 workpiece code: 06102014-SA1

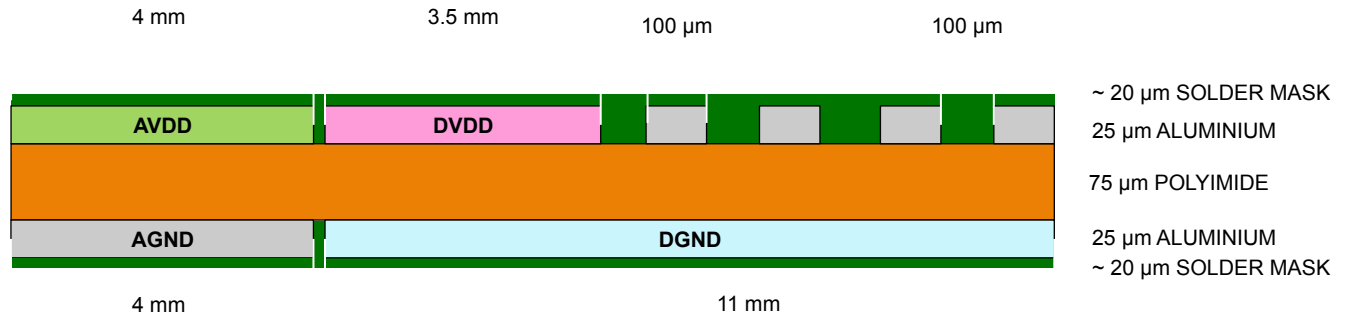
07.10.2014 10:59:08, duration: 6.500 s

PI: 217.28 %s, script: 181, errors: -

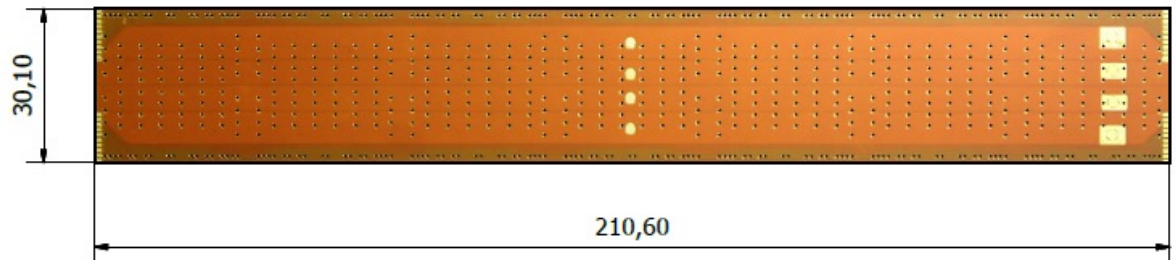
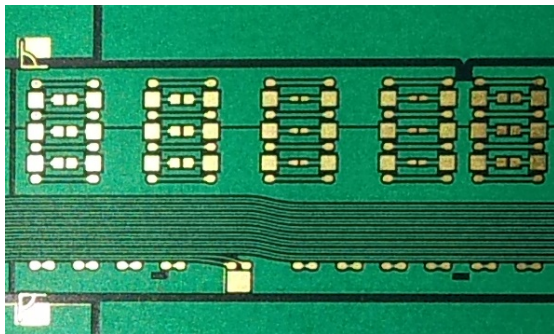
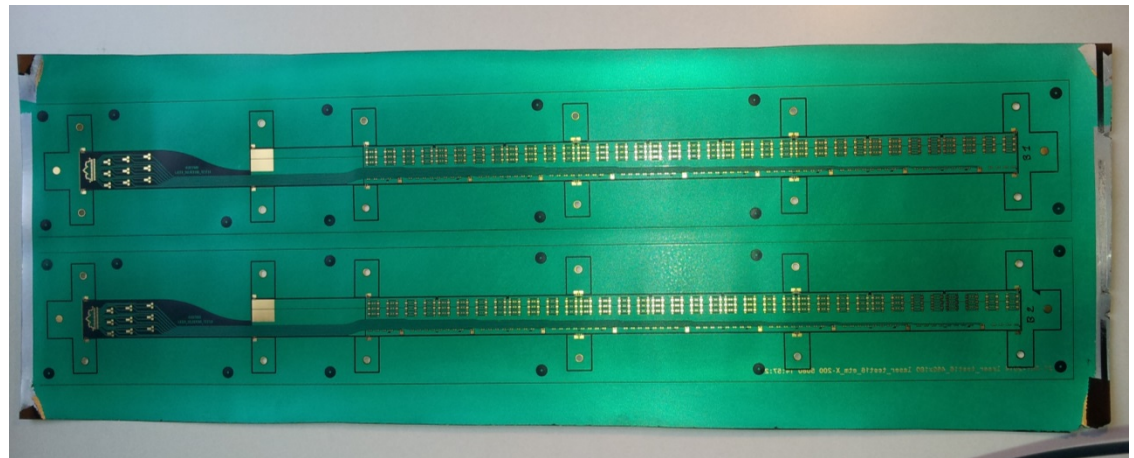


# FPC main characteristics

## Flexible Printed Circuit



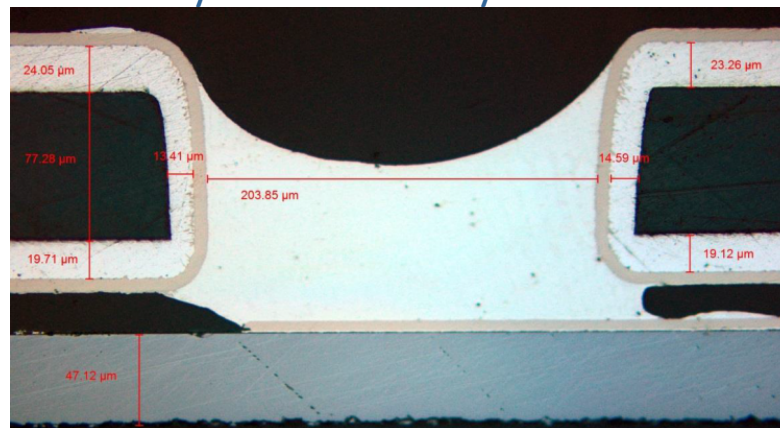
- 2 layouts:
  - IB: 1x9 chips, Al
  - OB: 2x7 chips, Cu
- Metallised vias of 220 μm diameter
- Two openings of 1x1 and 1x0.4 mm<sup>2</sup>, respectively, to “see” chip targets

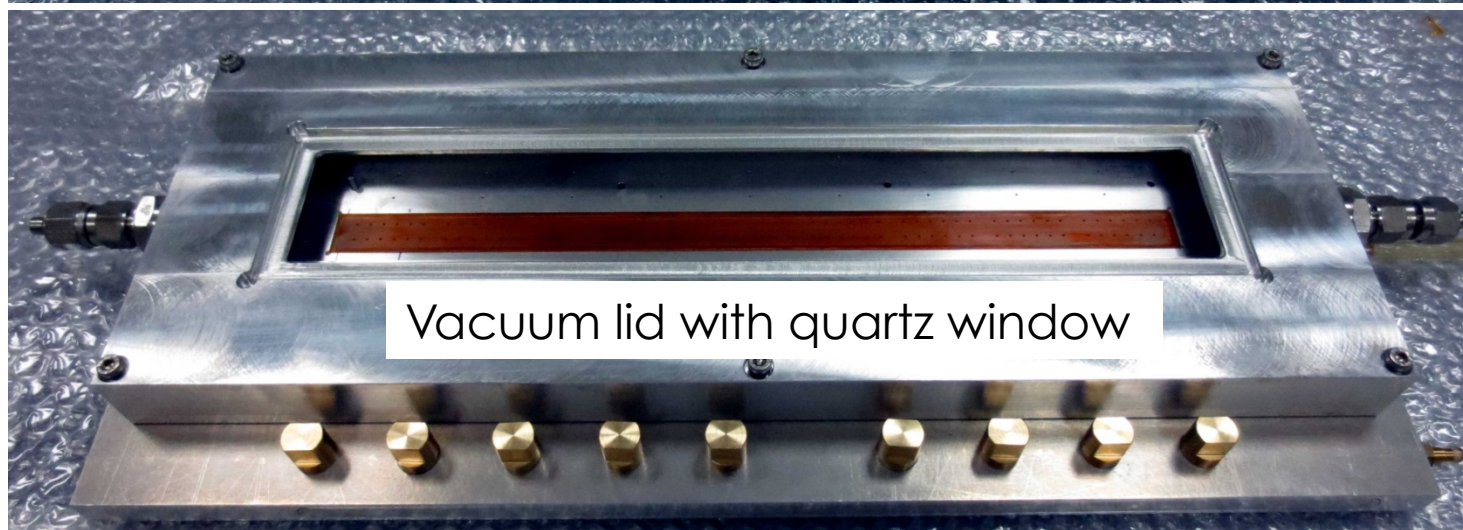
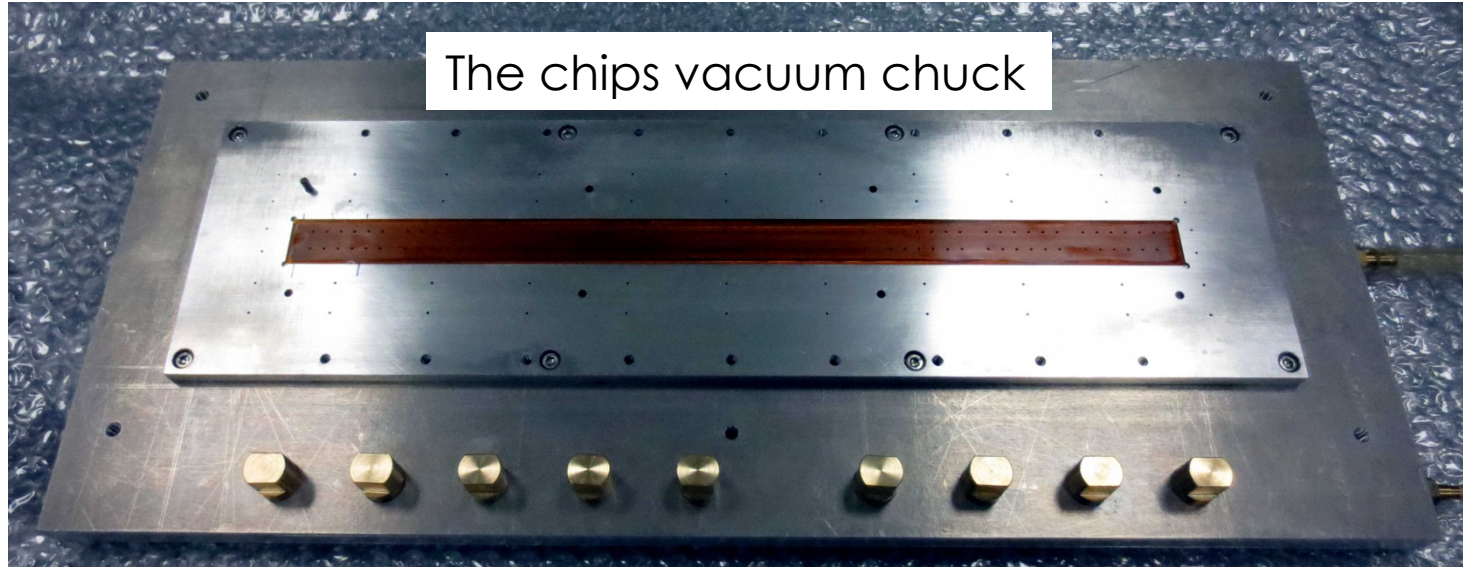


- The amount of HICs and the time available require a distributed production over many sites
- Usage of same procedure and system is necessary to ensure homogenous production
- To simplify/shorten the assembly procedure, chips are placed in nominal positions and FPC is overlapped using nominal pinholes
- Depending on FPC hole position accuracy, possibility of mismatch, i.e. hole is not fully contained in a pad

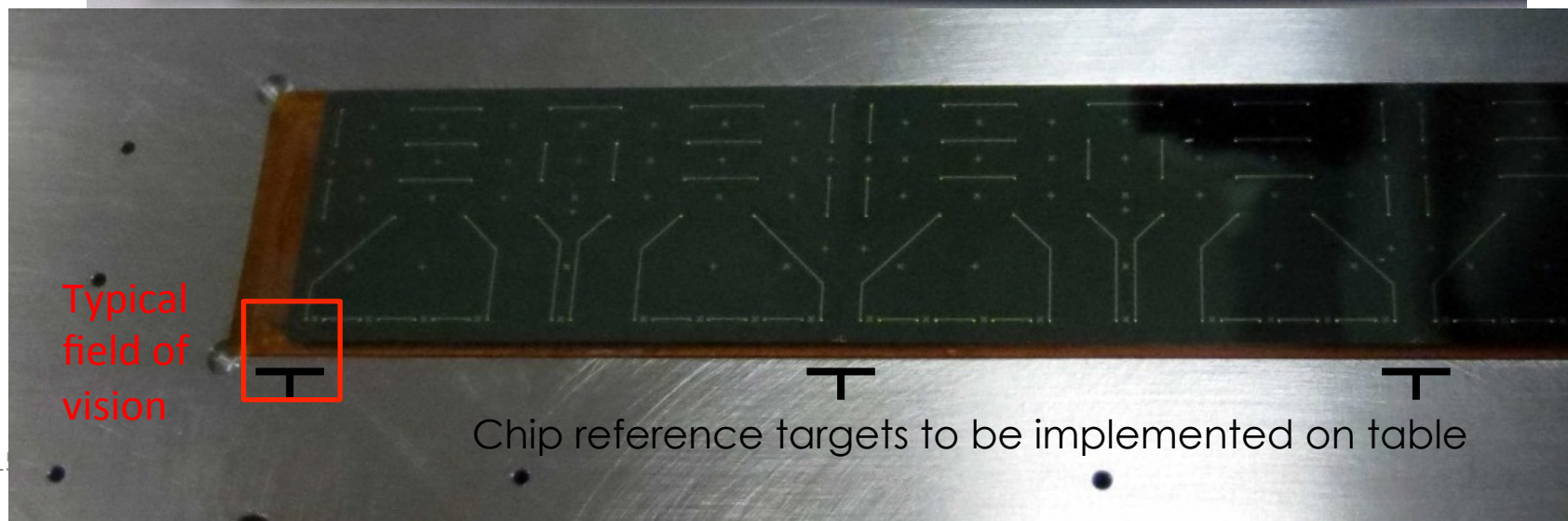
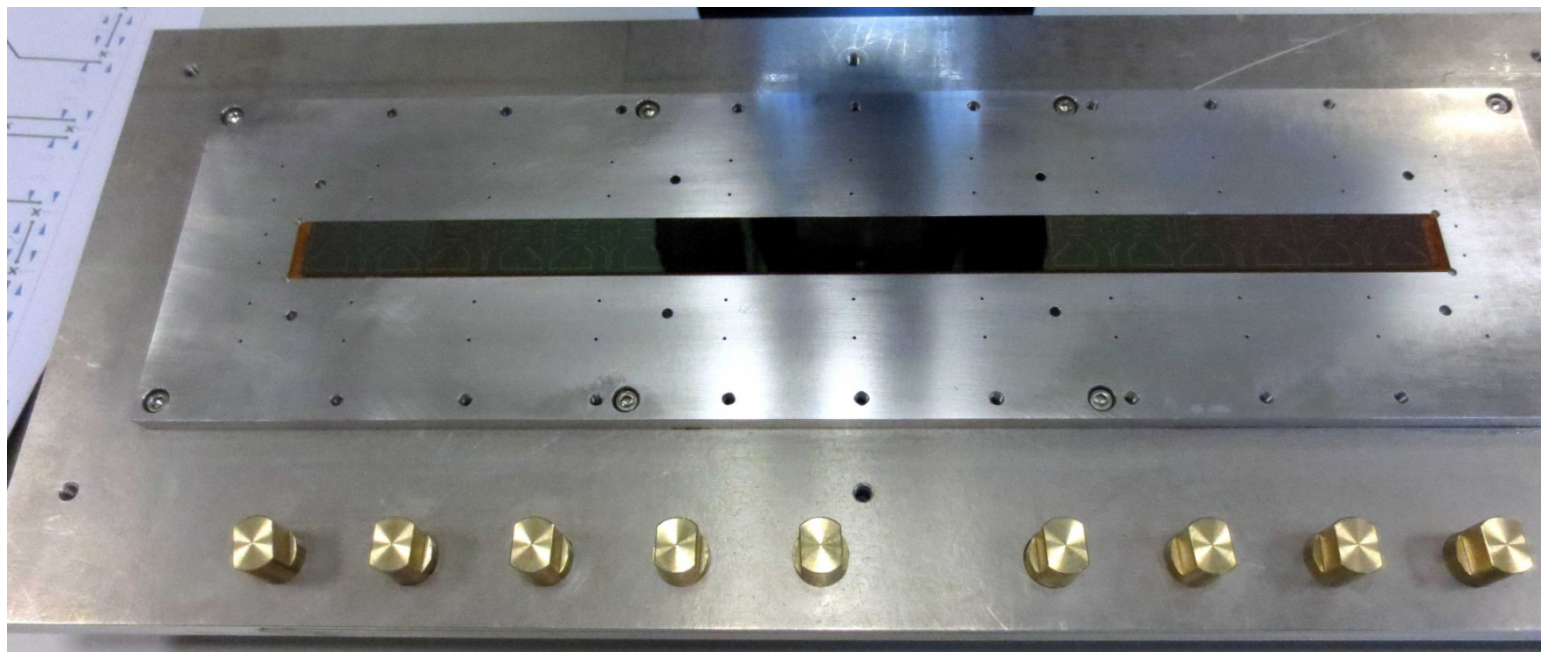


- A few soldering tests with misaligned (up to 20 mm) pads have been performed: not conclusive, need more systematic study





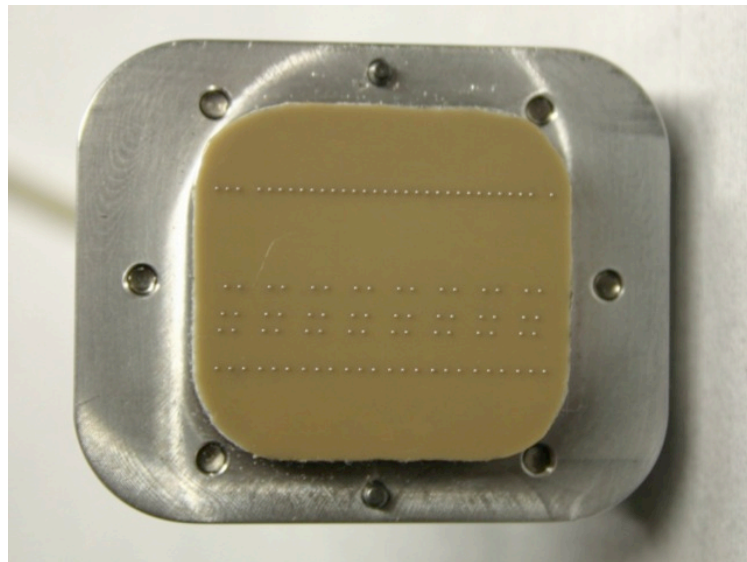
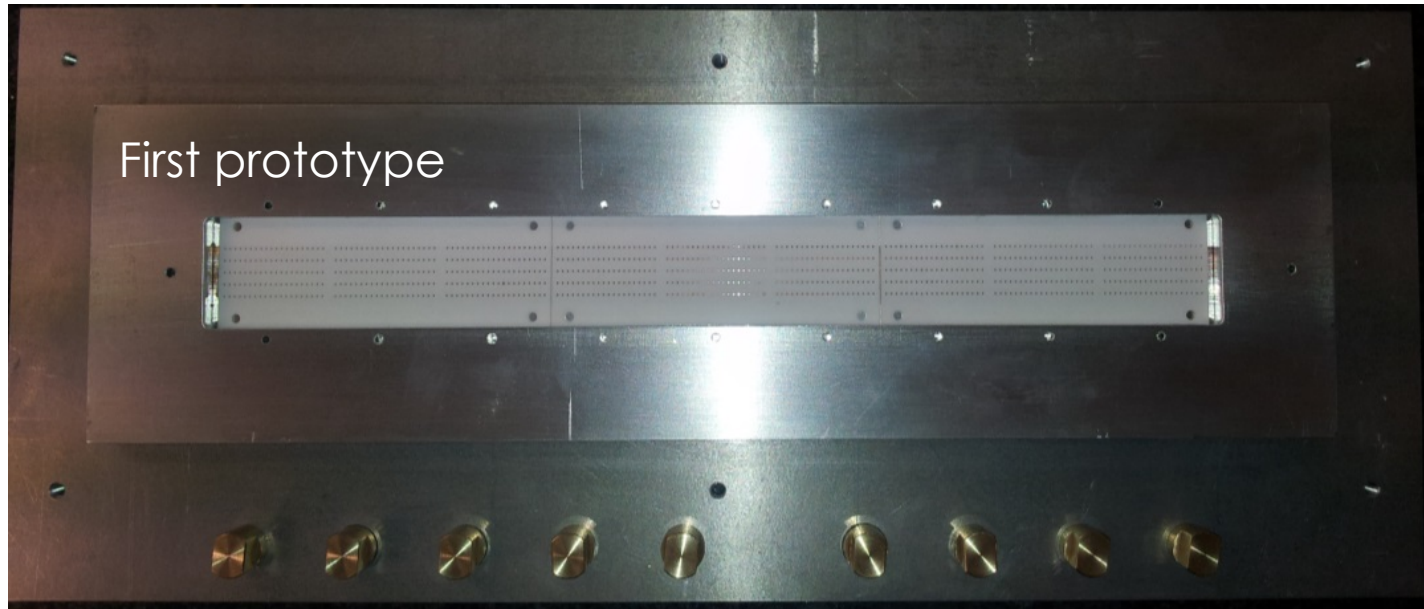
# HIC assembly - aligned pad chips



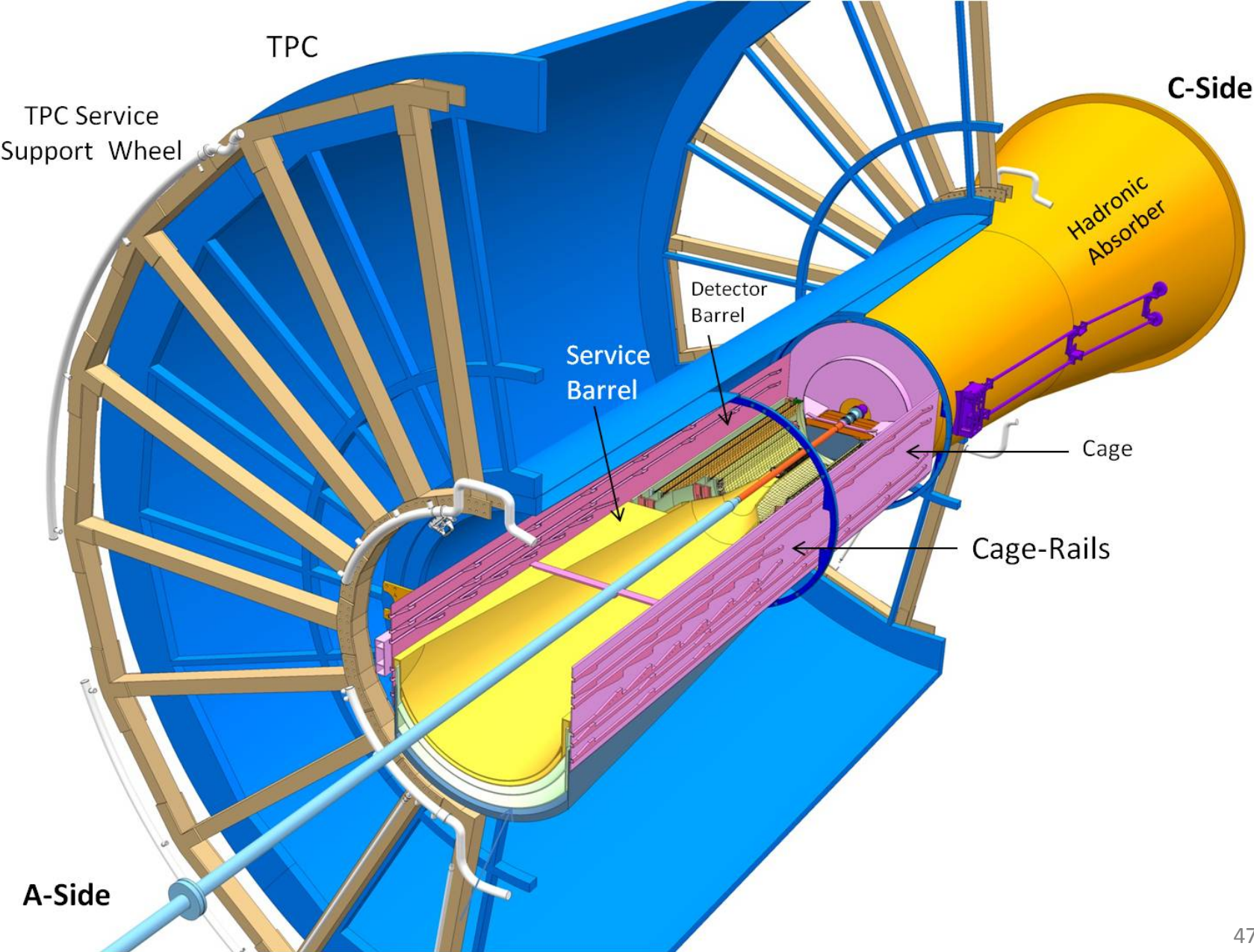
Typical  
field of  
vision

Chip reference targets to be implemented on table

# The soldering mask and ball transfer tool

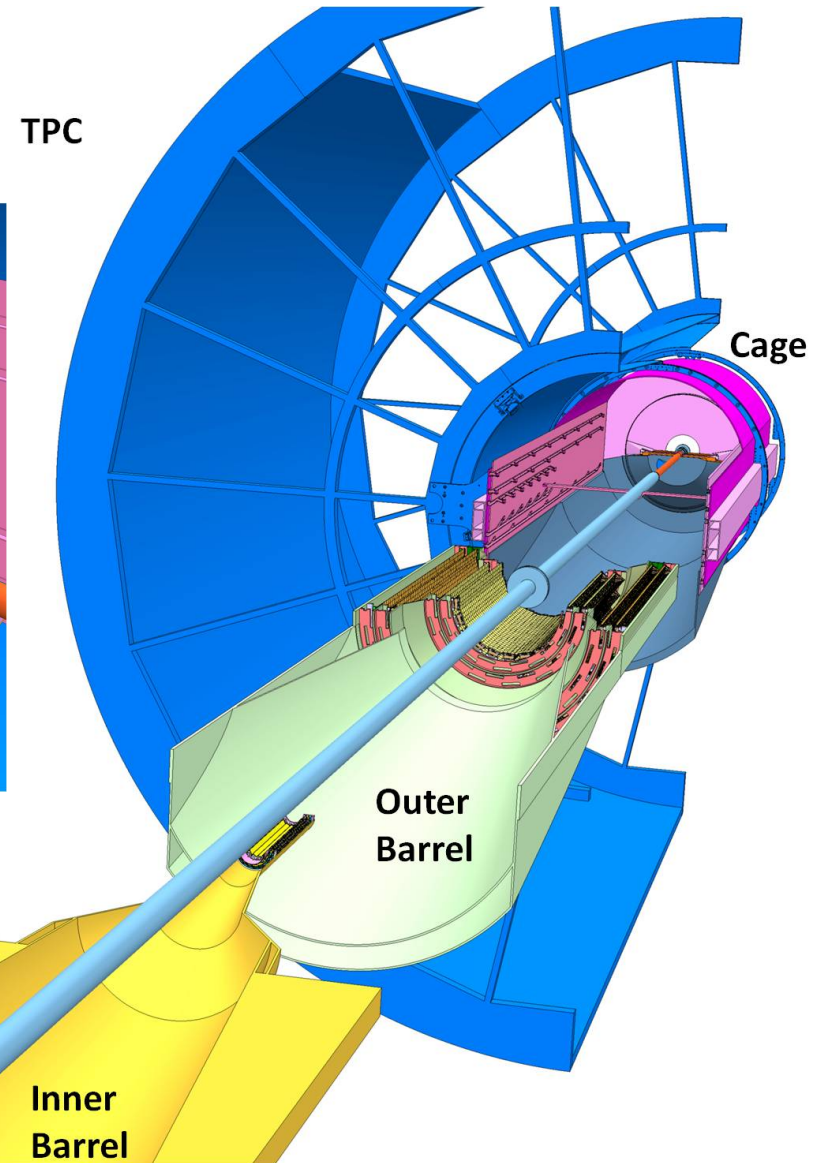
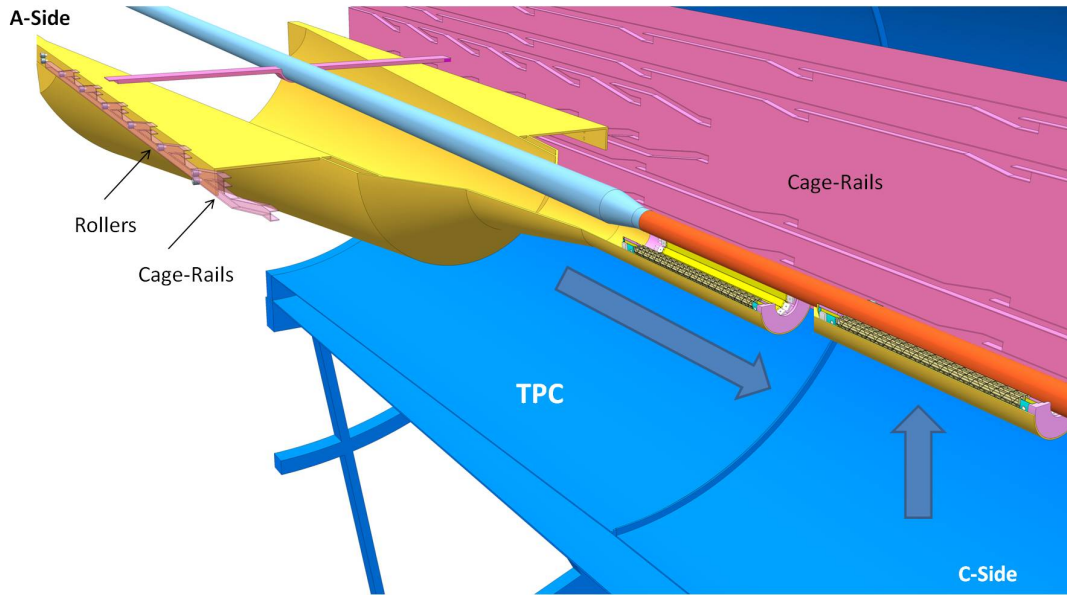


# Mechanical Integration



# Mechanical Integration

## Installation of IB half-barrel



half-barrel are utilizes rollers fixed to the Cylindrical Structural Shell to slide along a rail system supported by the cage



# Mechanical Integration

