MICE Trigger System

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Contents

1 General description

1.1 Introduction

In MICE the spill is defined as the period when the target crosses the ISIS proton beam. The maximum spill repeating rate allowed by the MICE target system is $\sim 1\ Hz$. The Detector Data Acquisition (DDAQ) system of the experiment has been designed for the acquisition of up to 600 muon events in a 1 ms beam spill. It is based on VME Front-End Electronics (FEE) interfaced to Linux PC processors. The software framework performing the management of all the independent readout processes, the event building and the data taking human interface has been developed from the DATE package [1] provided by the CERN-ALICE experiment. The overall principle of the MICE DDAQ is that the readout is performed only at the end of the spill. In a normal operation mode the DDAQ cycle (Fig. 1) is started by the so called "Machine Start" signal, received from the ISIS Control room[1].
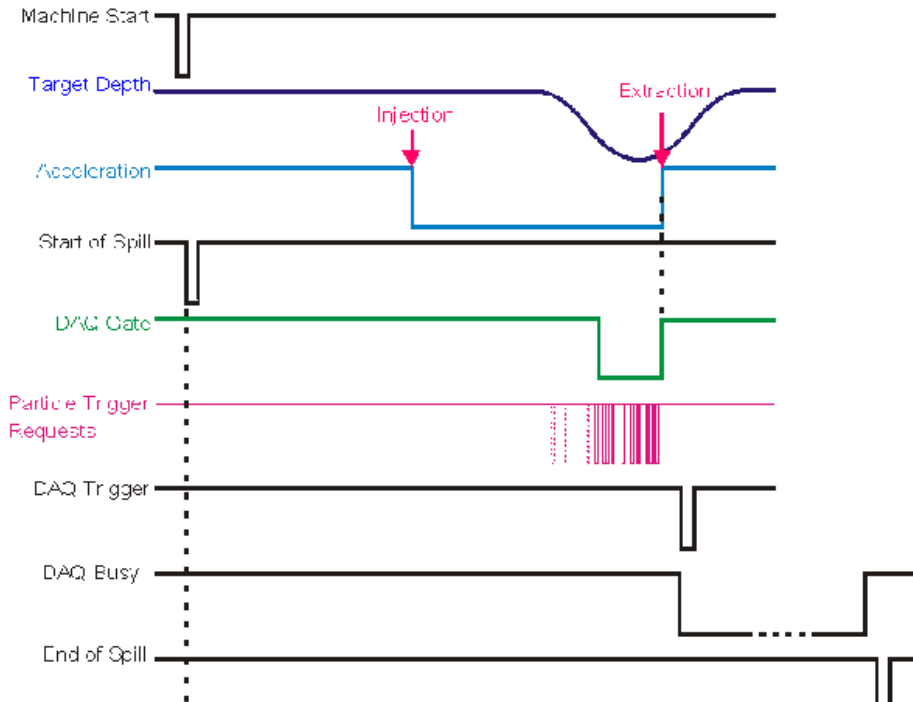

Figure 1: Time of the DAQ control signals.

1.2 MICE Trigger system

The MICE Trigger system is implemented exploiting two General Purpose VME Board CAEN V1495 [?] and five Input/Output Register CAEN V977 [3] (one

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[1]The same signal is used to synchronise the MICE target with the ISIS duty cycle.

per readout processes). The user firmwares fot the CAEN V1495 boards are available at https://launchpad.net/mice-trigger under the terms of the GNU General Public License.

The MICE DDAQ is strongly dependent on the Trigger System of the experiment. The duties of the Trigger system are:

Generation of the DDAQ control signals. The first part of the Trigger System is responsible for the generation the folowing DDAQ control signals:

1. Start of Spill: This signal is generated immediately after the beginning of the DAQ cycle. It triggers the so called START OF BURST event.

2. DAQ Spill Gate: Gate signal used by the EMR read boards (DBBs).

3. DAQ Trigger: This signal is generated after the end of the spill. It triggers the so called PHYSICS EVENT when the readout and storage of the digital data, corresponding to all the particle triggers received during a spill is performed.

4. End of Spill: This signal is generated immediately after the end of the readout of the physics data. It triggers the so called END OF BURST event.

Generation of the Particle Triggers. The second part is responsible for the generation of the so called Particle Trigger Request (PTR) and Particle Trigger (PT) signals. The programmable FPGA logic of the trigger allows for a great variety of trigger conditions[2].

The PTR signals are generated every time when the trigger condition is satisfied. The PT signals are generated from the PTRs only within the DAQ Spill Gate. Additional programmable veto rejects the PTRs which are too close in time to the last accepted PT [3].

The PT signel triggers the digitization of the analog signals received from the detectors. The TOF detectors pattern immediately after the generation of the PT is record in the Readout buffer of the first CAEN V1495 board.

2 VME Interface

2.1 Registers address map

The Address map for the Trigger engine board is listed in Table 1. All register addresses are referred to the Base Address of the board, i.e. the addresses reported in the Tables are the offsets to be added to the board Base Address.

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[2]For more details see sections: *Particle Trigger Generator Control register*, *TOF0 Mask*, *TOF1 Mask* and *TOF2 Mask*.

[3]For more details see section *Particle Trigger veto lenght*

Register name	Address	Addr. size	Data size	Read/Write
Event readout buffer	base + 0x0000-0FFC	A32	D32	R, BLT
Module reset*	base + 0x800A	A32	D32	W
GEO*	base + 0x102C	A32	D32	R/W
Status	base + 0x1030	A32	D32	R
User firmware version*	base + 0x1008	A32	D32	R
Number of triggers	base + 0x1034	A32	D32	R
Number of data words	base + 0x1038	A32	D32	R
Number of spills	base + 0x103C	A32	D32	R
Software cycle start	base + 0x1040	A32	D32	R
Busy times 0,1	base + 0x1060	A32	D32	R
Busy times 2,3	base + 0x1064	A32	D32	R
Busy times 4,5	base + 0x1068	A32	D32	R
Part. Tr. veto lenght	base + 0x100C	A32	D32	R/W
Spill Gate open delay	base + 0x1010	A32	D32	R/W
Spill Gate Clese delay	base + 0x1014	A32	D32	R/W
Spill Gate Gen. Ctrl	base + 0x1018	A32	D32	R/W
Part. Tr. Gen. Ctrl	base + 0x1028	A32	D32	R/W
TOF0 Mask	base + 0x101C	A32	D32	R/W
TOF1 Mask	base + 0x1020	A32	D32	R/W
TOF2 Mask	base + 0x1024	A32	D32	R/W

* This register is available also for the Translator board.

Table 1: Address Map

2.2 Event readout buffer

(base + 0x0000-0FFC; r, blt)
Each time a DAQ Spill Gate is created, the "Particle Triggers" accumulated during the spill are loaded into the Output Buffer where they are organised in events. Each event consists of:
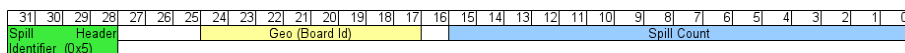

Figure 2: Spill header.

Spill header The Spill header (Fig. 2) contains the Header Identifier (0x5), the GEO number of the board and the spill number.
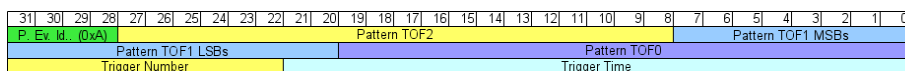

Figure 3: Particle event record.

Spill payload The spill payload contains a number of consecutive Particle Event records. Each record is made of three 32bit words. The structure of the Particle Event Record is shown on Fig. 3. It contains:

1. Particle Event Identifier (0xA);

2. The TOF0, TOF1 and TOF2 patterns are coded in 20 bits each. The first 10 bits are used to code the pattern in the vertical plane of the detector and respectively the second 10 bits correspond to the horizontal plane of the detector;

3. Trigger number inside the spill is coded in 10 bits;

4. Time of the trigger with respect to the beginning of the Spill Gate is coded in 22 bits using 10 nanosecond unit (max time ~ 0.4 sec.).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Spill Trailer Identifier (0xF)					Trigger Count												Spill Count														
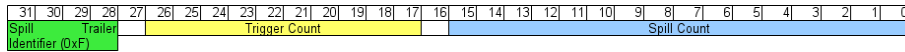
Figure 4: Spill Trailer.

Spill trailer The Spill trailer (Fig. 4) contains the Trailer Identifier (0xF), the number of the Accepted Particle Triggers during the spill and the spill number.

2.3 Module reset register

(base + 0x800A; w)
A dummy access to this register allows to reset the module. After the reset all the configuration registers are set to there default values and the Event readout buffer is empty.

2.4 GEO register

(base + 0x102C; r/w; Default : 0x0)
This register can be accessed both in read and write mode. It allows to write the correct GEO address (default setting = 0) of the module before operation. GEO address will be contained in the SPILL HEADER.

2.5 Status register

(base + 0x1030; r)
This register (Fig. 5) aims to be useful only for debugging. It isn't made to be used during the operation of the board.

2.6 User firmware version register

(base + 0x1008; r)
This register (Fig. 6) contains the User Firmware version number and the Board type identifier. Board type identifier is equal to 0x0 for the Trigger engine board and to 0x1 for the Translator board.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						rdusedw												wrfull	rdempty	Trigger Controller State Machine Status											BLT ready

Figure 5: Status register.

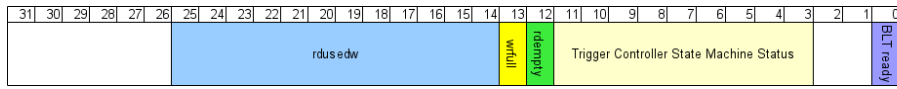| 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																								Board Type Id.				Firmware release			
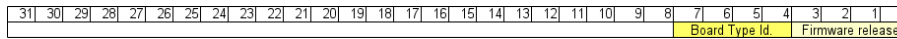
Figure 6: User firmware version register.

2.7 Number of triggers register

(base + 0x1034; r)

This register contains the number of Particle Triggers generated during the last spill. The number of Particle triggers currently stored in the Output Buffer can be bigger if no readout is performed after the end of the previouse spill. The number of triggers is also contained in the SPILL TRAILER.

2.8 Number of data words register

(base + 0x1038; r)

This register contains the number of Data Words generated during the last spill. The number of Data Words currently stored in the Output Buffer can be bigger if no readout is performed after the end of the previouse spill.

2.9 Number of spills register

(base + 0x103C; r)

This register contains the number of Spills generated after the last reset of the board. The Spill number is also contained in the SPILL HEADER and the SPILL TRAILER.

2.10 Software cycle start register

(base + 0x1040; r)

This register can be accessed only in read mode. The access to this register allows to start a new DAQ cycle ($Start\,of\,Spill \rightarrow Spill\,Gate \rightarrow DAQ\,Trigger \rightarrow End\,of\,Spill$). The read value is the numper of the spill which will be generated.

2.11 Busy times 0,1 register

(base + 0x1060; r)

The lenght in time of the DAQ busy signals generated by readout processe 0 and readout processe 1 are coded in 16 bits (Fig. 7) using 3.2 $\mu sec.$ unit (max time $\sim$ 210 msec.).

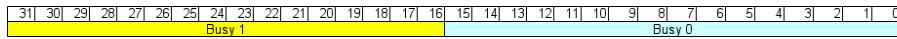| 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Busy 1																Busy 0															

Figure 7: Busy 0,1.

2.12 Busy times 2,3 register

(base + 0x1064; r)

The lenght in time of the DAQ busy signals generated by readout processe 2 and readout processe 3 are coded in 16 bits (Fig. 8 using 3.2 μsec. unit (max time $\sim$ 210 msec.).

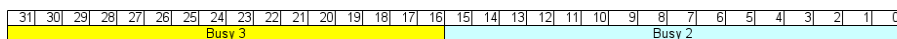| 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Busy 3																Busy 2															

Figure 8: Busy 2,3.

2.13 Busy times 4,5 register

(base + 0x1068; r)

The lenght in time of the DAQ busy signals generated by readout processe 4 and readout processe 5 are coded in 16 bits (Fig. 9) using 3.2 μsec. unit (max time $\sim$ 210 msec.).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Busy 5																Busy 4															

Figure 9: Busy 4,5.

2.14 Particle Trigger veto lenght register

(base + 0x100C; r/w; Default : 0x1E)

This register can be accessed both in read and write mode. It allows to set the time lenght of the veto that rejects the PTRs which are too close in time to the last accepted PT. 10 ns units are used (default setting = 300 ns).

2.15 Spill Gate open delay register

(base + 0x1010; r/w; Default : 0x7F)

This register can be accessed both in read and write mode. It allows to set the time of the beginning of the Spill gate with respect to the "Machine start" sihnal. 10 ns units are used (default setting = 1.27 μs).

2.16 Spill Gate Clese delay register

(base + 0x1014; r/w; Default : 0xFF)

This register can be accessed both in read and write mode. It allows to set the time of the end of the Spill gate with respect to the "Machine start" sihnal. 10 ns units are used (default setting = 2.55 μs).

2.17 Spill Gate Generator Control register

(base + 0x1018; r/w; Default : 0x0F)
This register (Fig. 10) can be accessed both in read and write mode. It allows to program the structure of the DDAQ cycle (Fig. 1). The meaning of the bits in this register is the following:

- Bit 0 - Enable/Disable of the generation of the Start of Spill signal.

- Bit 1 - Enable/Disable of the generation of the End of Spill signal.

- Bit 2 - Enable/Disable of the generation of the Spill Gate and DAQ Trigger signals.

- Bit 3 - Enable/Disable of the generation of Calibration triggers.

- Bit 4 - If this bit is set the internal processing of the DAQ cycle is disabled. In this case an external Spill Gate signal is expected at input G1.

- Bits 8-13 Enable/Disable the DAQ busy inputs (0-6).

- Bit 28 Enable/Disable the external (Tracker) veto.

Figure 10: Spill Gate Generator Control register.

Default value is: Start of Spill, End of Spill, Phys Event and Calibration Event are enabled. External Spill Gate, External veto and all the Phys. Busies are disabled.

2.18 Particle Trigger Generator Control register

(base + 0x1028; r/w; Default : 0x18)
This register (Fig. 11) can be accessed both in read and write mode. It allows to program the trigger condition.

Figure 11: Particle Trigger Generator Control register.

The trigger condition can be a combination of:

- Coincidence of hits in both PMTs attached to a slab in any of the TOF stations;

8

- Hit in the Gva counter;

- Pulser trigger.

This register contains the following sections, used to program the trigger condition:

1. Trigger logic configuration for TOF0,TOF1 and TOF2. For the meaning of the bits in the Trigger logic configuration see Table 2

2. Global trigger condition. For the meaning of the bits in the Global trigger condition see Table 3

3. Pulser trigger condition . For the meaning of the bits in the Pulser trigger condition see Table 4

bits 0-2	TOF station trigger logic configuration
000	This station is disabled fron the trigger condition
001	Coincidence in Vertical plain only
010	Coincidence in Horizontal plain only
011	Coincidence in Vertical OR Horizontal plains
111	Coincidence in Vertical AND Horizontal plains

Table 2: The meaning of the bits in the Trigger logic configuration sections of the Particle Trigger Generator Control register.

bits 0-1	Global trigger condition
00	TOFs Trigger condition* ONLY
01	TOFs Trigger condition* OR Gva
10	TOFs Trigger condition* OR Pulser
11	TOFs Trigger condition* OR Gva OR Pulser

*Trigger condition specified by the Trigger logic configurations for TOF0,TOF1 and TOF2 (bits 0-8 on Fig. 11).

Table 3: The meaning of the bits in the Global trigger condition sections of the Particle Trigger Generator Control register.

Default setting: TOF1 - Coincidence in Vertical OR Horizontal plains

Examples:
TOF0 Vertical AND Horizontal plains   0x7
GVA   0x200
Pusler trigger 50KHz   0x2400
Pusler trigger 200KHz Rand. period   0xB400

bits 0-2	Pulser frequency		bits 3-4	Pulser Randomness
000	2 KHz		00	No Randomness
001	5 KHz		01	Random start
010	10 KHz		10	Random period
011	20 KHz		11	Random start and period
100	50 KHz			
101	100 KHz			
110	200 KHz			
111	500 KHz			

Table 4: The meaning of the bits in the Pulser trigger condition sections of the Particle Trigger Generator Control register.

2.19 TOF0 Mask register

(base + 0x101C; r/w; Default : 0xFFFFF)
This register (Fig. 12) can be accessed both in read and write mode. It allows to customise the configuration of slabs in the two planes of TOF0 included in the Trigger condition (default setting - all slabs are included).
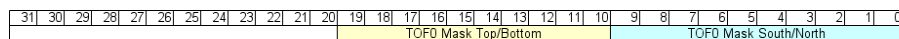
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												TOF0 Mask Top/Bottom										TOF0 Mask South/North									

Figure 12: TOF0 Mask register.

2.20 TOF1 Mask register

(base + 0x1020; r/w; Default : 0xFFFFF)
This register (Fig. 13) can be accessed both in read and write mode. It allows to customise the configuration of slabs in the two planes of TOF1 included in the Trigger condition (default setting - all slabs are included).
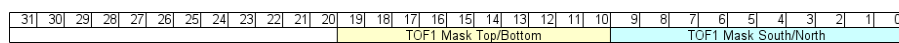
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												TOF1 Mask Top/Bottom										TOF1 Mask South/North									

Figure 13: TOF1 Mask register.

2.21 TOF2 Mask register

(base + 0x1024; r/w; Default : 0xFFFFF)
This register (Fig. 14) can be accessed both in read and write mode. It allows to customise the configuration of slabs in the two planes of TOF2 included in the Trigger condition (default setting - all slabs are included).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												TOF1 Mask Top/Bottom										TOF1 Mask South/North									

Figure 14: TOF1 Mask register.

3 Front panel I/Os and connection for CAEN V1495 and CAEN V977

The two V1495 boards (so called Trigger engine and Translator) are situated in the Central Trigger VME crate (Fig.15). In addition we have one V977 board (I/O register) in each crate. Connection scheme of this boards is shown on Fig. 16.
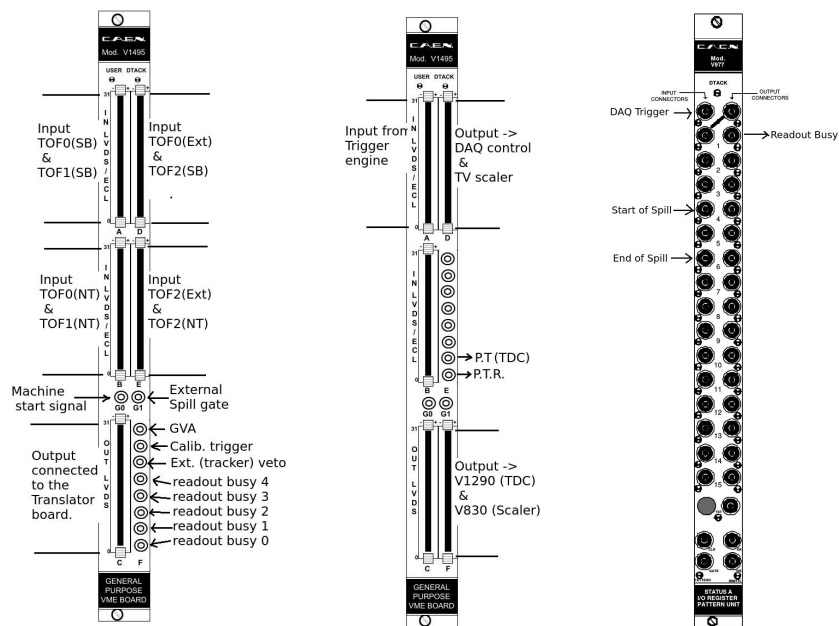

Figure 15: Central Trigger VME crate.

11

Figure 16: Left: Trigger engine board connection scheme. Middle: Translator board connection scheme. Right: I/O connection scheme.

References

[1] ALICE DAQ and ECS Manual, *https://ph-dep-aid.web.cern.ch/ph-dep-aid/Collaborators/DATE/Releases/kits/doc/dateUserGuide.pdf*

[2] CAEN V1495 Technical Information Manual
http://www.caen.it/servlet/checkCaenManualFile?Id=8618

[3] CAEN V977 Technical Information Manuel
http://www.caen.it/servlet/checkCaenManualFile?Id=5172