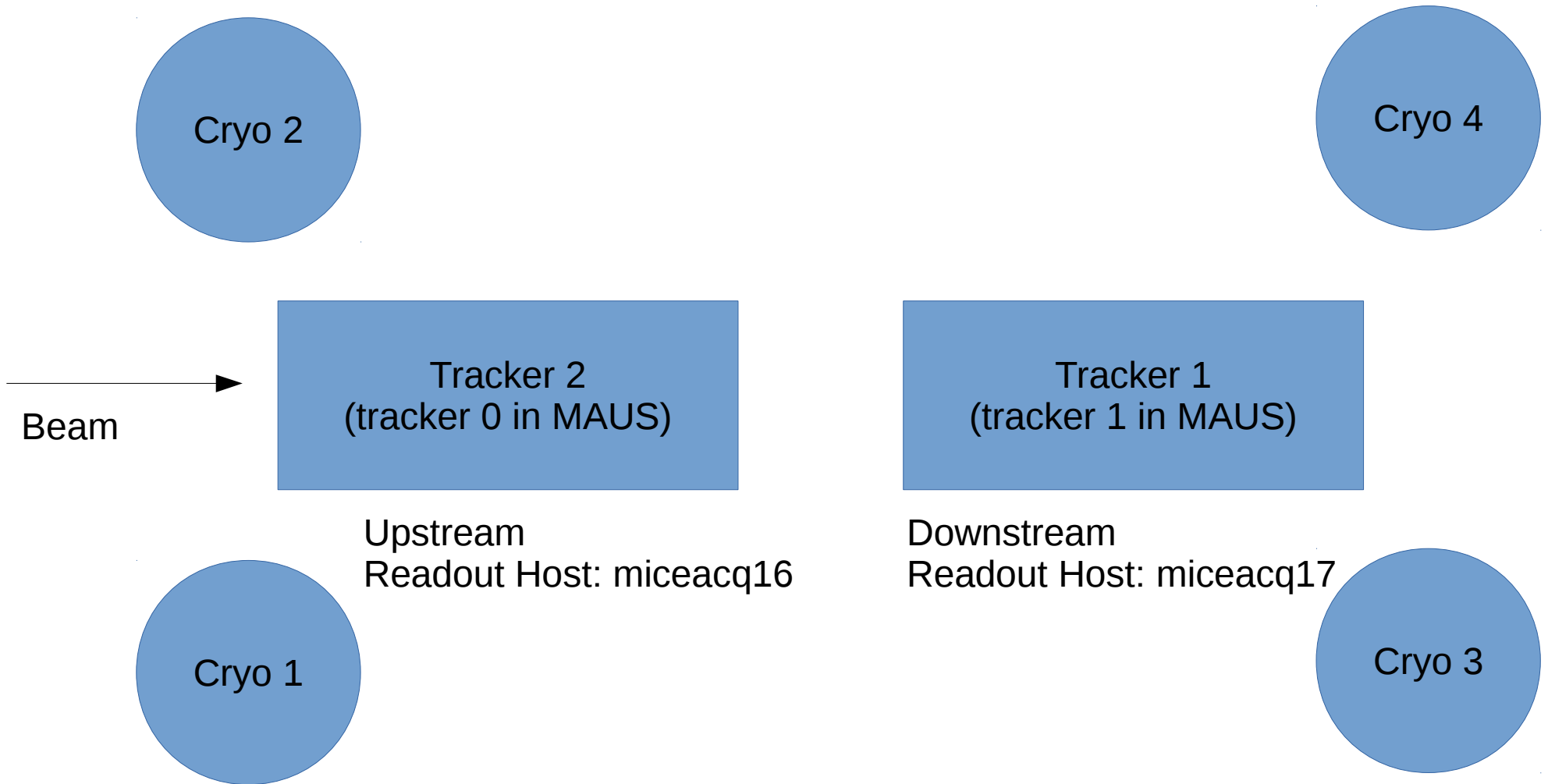


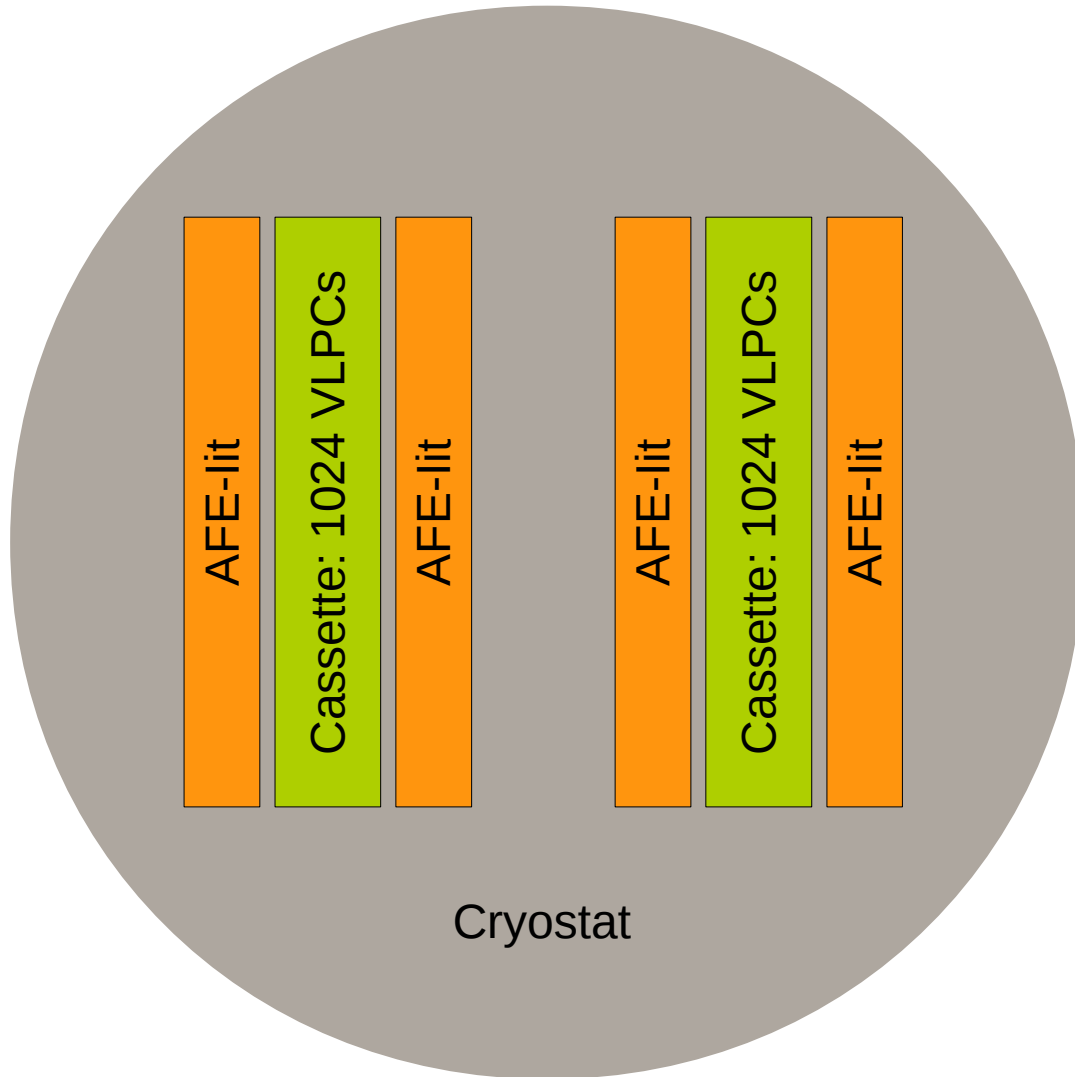
Tracker Data Acquisition

- System schematics
- Data Format
- Timing Signals
- Trigger
- Date Readout
- Hardware Status
- DAQ Code Changes

System Overview



System Schematic



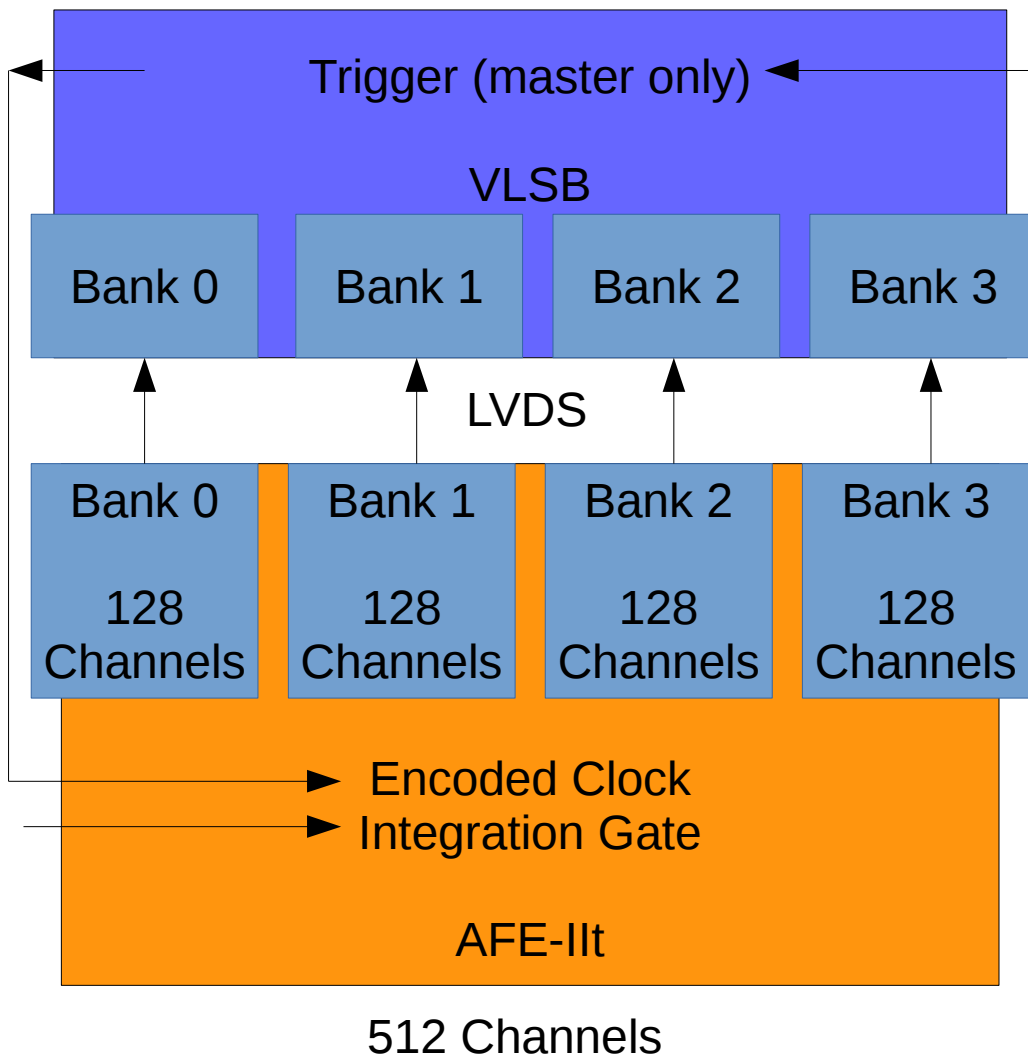
Each cryostat contains two “cassettes”, and has 2048 channels of readout

Each cassette contains 1024 VLPCs, which must be temperature regulated to 9.0K.

The VLPCs were fabricated in modules of 8.

Readout of each cassette is performed by two Analog Front End II with Timing (AFE-II) boards.

System Schematic



Each AFE has 512 channels and is responsible for digitising the charge and timing data.

Charge is Integrated over a period dictated by the Integration Gate. This data is stored in an analog pipeline.

A trigger (externally generated) is sent to one of the VLSB boards, where it is encoded and distributed to the AFE boards.

Upon receiving a trigger the AFE-lit looks back in the analog pipeline and begins the digitisation process (5.7us dead time).

The 512 channels are divided into 128 channel banks. Data is sent from the AFE to the VLSB where it is buffered until the end of spill.

Data Format

- Each channel transmitted and stored has the following data:
 - 31-24 : Event in spill.
 - 23 : Discriminator Bit.
 - 22-16 : Channel Number
 - 15-8: TDC
 - 7-0: ADC
- The readout ordering is not continuous:
 - 0, 64, 32, 96
 - 1, 65, 33, 97
 - 2, 66, 34, 98
 - .. and so on.

Timing Signals

- The integration gate for the front end boards is ***synchronised*** to particle arrival.
- This is done using the ISIS-1RF reference signal, which is synchronised to the protons in ISIS.
- The ISIS 1-RF is a 2.9-3,1 MHz sine wave(in region of interest), we get our timing by:
 - Triggering on rising edge, zero crossing.
 - Apply variable delay.
 - Apply variable gate.
- The system implemented can provide up to 4 synchronous gates.

Timing Signals II

- We produce 4 timing signals:
 - Alive window: Veto triggers inside the DAQ to a 110 ns wide window. Note that this time is likely to be shortened.
 - Integration window upstream: The charge integration gate sent to the upstream AFE boards. This is 190ns wide at the boards.
 - Integration window downstream: The charge integration gate sent to the downstream AFE boards.
 - Timing gate for triggering LED system.

Trigger

- To only trigger the DAQ equipment when the tracker actuarially integrates charge 3MHz based, 110ns wide alive window must be implemented in the trigger.
- Yordan finalised the firmware containing this modification just after MDR3 and with plenty of time prior to beam.
- When testing on the live system we found some glitch triggers were generated and yordan fixed these in the vhdl.
- The alive window veto can be disabled by adjusting a register setting on the V1495.
- The firmware is now stable.

DATE Readout

- The two trackers are connected to two data acquisition machines:
 - Upstream = miceacq16, LDCID 3
 - Downstream = miceacq17, LDCID 4
- Integration with date was started in January.
- Thanks to yordans diligence in looking over the data in the unpacking a number of readout errors were spotted.
 - These were caused by mistakes in the wrapper layers.
 - These were fixed in the post MDR debug.
- When integrating with the downstream detector, the GEOID's for the equipment was set wrongly. This was spotted during beam running and fixed (although it did crash the code at first, and a quick cheap modification (hack) was put in place)
- DATE readout is now working for both detectors.

Hardware Status

- Upstream tracker is OK.
- Downstream tracker has issues on two banks, reading incorrect event numbers.
- Possible issues in readout of 4th station.
- Investigation of these issues is a priority
- Spares...
 - Need to perform an inventory of spares (with calibrations – few at present).
 - Need to setup onsite test stand.
 - Prepare spare boards, so hotswap is possible.

DAQ Code Changes

- The DAQ code at present is implemented in a complex library. (TrReadoutLib).
 - This has a large amount of superfluous readout machinery.
 - It is wrapped by two layers (MICE Daq Equipment) and DateReadout code.
 - These layers are difficult to follow, and tough to debug.
 - VME operations are not checked for success.
 - VME multiread is used, which claims to be “fast”, 3.2Mbyte/s. Will try using block transfers.
 - Errors are not reported back using the standard machinery set up in Mice Daq Equipment.
- Rewrite is planned to address these issues.