On the FMC ADC project

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Current system

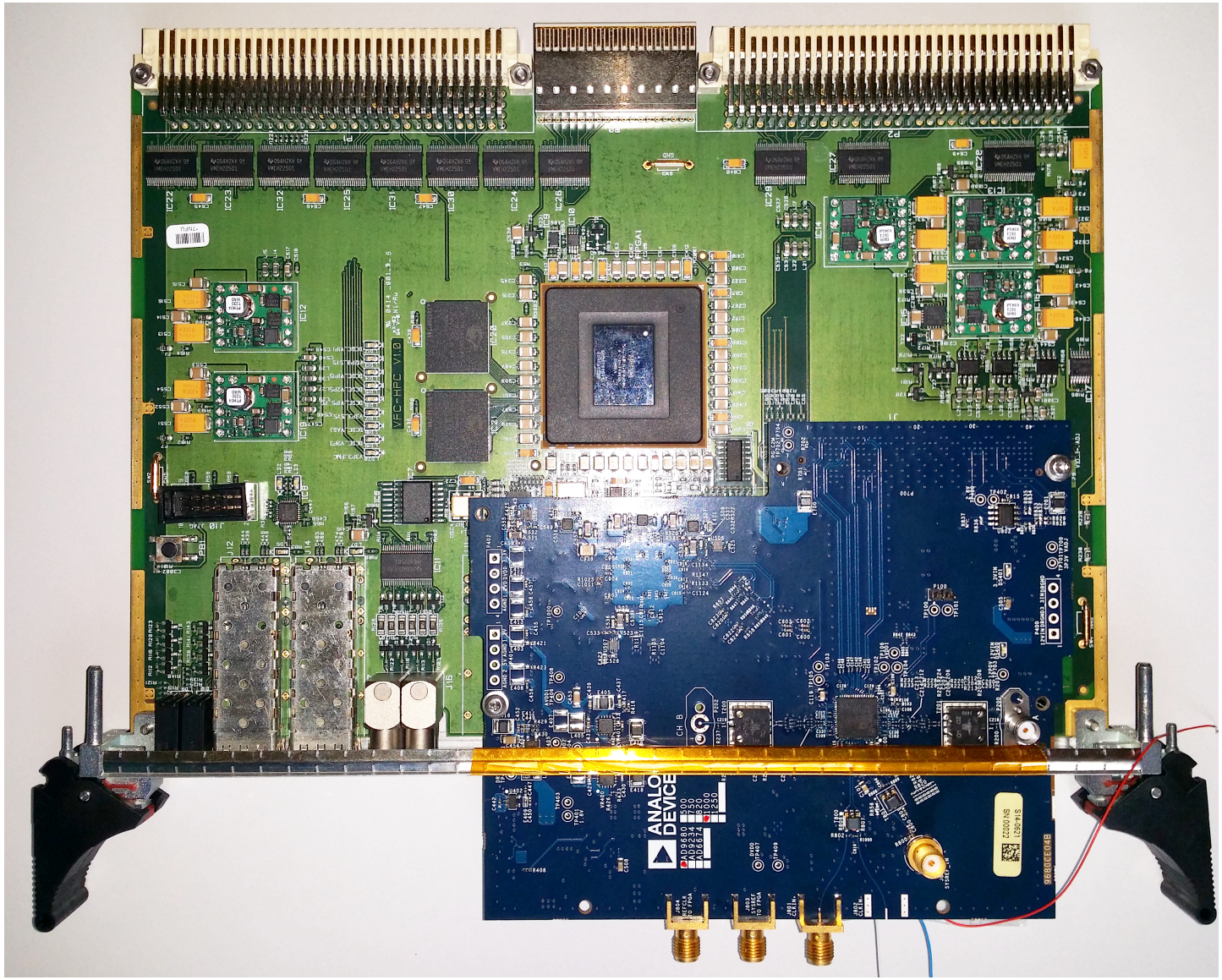
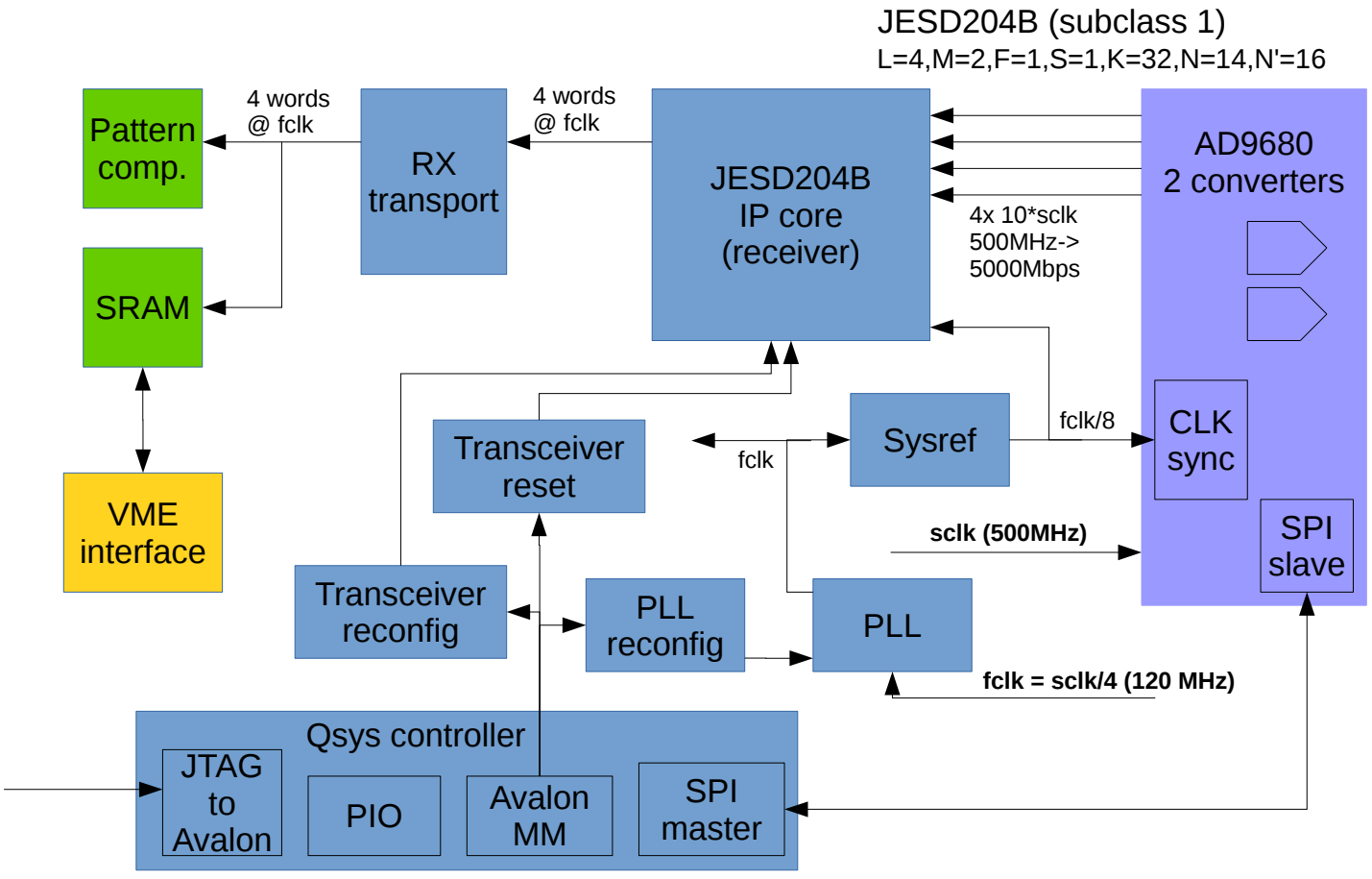
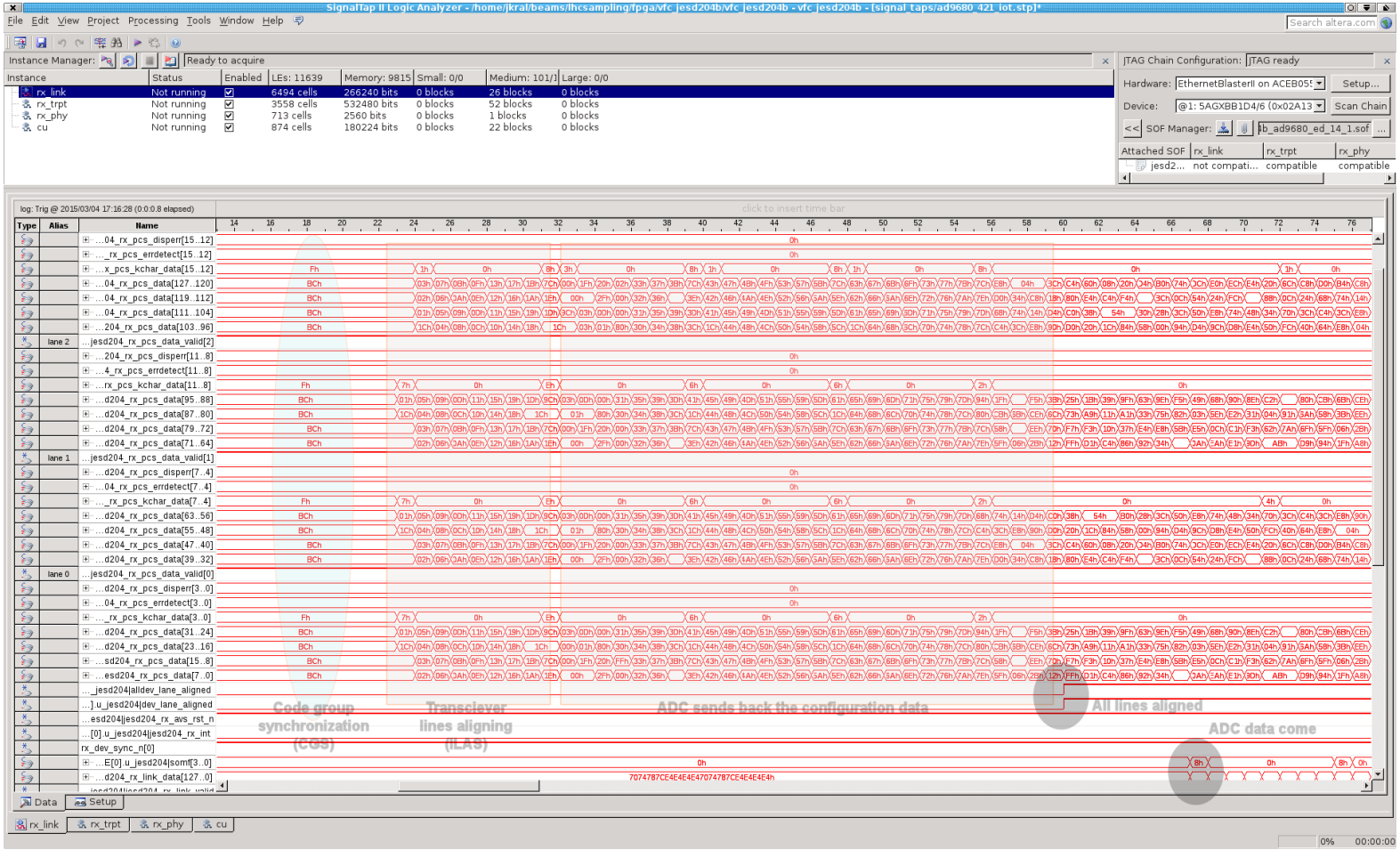


Figure: VFC V1.0 with FMC ADC AD9860 eval board

Actual implementation

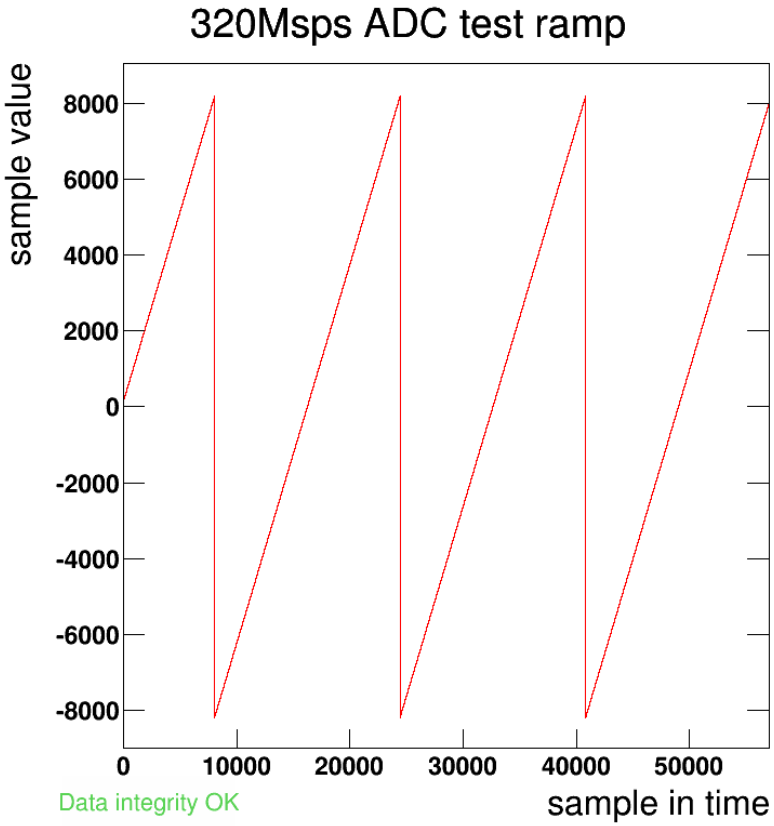


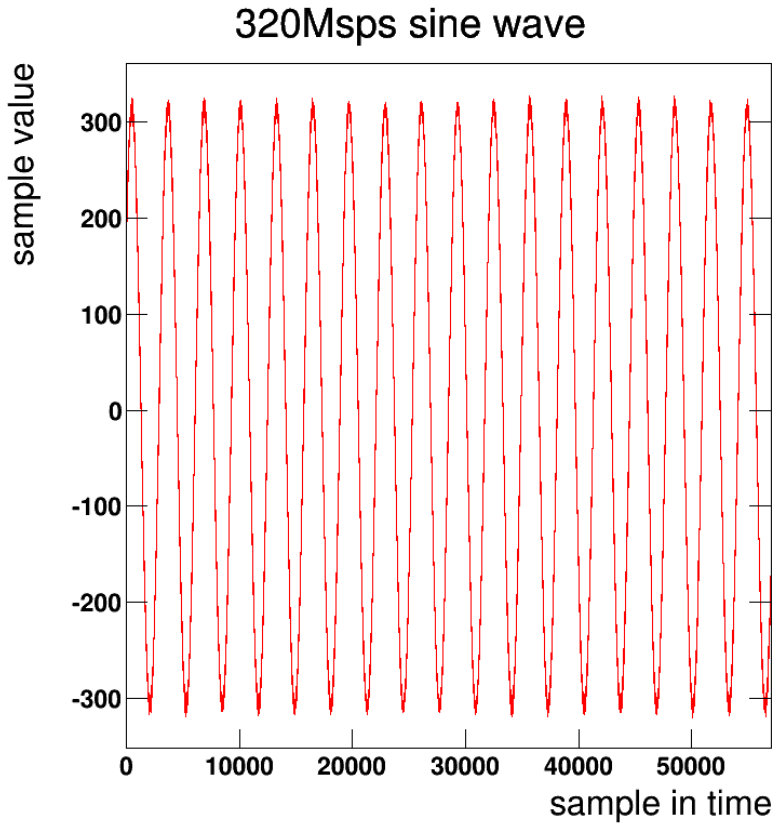
ADC syncing


SignalTap II Logic Analyzer - /home/jkral/beams/lhcsampling/fpga/vfc_jesd204b/vfc_jesd204b - vfc_jesd204b - [signal_taps/ad9680_421_lot.stp]*
Code group synchronization (CGS)
Transciever lines aligning (ILAS)
ADC sends back the configuration data
All lines aligned
ADC data come

Measurements at 320MSPS

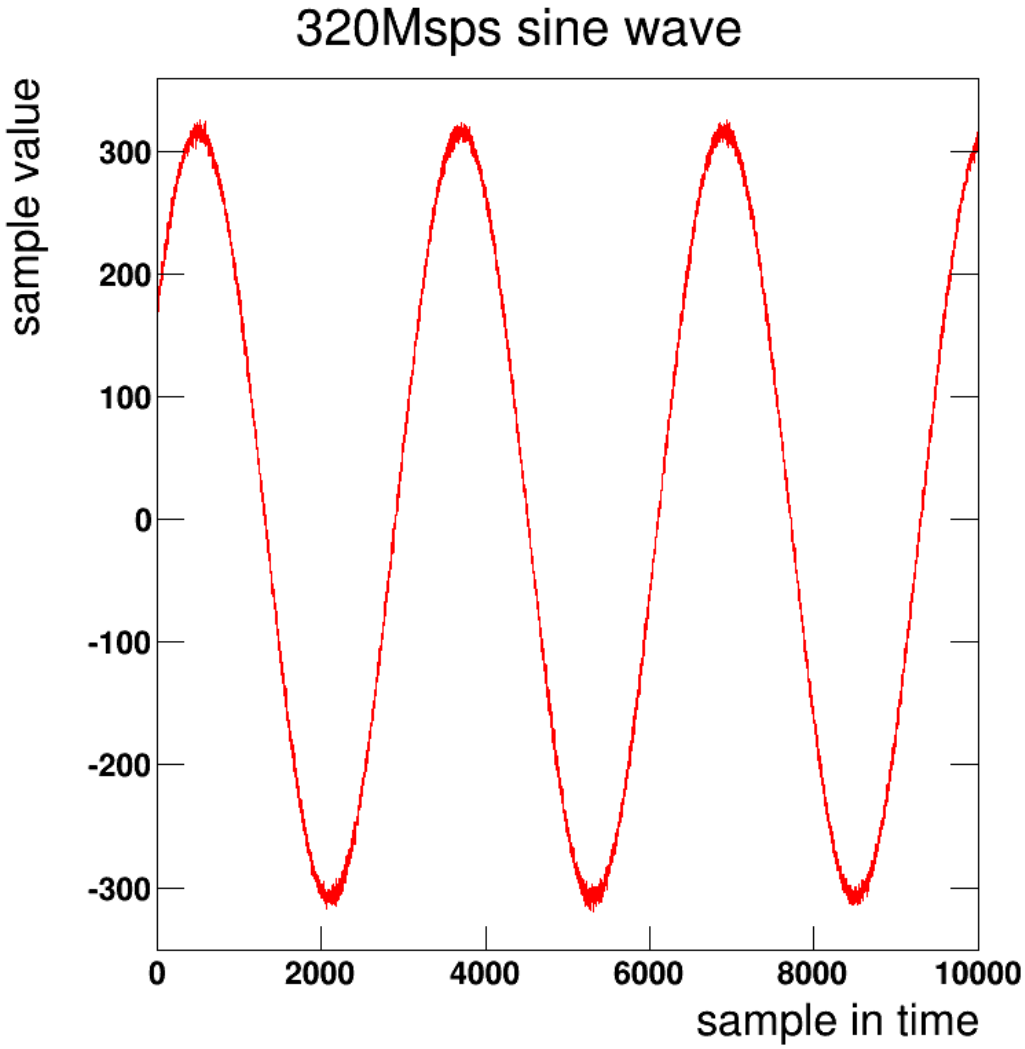
- ADC clock = 320 MHz, FPGA clock = 80 MHz, 100 kHz sine





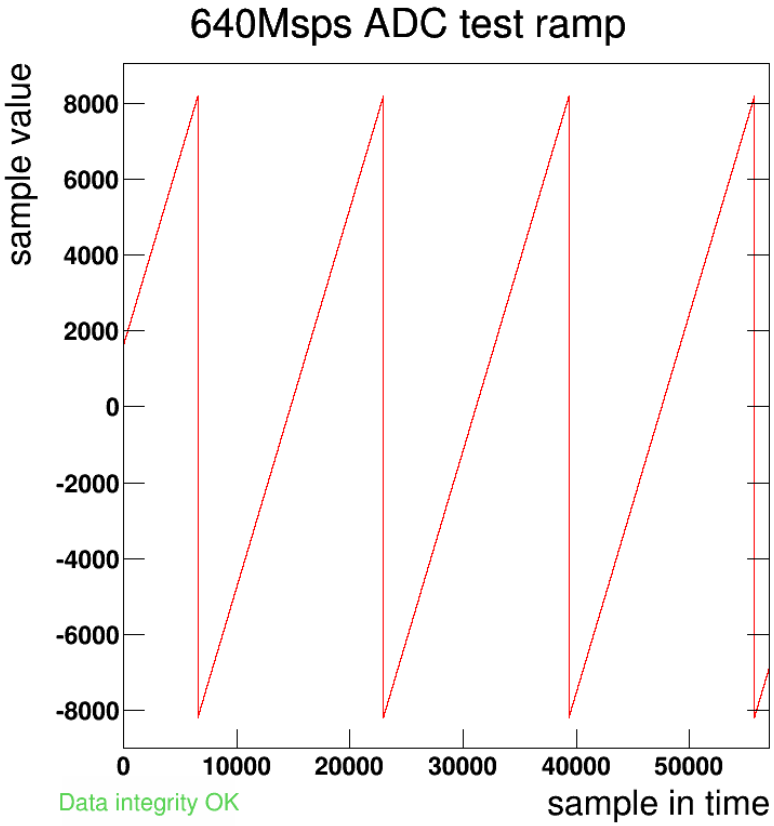
Measurements at 320MSPS cont'd

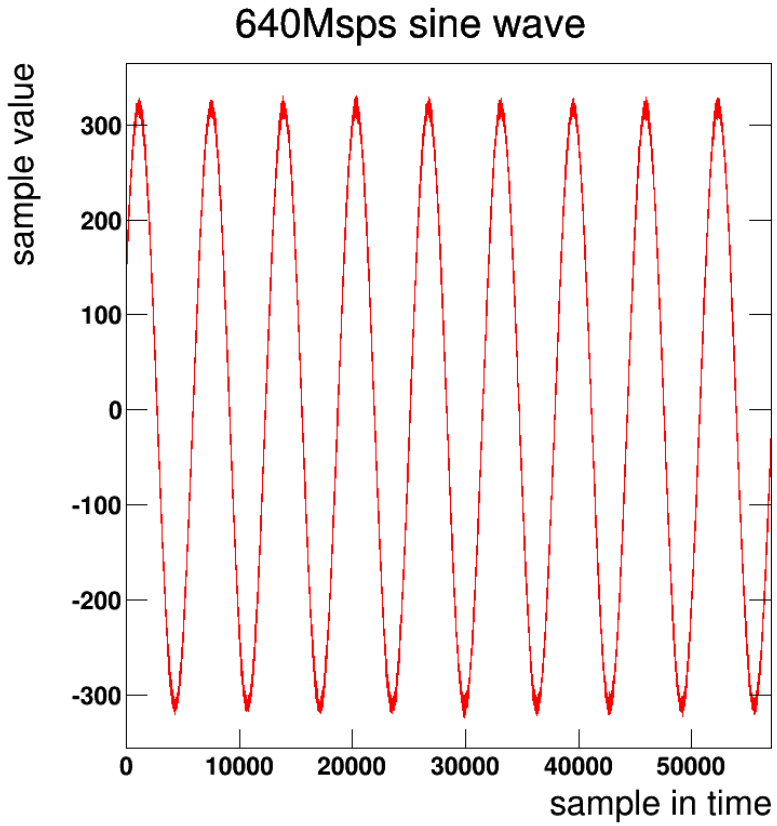
- Sine zoom



Measurements at 640MSPS

- ADC clock = 640 MHz, FPGA clock = 160 MHz, 100 kHz sine

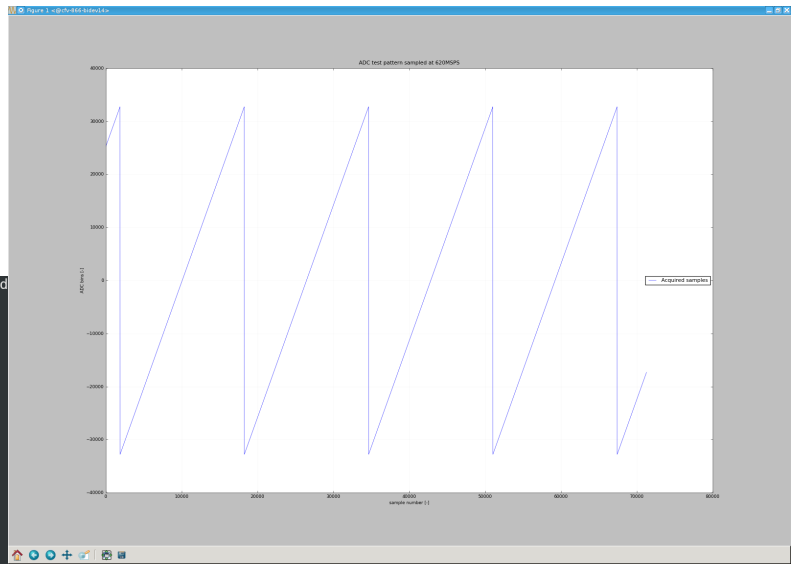




Setting up and fetching the data

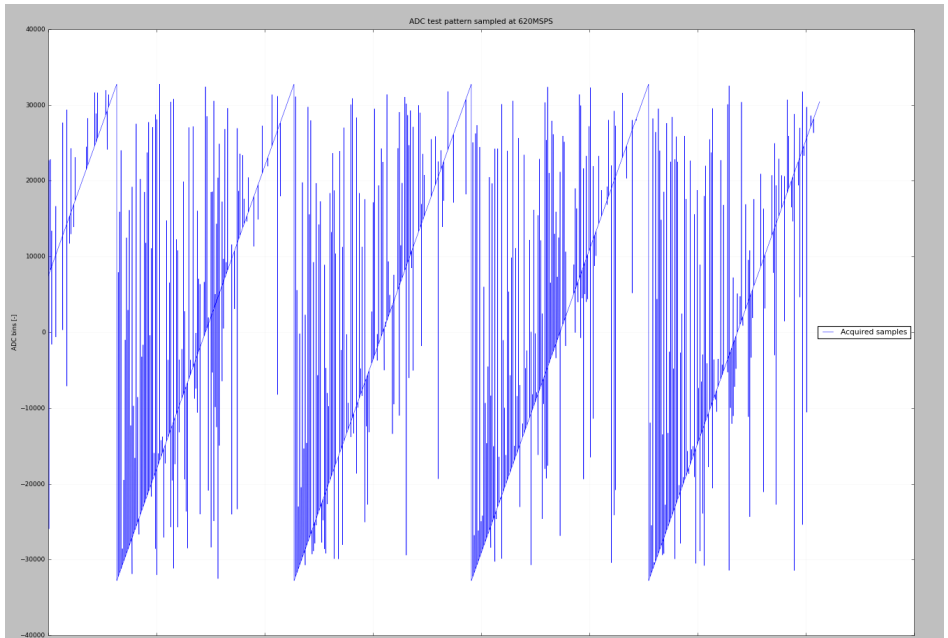
- VME preliminary drivers description files were written and the drivers were generated.
- Exported SRAM chips, some identification registers and a control register into the VME space to be able to start the acquisition
- Python script was written, which is able to fetch from the VME space the data through the 'standard' mechanism of encore drivers.

```
name,rwmode,block,block_address_space,block_offset,register_offset,offset,wordsize,depth,d
BOARDID,r,0,1,0x0,0x0000,0x0000,uint32,0,Board identification number,32,32
FPGAFIRMWARE,r,0,1,0x0,0x0004,0x0004,uint32,0,FPGA firmware version,32,32
FPGACOMPILATION,r,0,1,0x0,0x0008,0x0008,uint32,0,FPGA compilation time,32,32
FPGASTATUS,r,0,1,0x0,0x000C,0x000C,uint32,0,FPGA status register,32,32
COMMAND,rw,0,1,0x0,0x0040,0x0040,uint32,0,command register,32,32
CPLDTEMPHI,r,0,1,0x0,0xf7d8,0xf7d8,uint32,0,DS18B20U temperature chip high word,32,32
CPLDTEMPLO,r,0,1,0x0,0xf7dc,0xf7dc,uint32,0,DS18B20U temperature chip low word,32,32
CPLDPLATFORM,r,0,1,0x0,0xf7e0,0xf7e0,uint32,0,platform code (VFC1),32,32
CPLDCOMPILATION,r,0,1,0x0,0xf7e4,0xf7e4,uint32,0,dead beef,32,32
CPLDFIRMWARE,r,0,1,0x0,0xf7e8,0xf7e8,uint32,0,dead beef,32,32
CAPABILITY,r,0,1,0x0,0xf7ec,0xf7ec,uint32,0,what you can do with the card,32,32
CPLDCONFIG,r,0,1,0x0,0xf7f0,0xf7f0,uint32,0,CPLD configuration,32,32
SERIALHI,r,0,1,0x0,0xf7f4,0xf7f4,uint32,0,VFC HI part of serial nb,32,32
SERIALLO,r,0,1,0x0,0xf7f8,0xf7f8,uint32,0,VFC LO part of serial nb,32,32
SSRAMCHIP1,rw,0,1,0x0,0x800000,0x800000,uint32,2097152,SRAM data sample chip 1,32,32
SSRAMCHIP2,rw,0,1,0x0,0x1000000,0x1000000,uint32,2097152,SRAM data sample chip 2,32,32
```



Issues being currently solved

1. We still do not have a valid JESD204b license. John Evans is looking into this
2. drivers (or python wrapper) do not allow to load more than 1MLWord of the data at one go (not a real issue)
3. timing issues in the Quartus project - the SRAM memories are used in parallel, the project is not yet correctly constrained and hence at higher speeds we get erratic VME readings however the watchdog component does not trip (hence timing issue ADC $\rightarrow$ SRAM or SRAM $\rightarrow$ VME)



Outlook - hardware development

Done

- the 'basic' framework is done: VME register space, ADC setting up, data acquisition into the SRAMs, readout of the SRAMs via the VME iface
- GIT repository is already available and well maintained:

```
git clone ssh://lxplus.cern.ch/afs/cern.ch/project/fi/git/vfc_jesd204b.git
```

Follows

- we will concentrate on cleaning of the project to be usable for the others (automatic ADC programming from the start, VME registers allowing to control the test patterns, TCL goes out, TIMING ISSUES)
- long term link stability measurements will be performed by writing the python acquisition and test suites
- connection of the LHC clock through the SFP interface and generation all clock signals required for the ADC from there.

Outlook cont'd

- Start FBCT project related tasks
  - ADC linearity measurement test bench construction
  - turn clock data sampling synchronisation
  - implementation of the integration methods
  - implementation of the base line restoration and averaging
- preparation for Vfc V2.0 (DDR controller and how to store the data in the DDR memory, how to fetch them out of the Vfc(!))
- `In parallel procurement of any JESD204b 1GSPS FMC card`, see next slides

FMC modules availability

FMC-1000

1. Contacted Innovative, we get the offer:

Quotation date: 18.02.2015 Validity: 30 days

Pos	Ref.	Description	Unit Price CHF	Qty	Total CHF
1	80325-2-L0	80325-2-L0: FMC-1000, FMC module with 2-ch, 1000 MSPS, 14-bit ADC, two 1000 MSPS DACs, DC coupled A/D & DACs	7'100.00	1	7'100.00
		Conditions: Buyer acknowledges by placing purchase orders that sale is subject to Magentasys' General Conditions of Sales and Delivery ***EXW Genolier, Switzerland*** ***Shipping & Handling not included***			

Total CHF:	**7'100.00**

Payment Terms: 30 days

2. Delivery terms: promised May, likely June if we're lucky

FMC modules availability

Delphi engineering

1. Delphi quotes 16 wk delivery on orders received now
2. But
   - we don't have a data sheet
   - we don't have an exact part number
   - we know nothing about the product they want to sell to us
3. Daniel requested more information, so far no answer (email Feb. 24)

Current issues

1. Technical details of FMC-1000 not clear as no final version of the data sheet is available. Some technical issues were resolved yesterday.[1]
2. Lack of direct communication from Delphi (Curtiss-Wright)
3. Innovative communicates better, but they are unreliable what concerns the delivery terms
4. Recent news: we can have 1 FMC-1000 pre-release (some bugs in DAC chain) and when final comes, they will swap it. this one would be for march!!

Maybe this is a moment as well to choose another FMC mezzanine using JESD204b ADC, which does not comply with FBCT system requirements, but helps us to continue the development. When an FMC suitable for FBCT comes, buy it. Procurement service?

[1] Kudos to Andrea and Manoel as well for looking into the VFC → FMC1000 pin compatibility

Project time-line

- Jan 2013 - project starts with JJo, math model, market research. FMC500 as a candidate, 400MSPS eval board
- beg. Feb 2014 - JJo leaves, no manpower allocated
- beg. Apr 2014 - Daniel comes to CERN
- 4 Apr 2014 - we get first Vfc schematic from Andrea
- 17 Jun 2014 - FMC-310 is here, with xilinx career not working due to drivers
- 25 Aug 2014 - Innovative announces FMC-500 for Dec 2014, FMC-310 still does not work for us
- 10 Sep 2014 change the strategy to serial ADC!!
- 12 Sep 2014 - FMC-500 WILL NOT EXIST
- 2 Oct 2014 we get the very first Vfc, but FMC310 was not connected due to change of strategy
- 17 Oct 2014 delphi promises engineering samples of their 1GSPS to Jan 2015
- 3 Dec 2014 we finally get AD9860 ADC board and we can start any development

Time-line summary

All that only to say, that

- we had a real hardware available beg. December, so we are working on new serial ADC for only 11 weeks.
- we had zero success to obtain any FBCT suitable ADC mezzanine
- actually FMC-500 is in an 'engineering sample', i.e. 1.5 year after the first TTM estimation. FMC-1000 exist as first prototype, and we believe, that Delphi FMC ADC does not exist.