Hyper-Kamiokande DAQ

Overview
Ongoing R&D items

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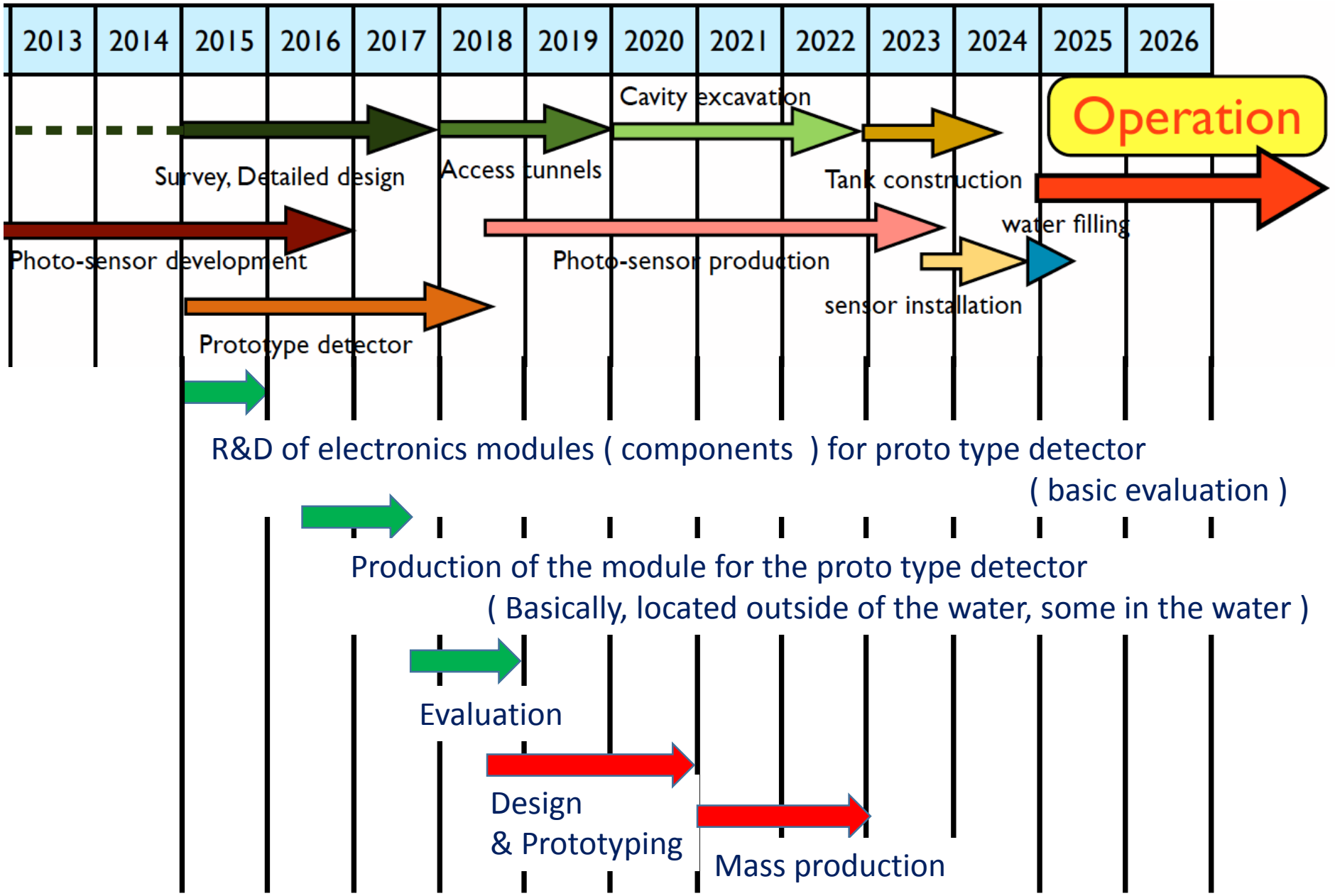
Timeline

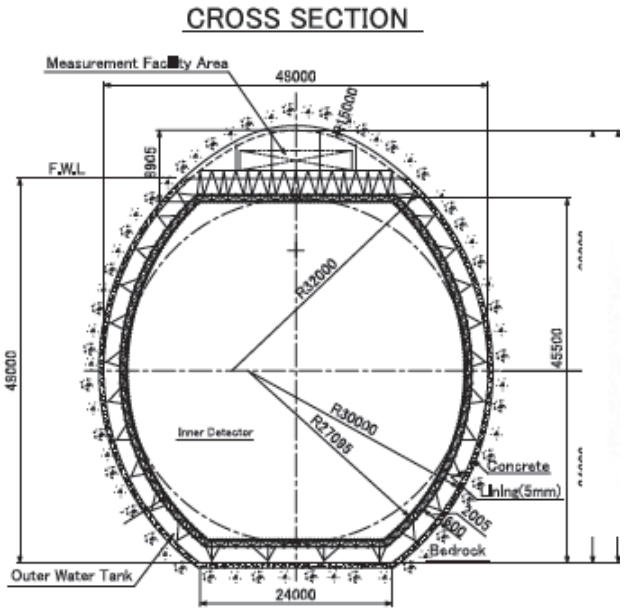

2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
Cavity excavation
Operation
Survey, Detailed design
Access tunnels
Tank construction
water filling
Photo-sensor development
Photo-sensor production
sensor installation
Prototype detector
R&D of electronics modules (components) for proto type detector
(basic evaluation)
Production of the module for the proto type detector
(Basically, located outside of the water, some in the water)
Evaluation
Design
& Prototyping
Mass production

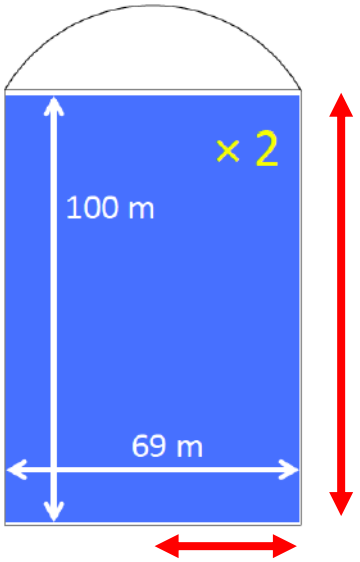
Two possibilities ~ In the water or outside of the water ~

Possible problems in running the cables to each photo sensor

a) Length of the cable

Maximum length of the cable > 100 ~ 200 m





15m (bottom)
+ 55m (wall)
+ 30 m (surface)

40 m (bottom)
+ 110 m (wall)
+ 40 m (surface)

- Degradation of the signal is expected.
- Different lengths of the cables may make calibrations difficult

Two possibilities ~ In the water or outside of the water ~

Possible problems in running the cables to each photo sensor

b) weight of the cable is 100 ~ 200 g /m

-> 10 kg ~ 20 kg / 100m –> *Total 400 ~ 1000 tons*!

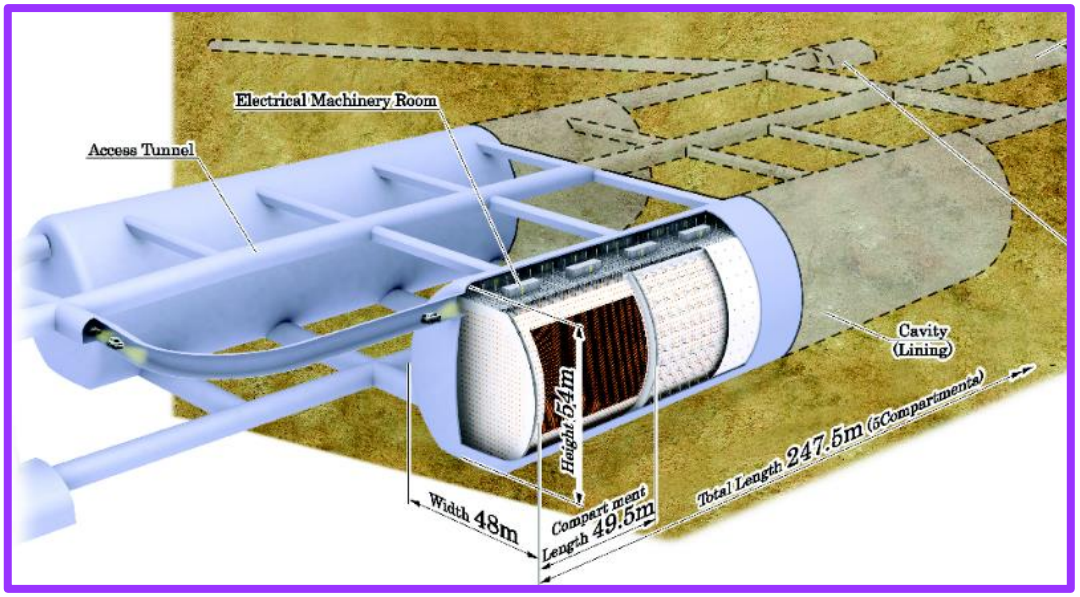
-> non negligible weight

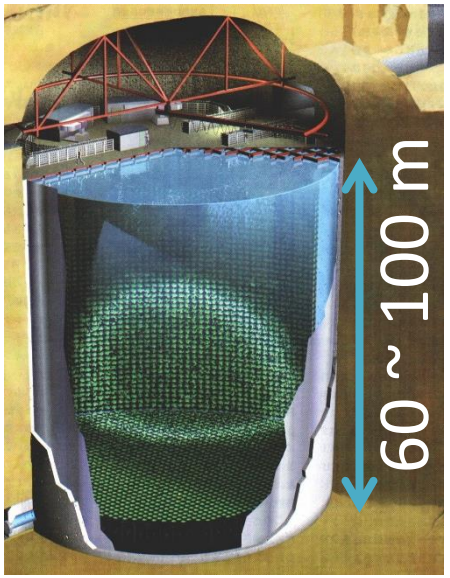
-> affect the design & cost of the structure

c) difficulties in construction (cabling)

-> detector shape dependent

but not easy even for SK-like shape.



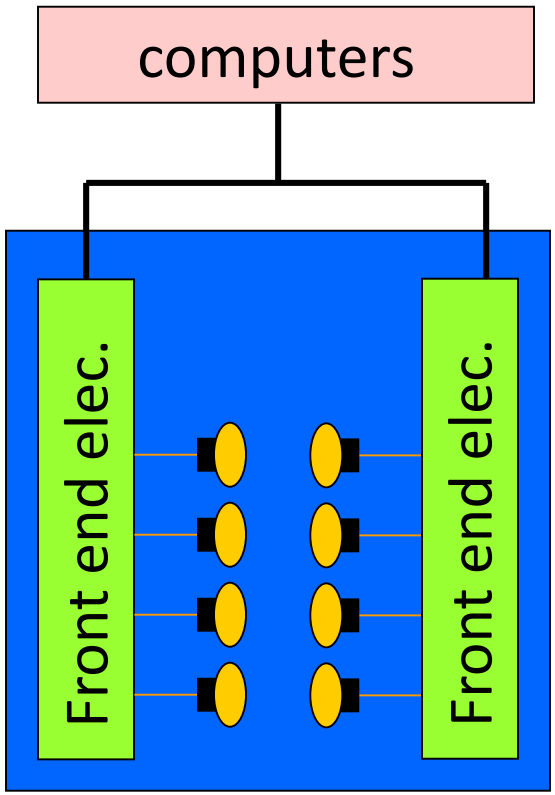


Two possibilities ~ In the water or outside of the water ~

Possible problems in running the cables to each photo sensor

a) Length of the cable
b) Weight of the cable
c) Difficulties in construction / cabling

☆ Several advantages to put front-end electronics modules closet to photo-sensors.



- Shorter length of the cables
  better signal quality
- Reduce the number of cables
  from the tank to the top floor.
  -> reduction of weight of the cable,
  and may be cost of structure.

Two possibilities ~ In the water or outside of the water ~

Of course, there are technical challenges (disadvantages)
to put front-end electronics in the water

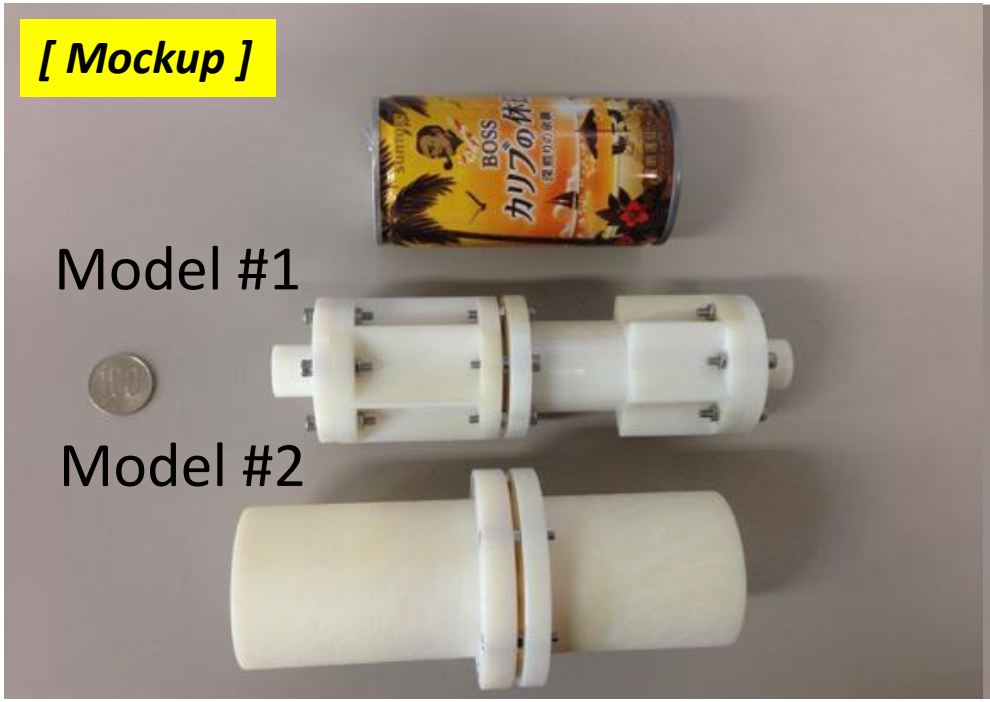
- Basically no way to fix or replace fault modules.
- Need special devices / designs
  water tight chassis, connectors
- Difficult to predict environment
  and difficult to make improvements.
  (electrical noise, grounding etc..)

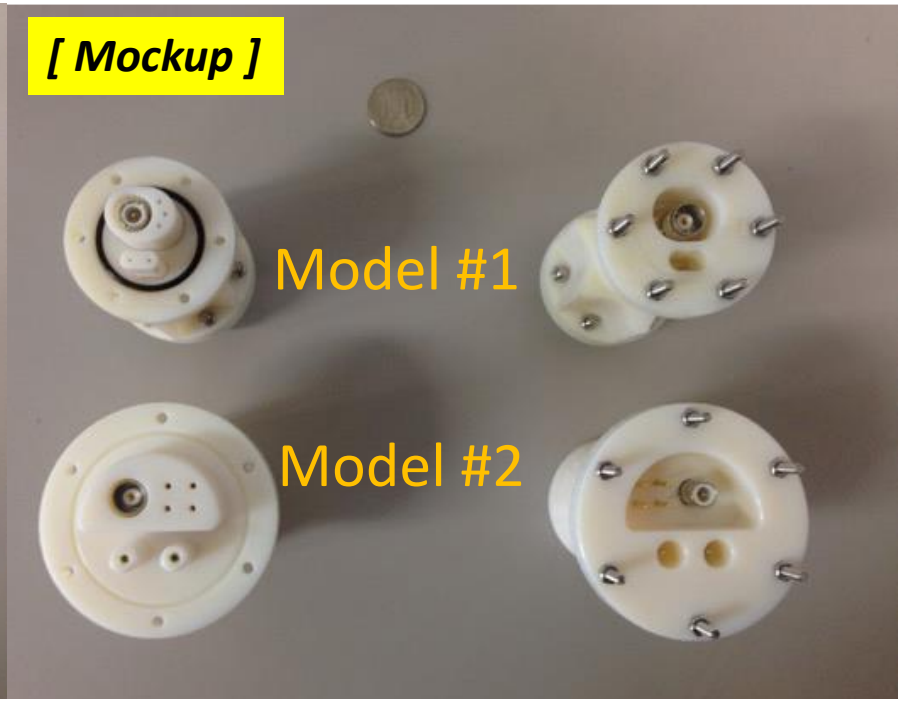
Necessary studies to put electronics in the water

1. Water tight, pressure tolerant connectors and chassis
2. Water tight, pressure tolerant cables
   (for data transfer and timing distributions)
3. Fault tolerance
4. **Long term stability (over 20 yrs)**

Water tight connectors

We have asked a company to design the water tight connector for HPD
(8KV, 8kV-Bias + signal + control lines)





Perform soak tests to select the material. (ongoing)

The company prepared a special connectors
to test the interference between the HV and the signal lines.

Also, test in vacuum environment. (May ~)

Water tight chassis

Suggested design (from one company)

SUS 316L (or 304) + Urethane seal

Thickness of the surface plates **~ 4mm**

Entire chassis is (better) to be filled with silicon or the other material (like R3600 PMT base)

Assuming 500mm x 500mm x 75mm (d = 4mm)

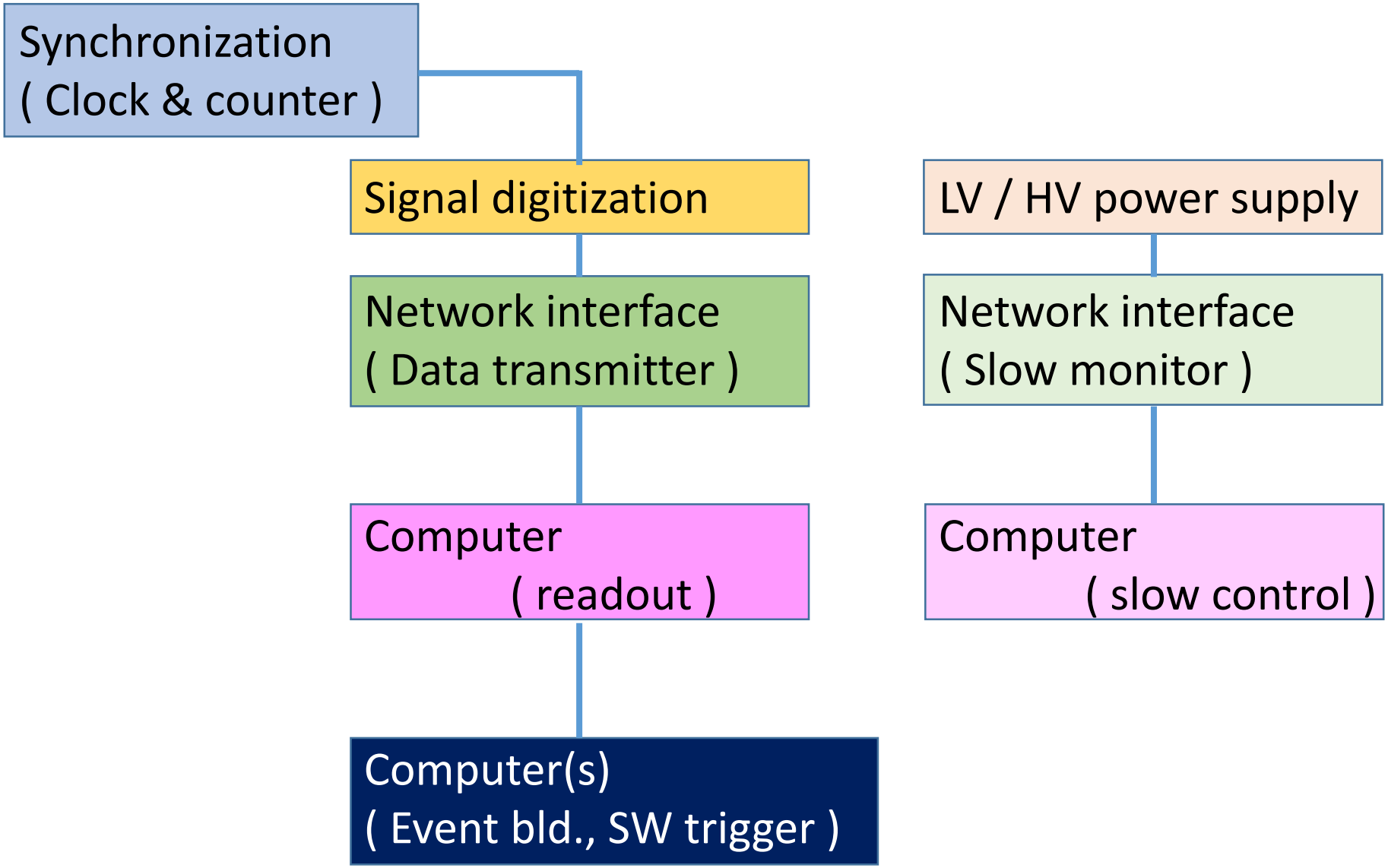
(VME 9U board : 360 mm x 340mm)

Chassis	~ 20 kg
Filler	~ 20 kg
Elec. components	~ 3 kg (?)
Total	***~ 43 kg !?***

This may be too heavy to handle, though…

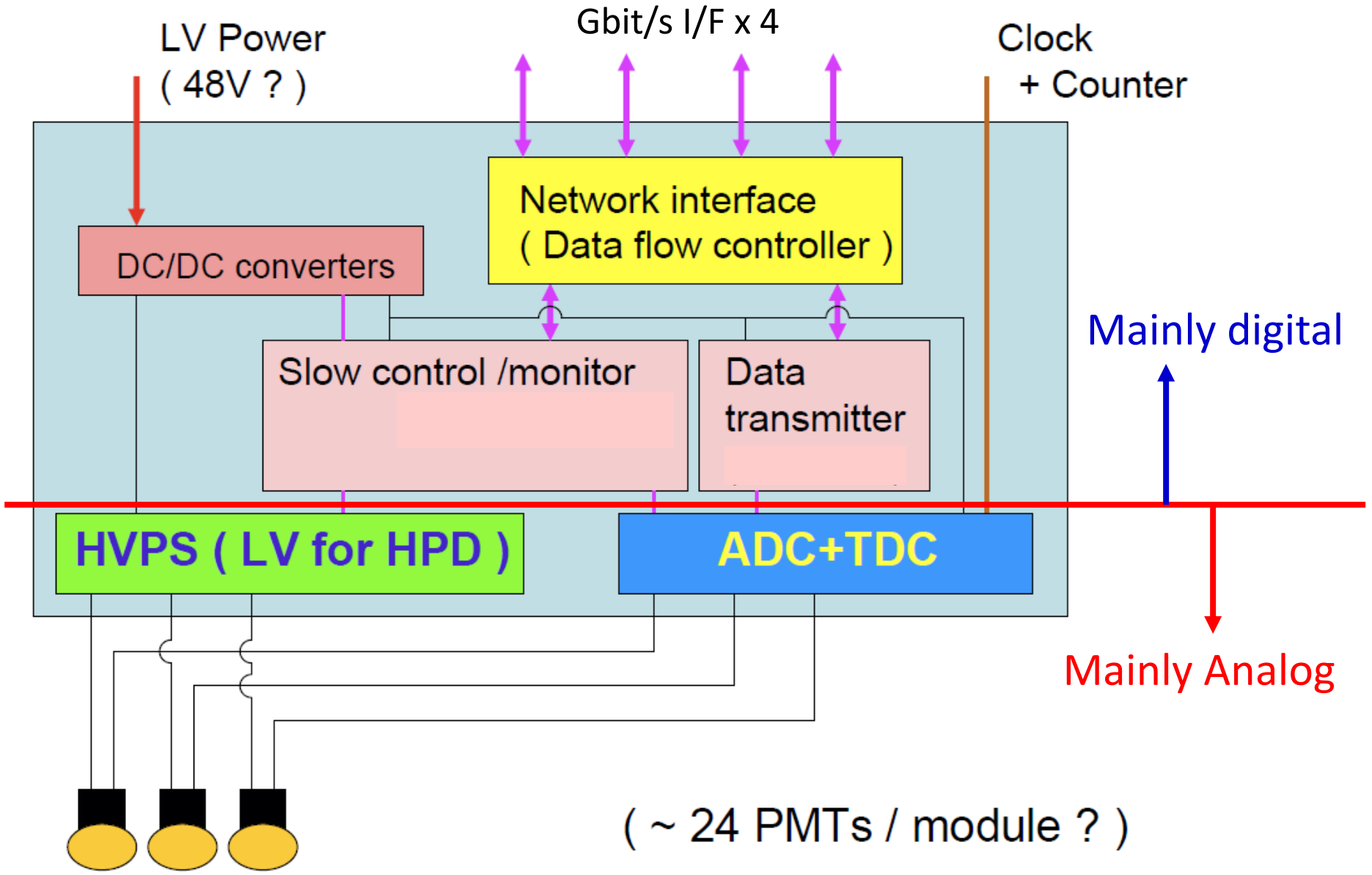
Realistic???

Components of the electronics / DAQ System

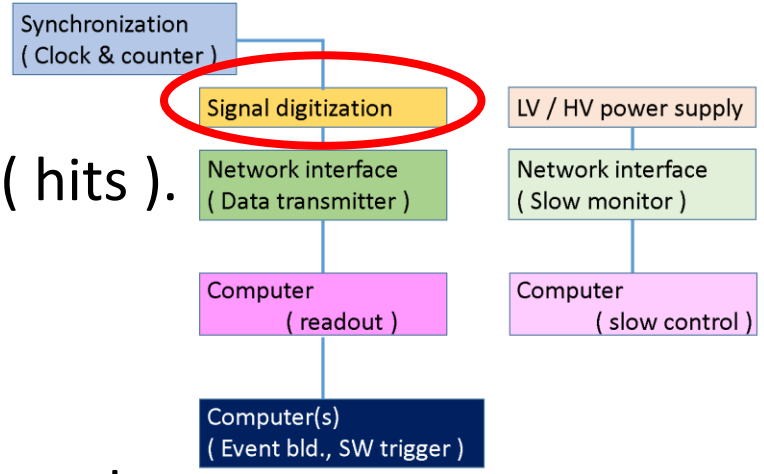


Components of the front-end electronics

Possible diagram for “in the water” solution



Signal digitization ~ requirements ~



- ***Dark noise*** dominates the input signal (hits).
  Expected dark rate is ***5 ~ 10 kHz***.

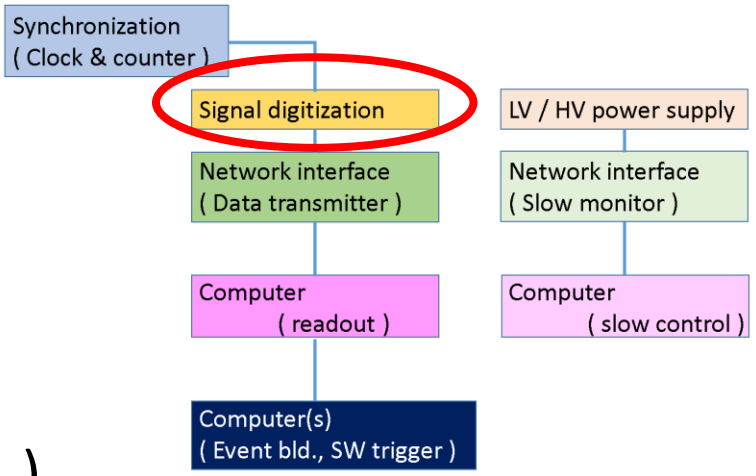
- ***Low occupancy for low energy events***.
  O(<1%) for typical solar neutrino events
  and background gamma-ray events.

- ***High energy event*** (mainly Cosmic ray muons) rate is rather low.
  Depend on the location of the detector but ***<< 100Hz***.

- Geometrical distribution of hit sensors for an event is rather broad.

- ***Possibility to have repeated hits in a channel is quite small.***
  After pulse from a photo sensor, signal reflections etc.
  O(1μs) of channel dead-time is acceptable.
- All the modules (TDCs) has to be synchronized.

Signal digitization ~ requirements ~

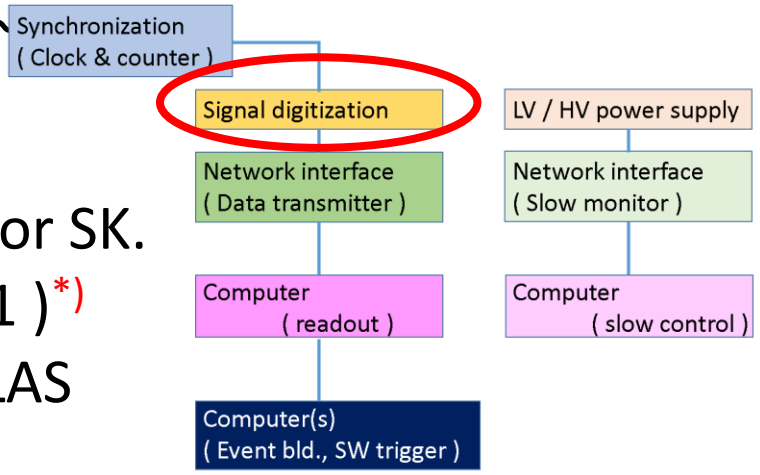


~ Some parameters ~

- Self triggering for each channel
- High Sensitivity for single p.e.
  - Discriminator threshold
    ~ ¼ p.e. *) (well below 1 p.e.)
- Processing speed/hit (channel dead-time)
  ~ 1 μsec / hit
- Charge dynamic range
  0.1 ~ 1250 p.e. (0.2 ~ 2500 pC)
- Charge resolution
  ~ 0.05p.e. (< 25 p.e.) in RMS
- Timing LSB
  ~ 0.52 ns
- Timing resolution
  0.3ns (@1 p.e.) in RMS
  0.2ns (> 5 p.e.) in RMS

*) QBEE : ¼ p.e. ~ 3 mV

Signal digitization ~ Possible designs ~



1) QTC + TDC

Similar to the current electronics for SK.

SK uses custom build QTC (CLC101)*)

and TDC developed for ATLAS

(AMT-3)

QTC has 3 channels in one chip.

Each channel has three ranges to cover wide dynamic range.

Different gains for different ranges

Outputs from all three ranges

are individually recorded by external TDC.

Process rule of QTC is CMOS 0.35 μm and

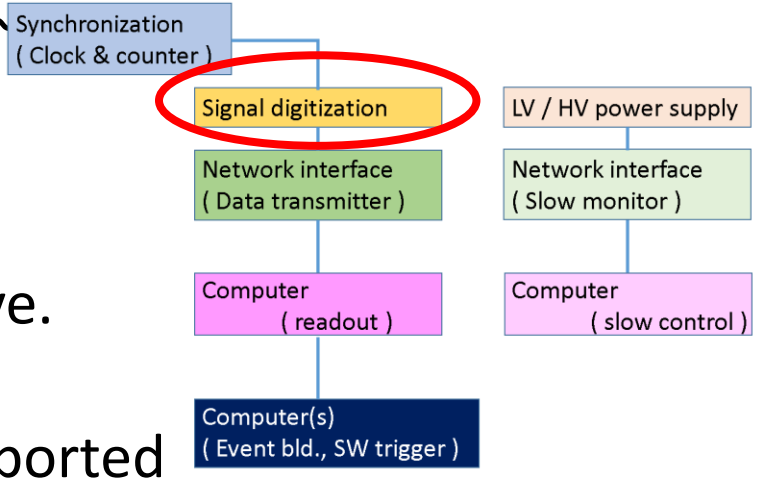
possible to reproduce the same chip ***at this moment***.

Est. price **@ ~ ¥ 6,000 / chip** for 100,000 chips

(¥ 2000 / channel)

(@ ~ ¥10,000 / chip for 1,000 chips)

Signal digitization ~ Possible designs ~



1) QTC + TDC

AMT3 has been discontinued
and need alternative.

-> FPGA based TDC is proposed.

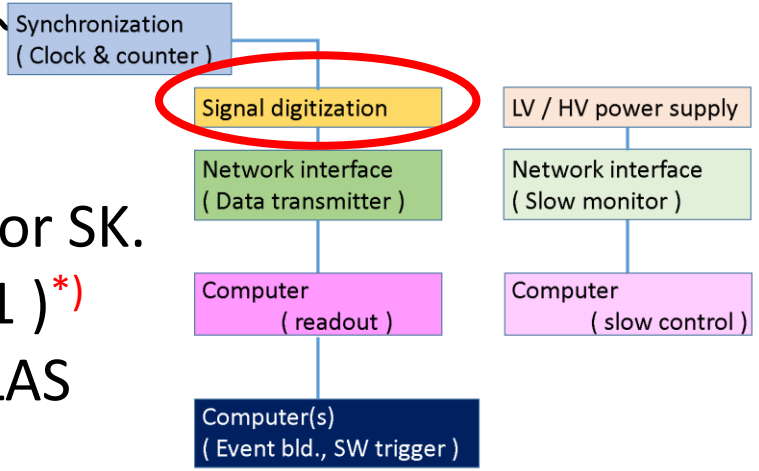
Recent low cost FPGA is reported
to have sufficient performance .

(FPGA-based "Wave Union" TDC
by Jin-Yuan Wu, Fermilab)

32 ch. TDC was implemented in *$75 FPGA* chip.
Only 56% of the logic elements in CYCLONE III
(EP3C25F324C6N) were used.

Estimated costs of ***these two core components***:
Assuming 24 ch. / board,
8 QTCs + 4 FPGAs (32ch.) are necessary.
~ ¥5,000 / channel for 100k sensors.

Signal digitization ~ Possible designs ~



1) QTC + TDC

Similar to the current electronics for SK.

SK uses custom build QTC (CLC101)*)

and TDC developed for ATLAS

(AMT-3)

Current status

QTC test board (2 QTCs = 6 ch inputs) was designed

and produced a few boards. (FNAL/BU)

Digital I/F (connector)

on this board is compatible

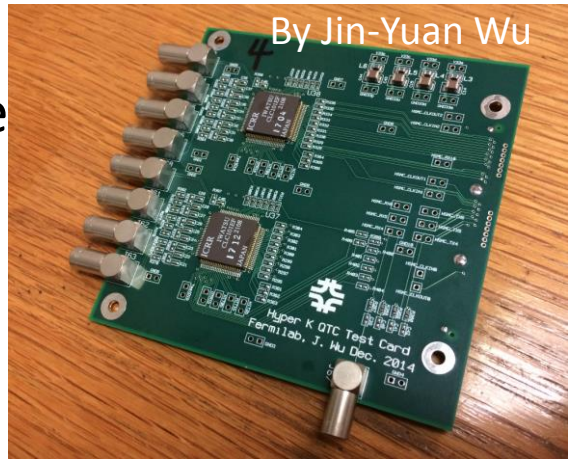
with ALTERA CYCLONE III

evaluation board.

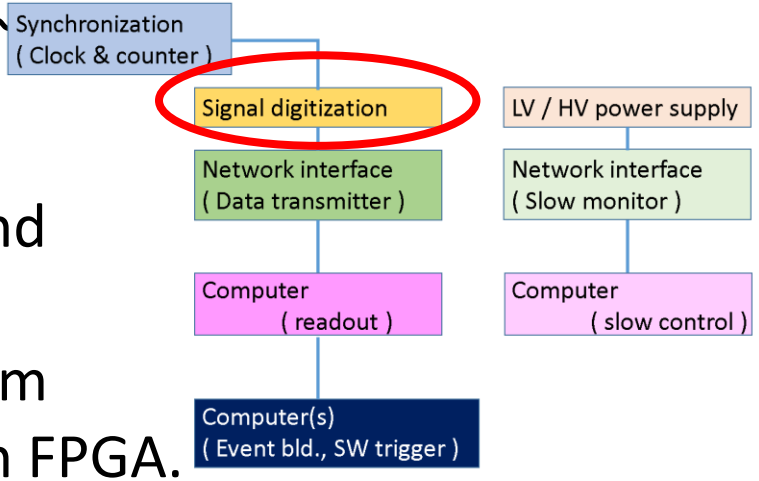
We need to evaluate

the performance of TDC

together with QTC in this year.

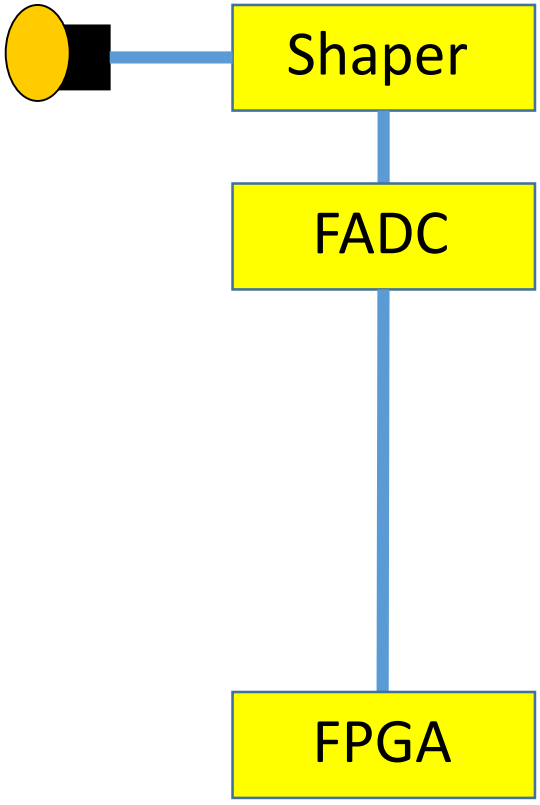


Signal digitization ~ Possible designs ~



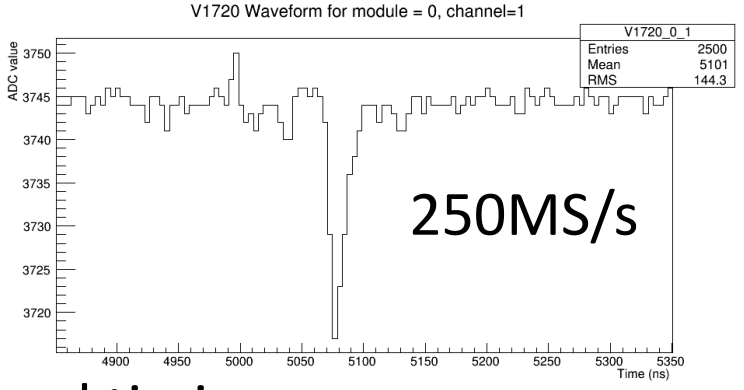
2) Shaper + FADC (+ FPGA)

Another proposal to use shaper and FADC to record waveform and process the digitized wave form with FPGA.



Sampling frequency 100 ~ 500MHz

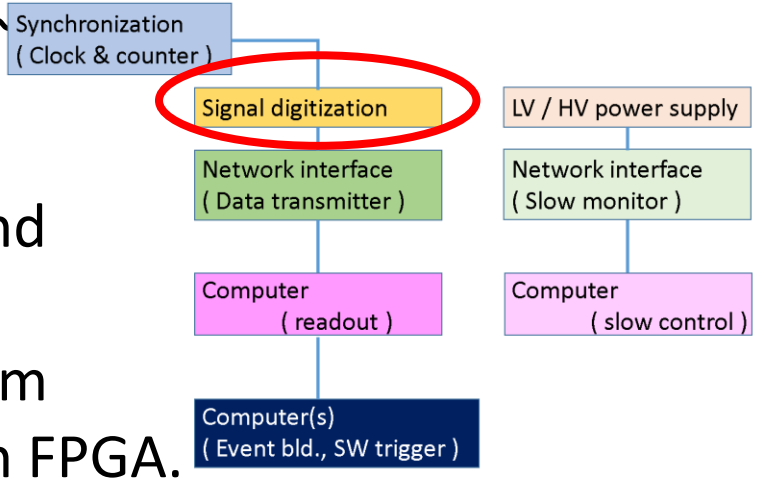
resolution 12 ~ 14 bits



Fit signal timing

Integrate charge

Signal digitization ~ Possible designs ~

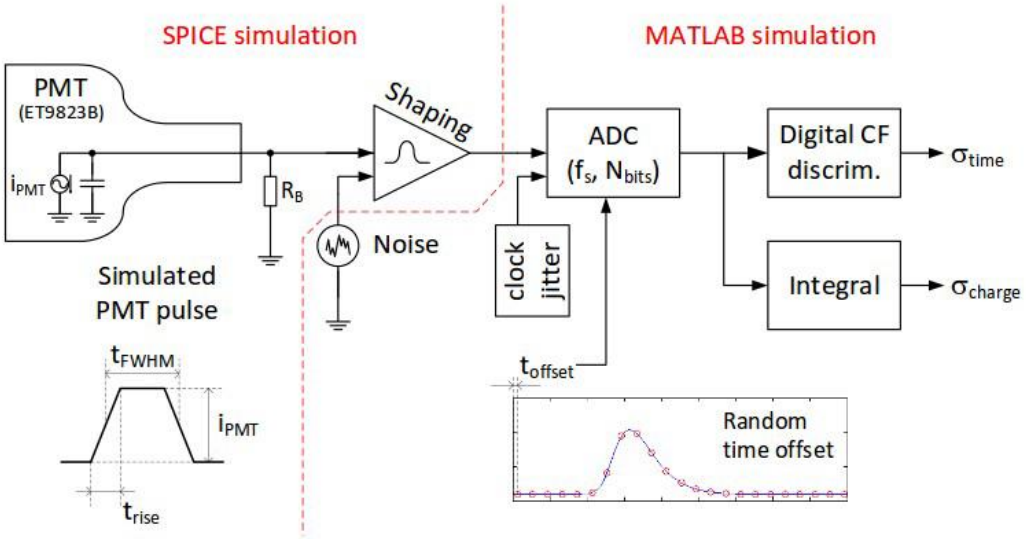


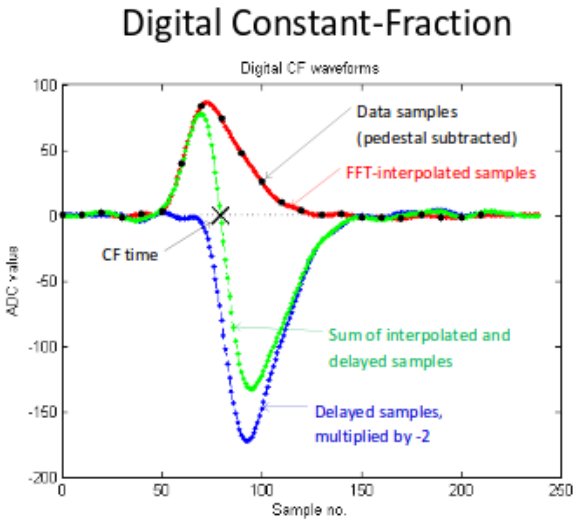
2) Shaper + FADC (+ FPGA)

Another proposal to use shaper and FADC to record waveform and process the digitized wave form with FPGA.

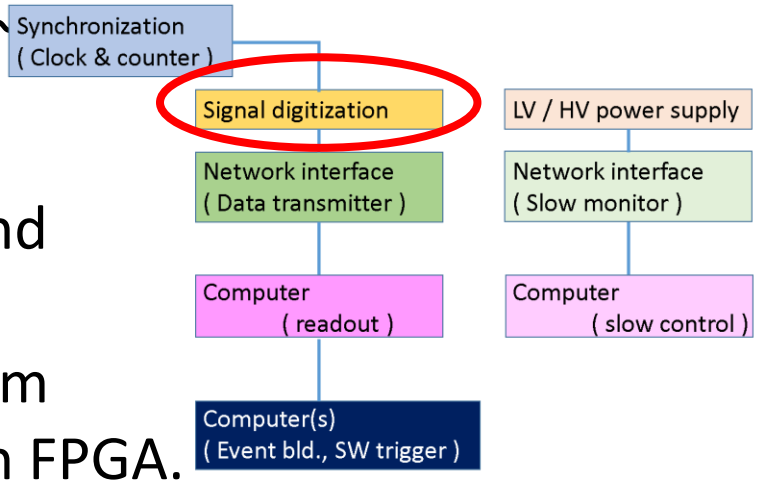
Current status

Searched for the possible combinations of shapers and FADC based on the simulation





Signal digitization ~ Possible designs ~



2) Shaper + FADC (+ FPGA)

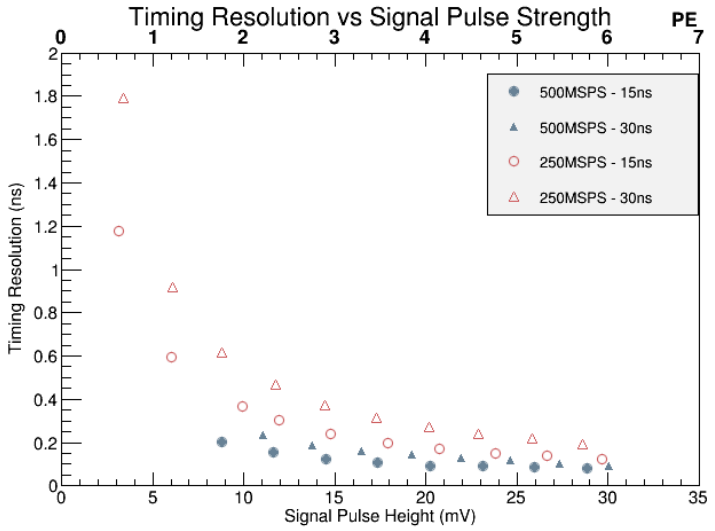
Another proposal to use shaper and FADC to record waveform and process the digitized wave form with FPGA.

Current status

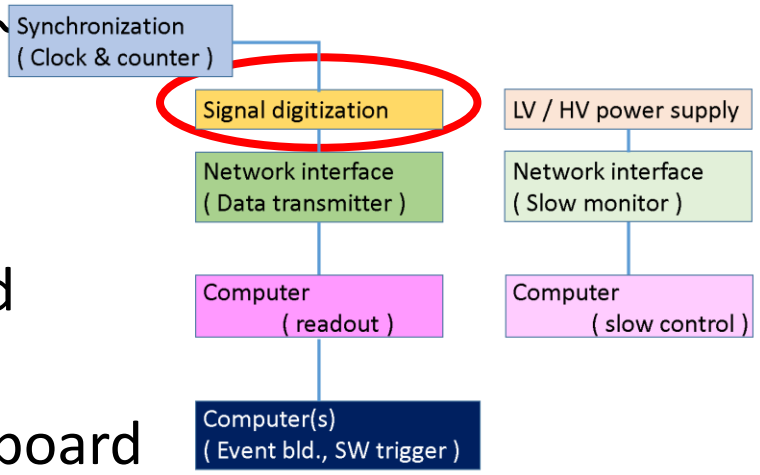
Evaluating the selected combination with arbitrary waveform generator

Preliminary result

T resolution vs charge



Signal digitization ~ Remaining tasks ~



There are a lot of things to be done.

1) QTC + TDC

Evaluate QTC + FPGA board

(Feasibility check)

Design of the 2nd QTC test board

2) FADC + FPGA

Various studies to select components

Timing resolution

Charge resolution

Dynamic range (how to handle ?)

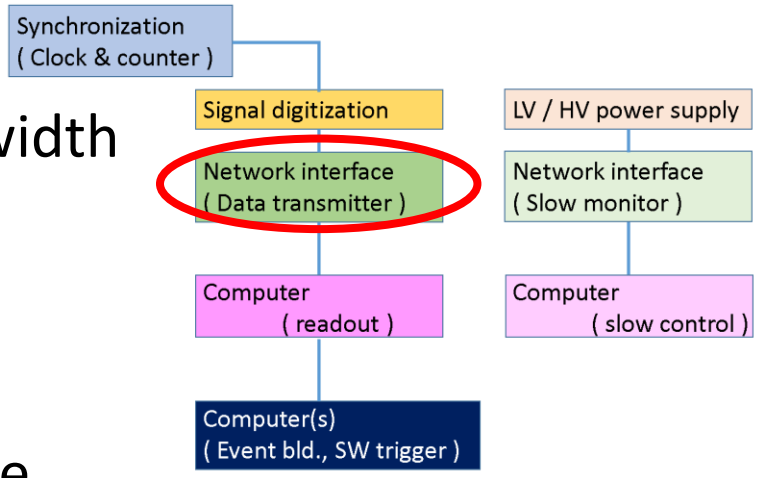
Design of the evaluation board

Realistic estimation of the cost

N) Alternative solutions?

If you are interested in either design or alternative solutions, please let me know.

Network interface



0) Expected data rate and required bandwidth

Assumption

24 channels / board

6 bytes / hits

10kHz photo sensor dark rate

Nominal data rate

10 kHz x 6 bytes = 60 kBytes/s/channel

-> 24 channels * 60 kBytes/s = ***1.5 MBytes/s***

Considering fluctuation

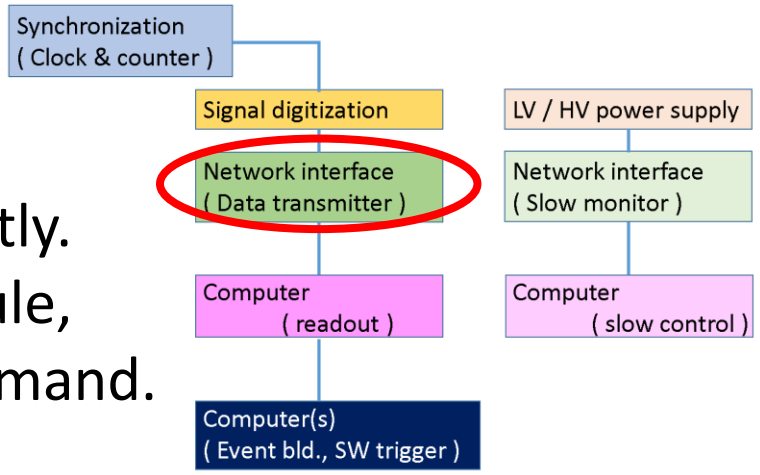
(high dark rate tube > 100 kHz)

If there are two high rate tubes (@ 100 kHz)

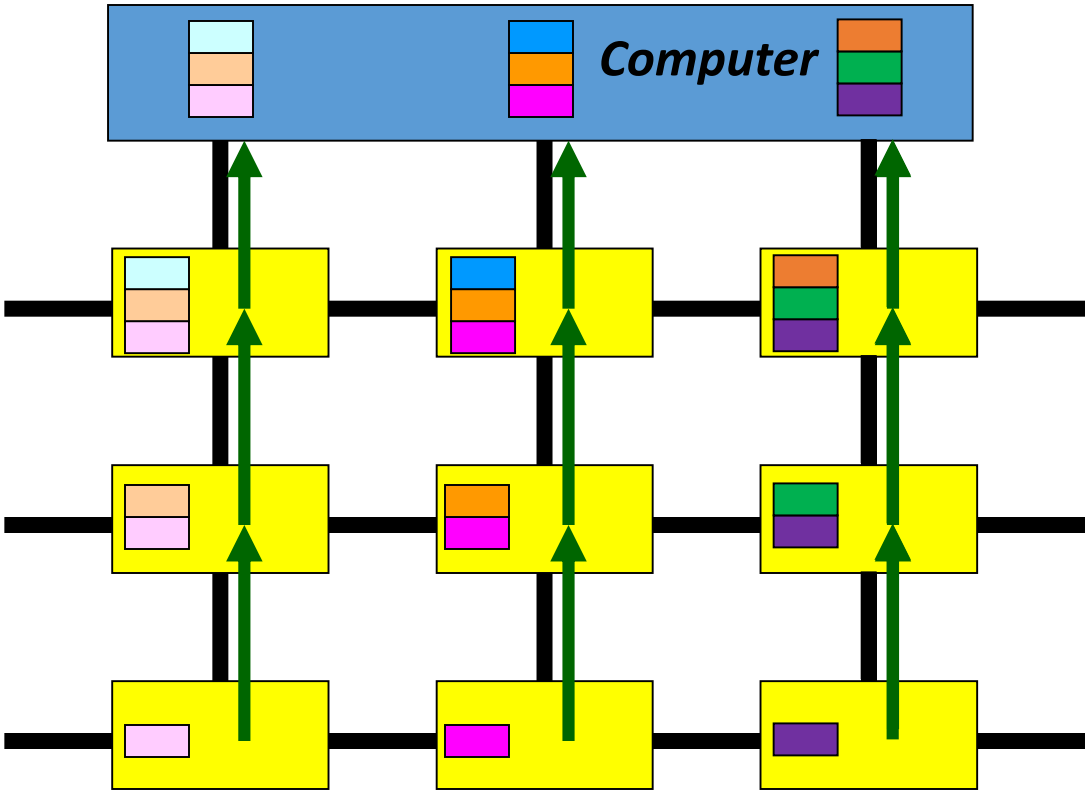
100kHz x 6 bytes * 2 channels = 1.2 MBytes / s

→ ***~2.5 MBytes/s/board*** seems to be sufficient under normal situation

Network interface ~ connections ~

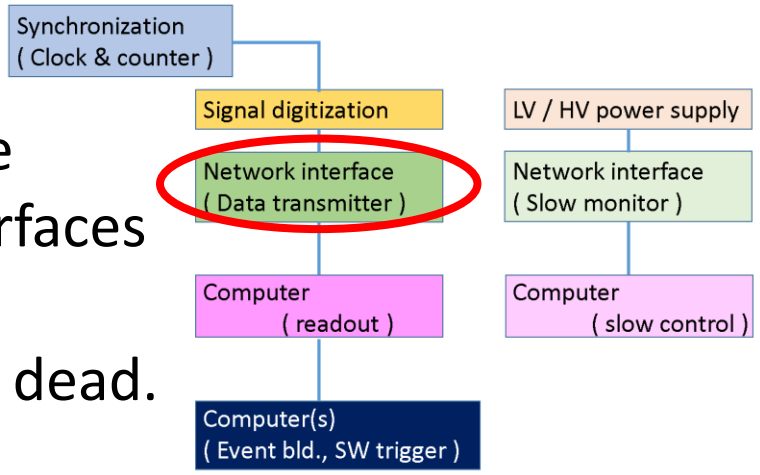


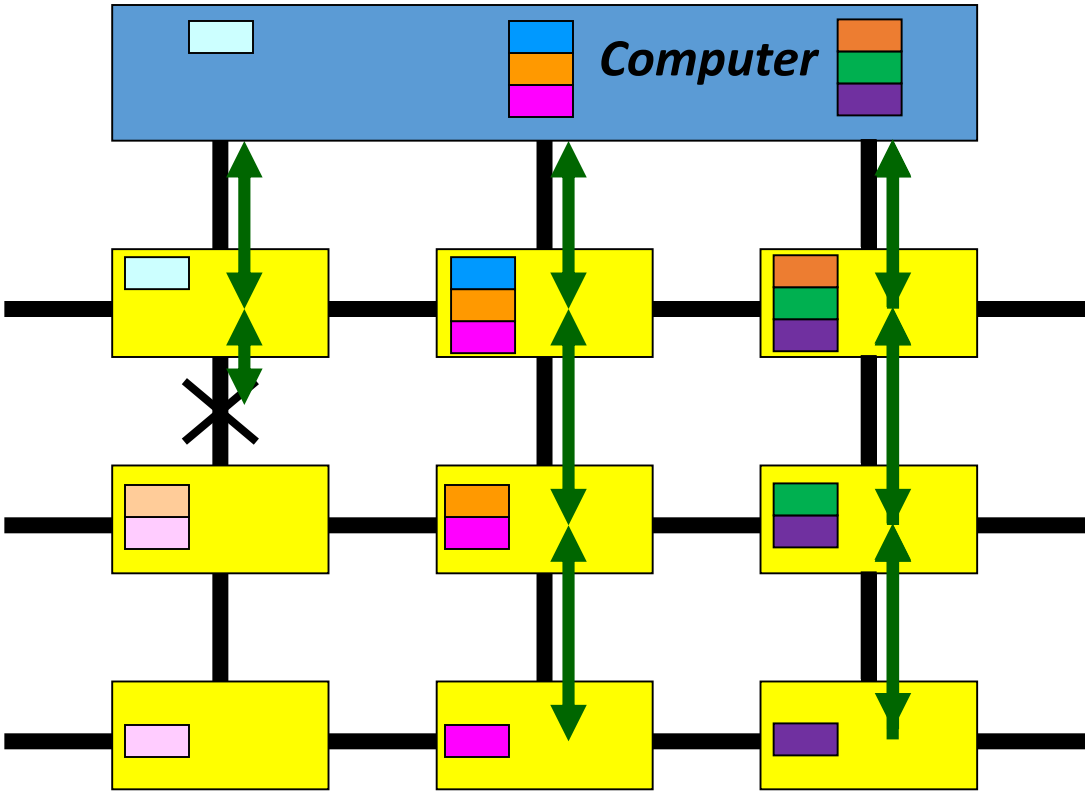
- Top modules communicate with the computer directly.
- If the command is for the other module, forward the command.
- Each module sends data to one of the neighbor module. (Usually, upside)
- Transmit received data with its own data.



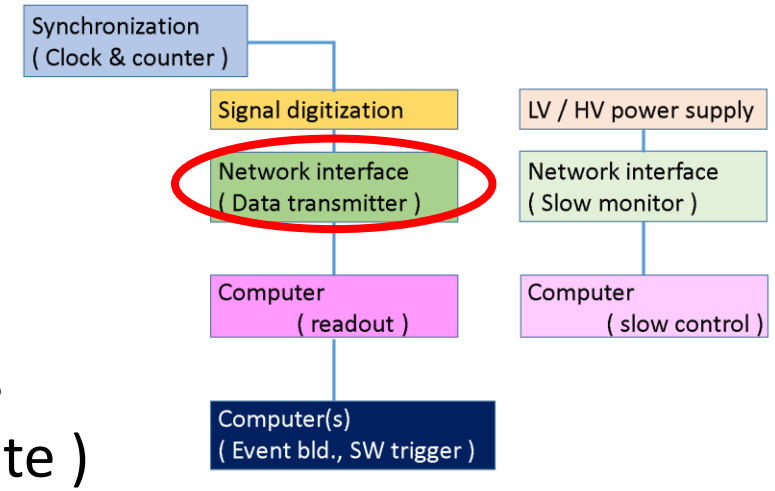
Network interface ~ connections ~

- Need to prepare the recovery scheme
  when some of the network interfaces
  are down
  or one of the modules is dead.





Network interface ~ connections ~



- In failure mode,
  send appropriate command
  from the computer
  to the relevant modules
  and reconfigure (re-route)
  the network paths.

- Need sufficient bandwidth
  at least twice
  of the maximum rate .

Expected data rate / board

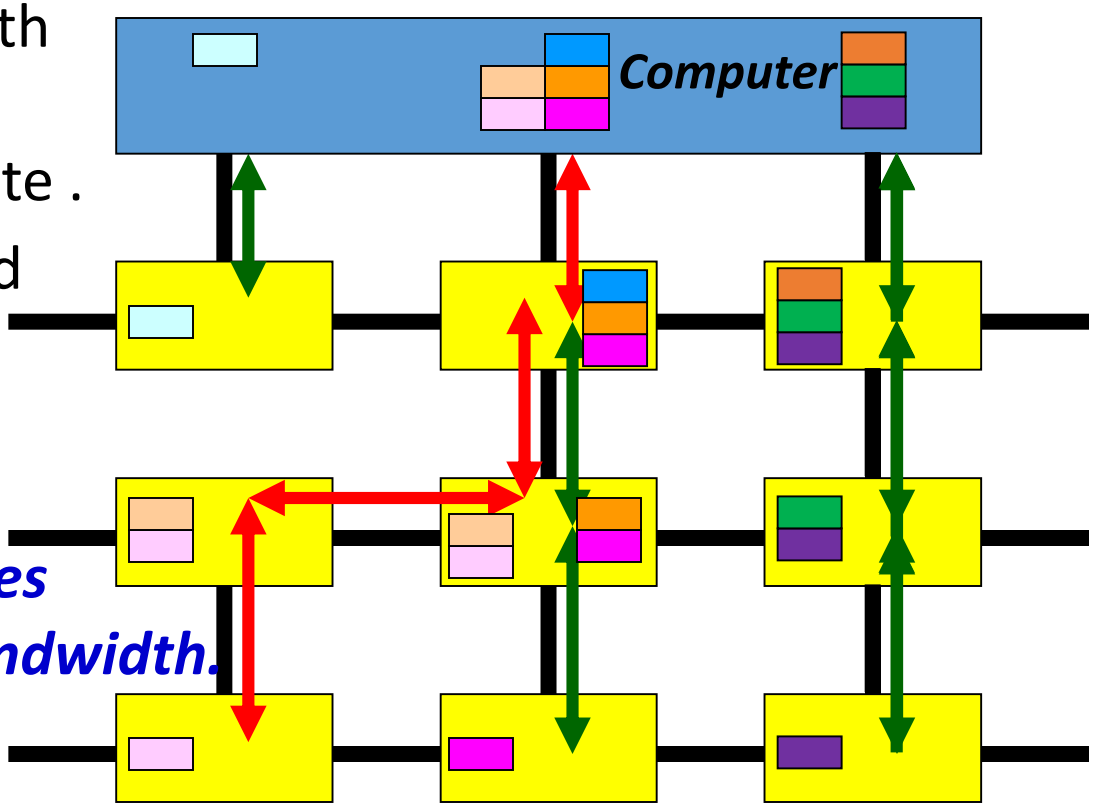
2.5 MBytes / sec

~ 20 Mbits/sec

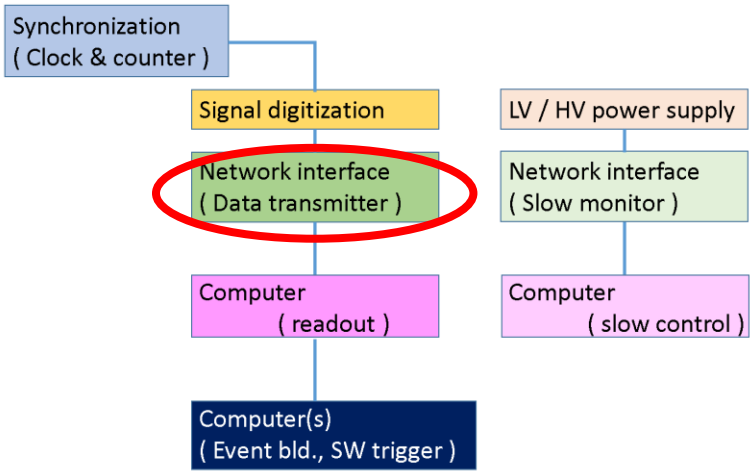
Nominal configuration

10 ~ 15 modules in series

with Gigabit/s bandwidth.



Network interface



1) Protocol

Gigabit Ethernet

(TCP/IP, UDP/IP, …)

Rocket IO

Rapid IO etc…

a) Gigabit Ethernet

Portable and easy to communicate with computers

~ easy to test and debug.

Some overhead (depend on the implementation)

Various implementations

Native implementation (SiTCP etc.)

SiTCP has been used in SK.

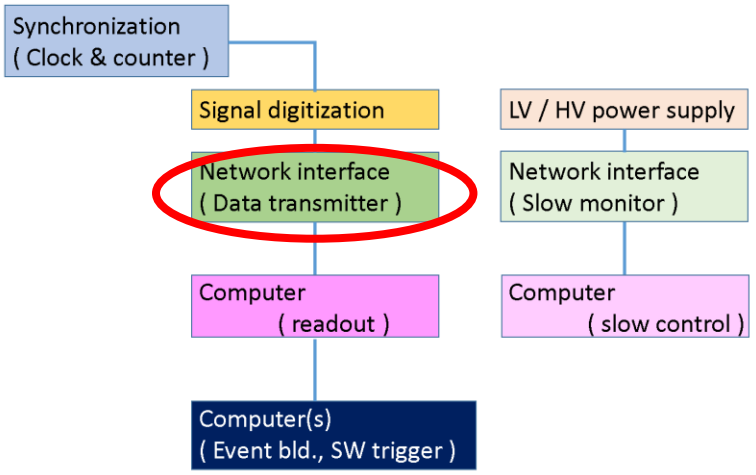
Possible to use ~ 95 % of bandwidth

CPU based implementations (Nios, MicroBlaze etc.)

Network interface

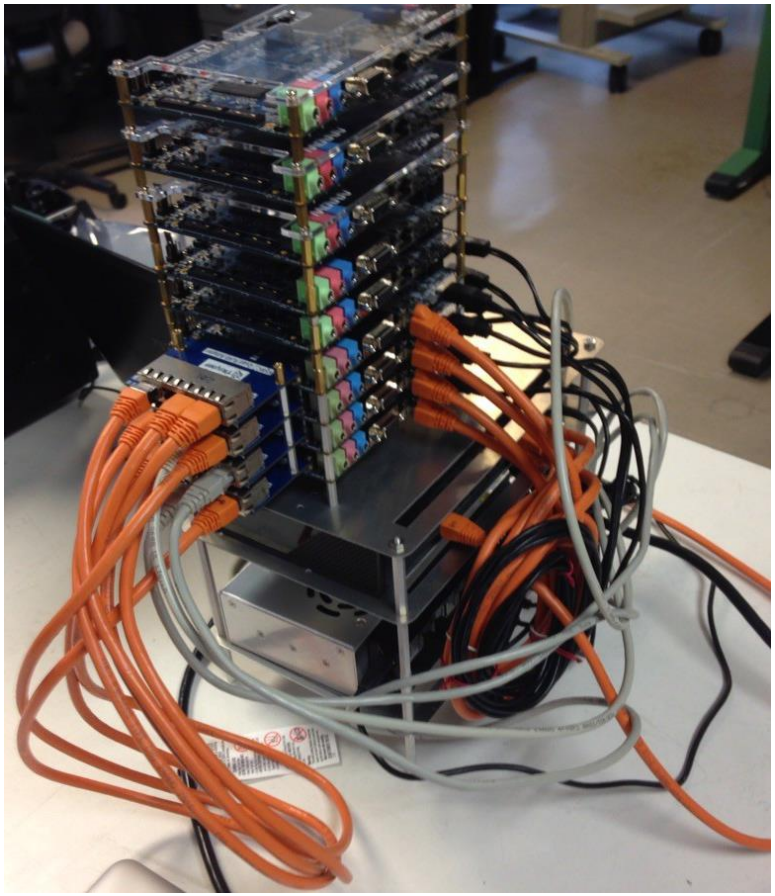
1) Protocol

Gigabit Ethernet
(TCP/IP, UDP/IP, …)
Rapid IO
Rocket IO etc…

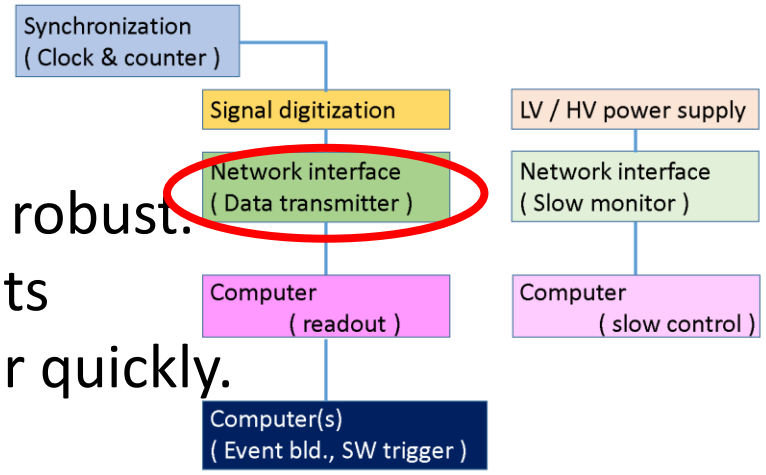


b) Rapid IO

Simple protocol
PCI-e I/F board is available.
Testing with evaluation board
(Soc Kit) in Triumf.
At this moment,
~ 550 Mb/s is achieved.
(using UTP cable)



Network interface



2) Connections : Optical or Electrical

Electrical connection seems to be robust.

Recent high speed optical elements
tend to be degraded rather quickly.

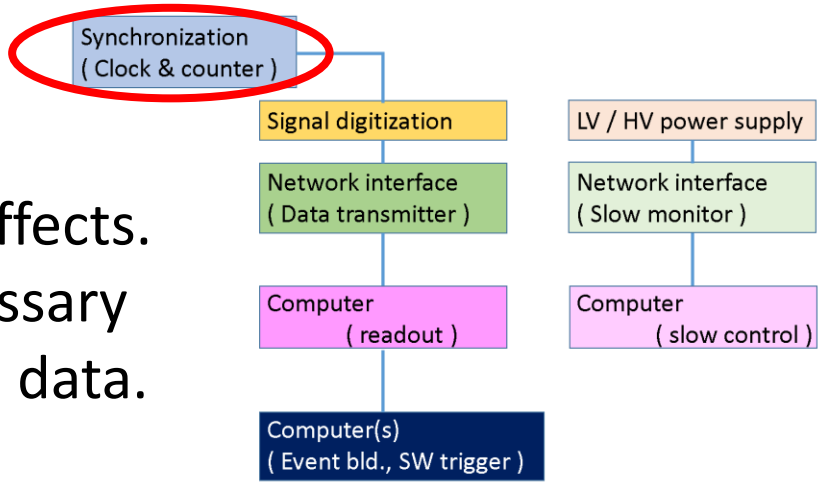
Especially, compact modules are easy to degrade.
(MTBFs are rather long but these numbers
do not take into account aging...)

Connectors may be simpler for optical fibers.
(Need careful handling of the fibers, though.)

Normal Ethernet cables are not pressure tolerant.

(Same discussions apply
for the timing / counter distributions)

Clock and counter distributions



Need to synchronize all the modules
in order to avoid quantization effects.
Also, global counter (~ 32 bits) is necessary
to be distributed to synchronize data.

Distribution method

a) White rabbit (normal UTP cable)

b) Custom using nano/zero-skew UTP cable (SK)

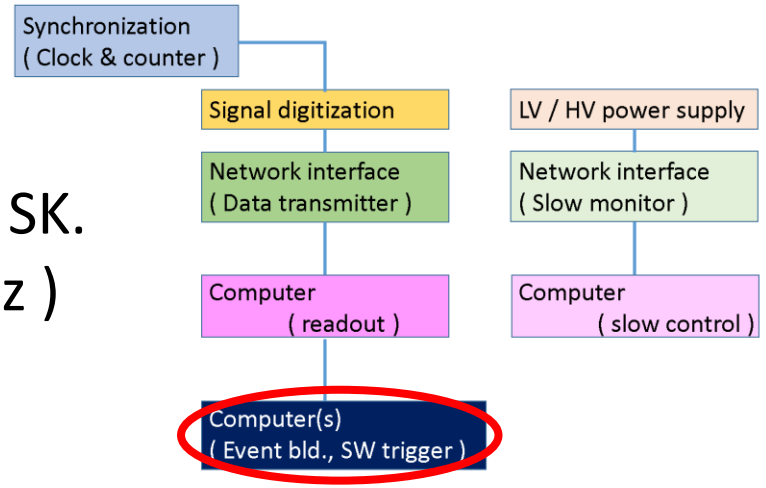
c) Optical fiber (usually, single mode)

various implementation (different encodings)

1) J-PARC beamline

2) K2K/T2K

Computer system ~ frontend ~



Front-end T/Q information readout

No problem in 30 boards / PC in SK.

(Dark rate ~ 5 kHz)

Even with ~ 10kHz dark rate,

I don't see any problem.

960 boards / PC may be possible.

-> # of front-end PCs ~ # of sensors / (720 or 960)

# of sensors / compartment (or detector)

for all proposed designs < 25,000 (ID + OD)

Each computer need to have at least

1 Gigabit/s input I/F x 4 sets

10 GbE I/F for output

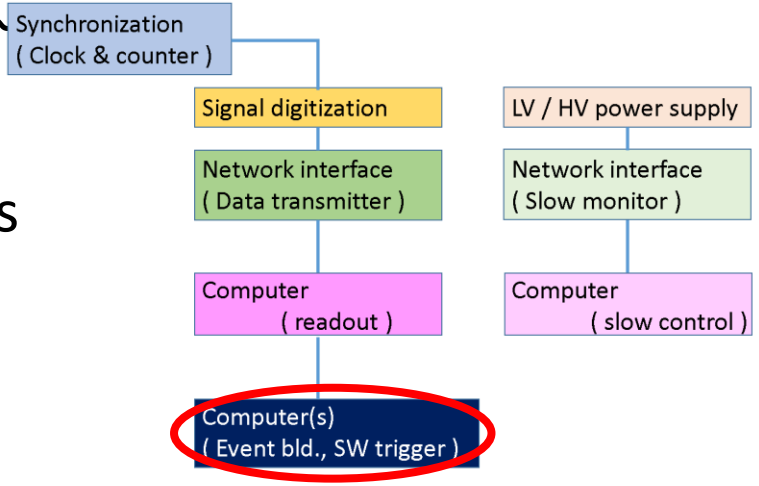
Clock / counter information handler (1 PC)

GPS information readout (1 PC)

→ *In total **35 ~ 45 PCs** are necessary*

for 1 compartment (or detector) readout.

Computer system ~ software trigger ~



Software trigger

~ depend on the detector characteristics

i.e. γ from radio activities in detector material, surrounding rock and water.

Currently, ***6 machines*** are used in SK for combining data and applying software trigger.

In total ***48 processes*** are running in parallel

6 machines x 8 processes.

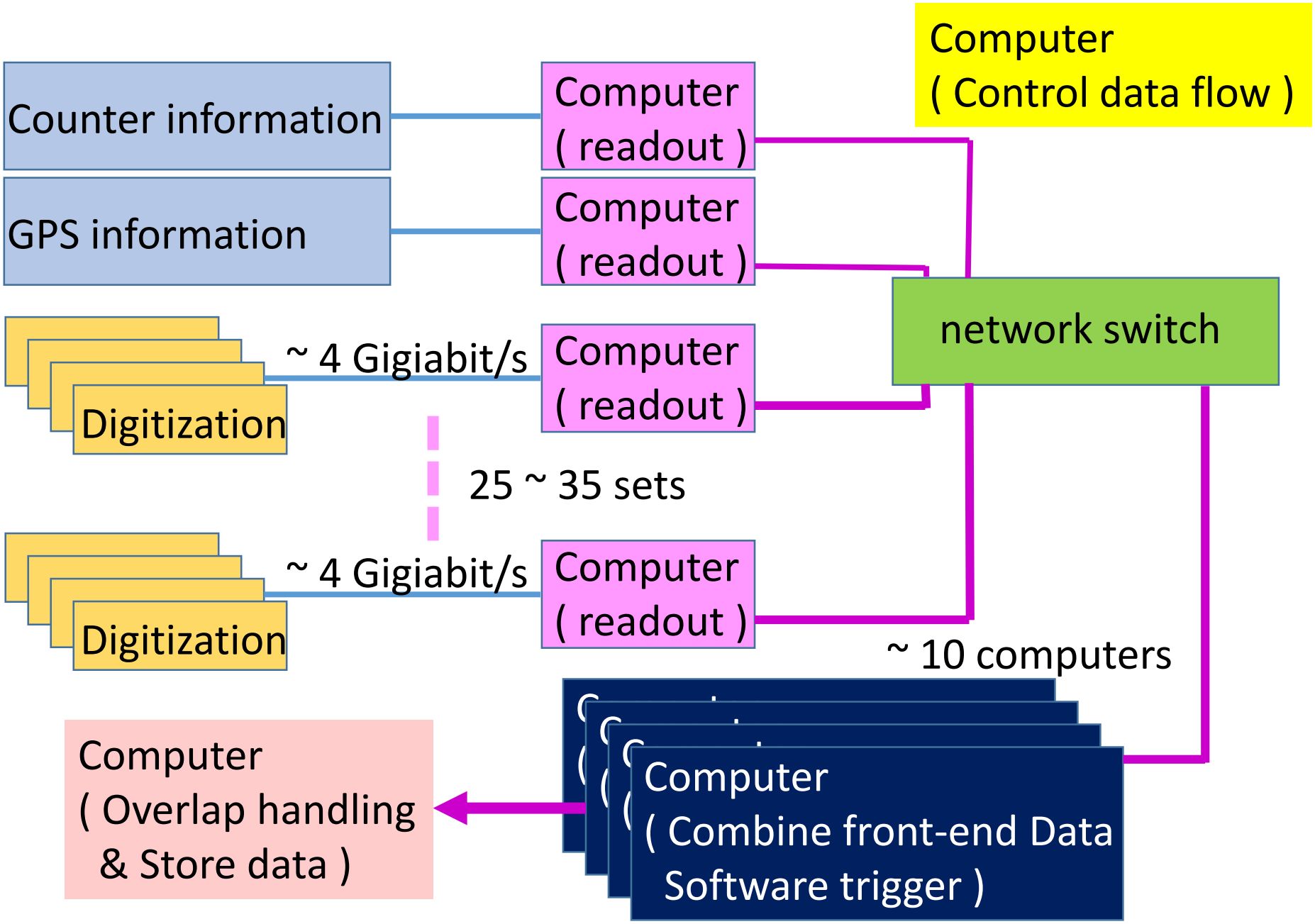
Each machine has 6 cores x 2 CPUs (Xeon 3 GHz)

With this configuration, *no problem in handling 11 kHz* for lowest energy trigger (31 hits in 200ns)

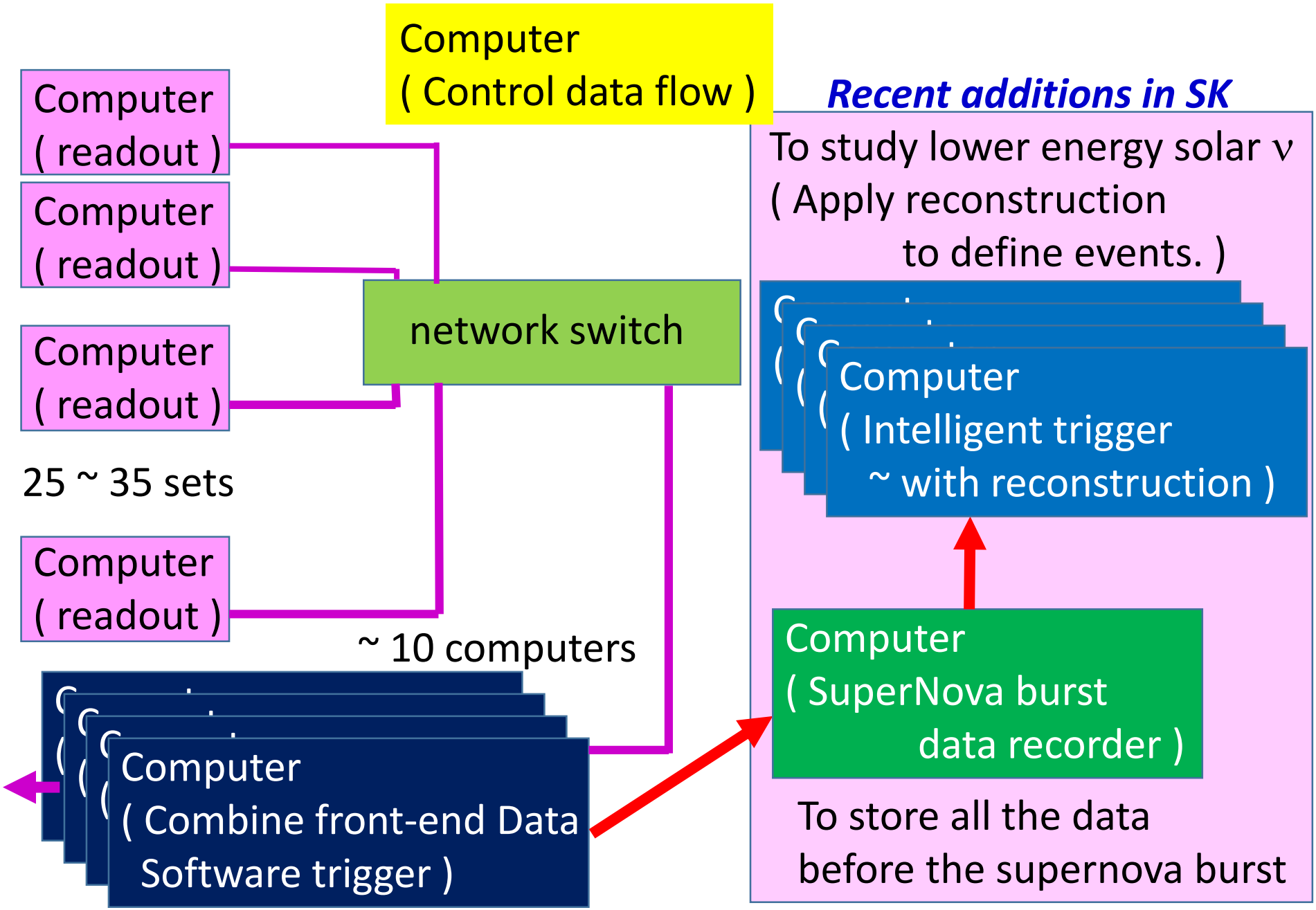
Actually, current bottleneck is the other process to eliminate overlaps.

(Data are distributed with some overlap intentionally.)

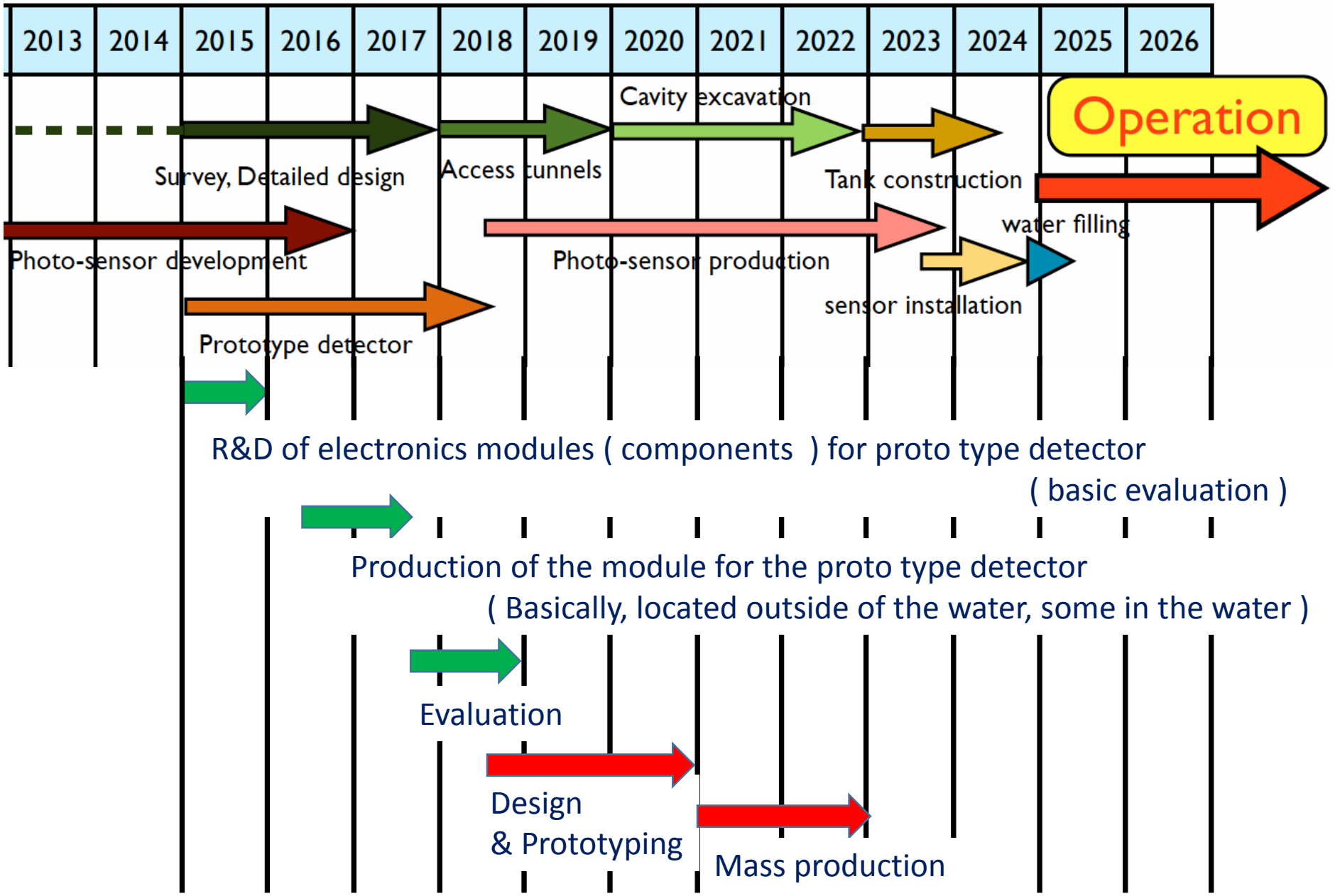
Computer system ~ rough and conceptual ~



Computer system ~ additional system in SK ~



Timeline


2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
Cavity excavation
Operation
Survey, Detailed design
Access tunnels
Tank construction
water filling
Photo-sensor development
Photo-sensor production
sensor installation
Prototype detector
R&D of electronics modules (components) for proto type detector
(basic evaluation)
Production of the module for the proto type detector
(Basically, located outside of the water, some in the water)
Evaluation
Design
& Prototyping
Mass production

List of major R&D items

Connectors, cables and chassis
- Water tolerant connector (for signal & HV/LV)
- Water tolerant connector (data transfer)
- Pressure tolerant cable (for data transfer)
- Water tolerant chassis (realistic one)

Evaluation of QTC + FPGA-based TDC

Evaluation of FADC + FPGA

Evaluation of data transfer system
- with SiTCP, Rapid I/O and possible other solutions

Slow control system
- not discussed this time (Need decision on sensor)

Reliability tests (method, environment and tools)

	Option 1	Option 2	Option 3
Water tank size	H: 100m, D: 69m	H: 80m, D: 64m	H: 60m, D: 74m
# of tanks	2	3	3
Water volume	747.9 kton	772.1 kton	774.2 kton
Fiducial volume	568.7 kton	565.2 kton	561.0 kton
ID surface	52795.5 m^2	60282.4 m^2	60188.1 m^2
# of PDs (ID)	50cm : 35,196 30cm : 105,590	50cm : 40,188 30cm : 120,564	50cm : 40,125 30cm : 120,375
# of PDs (OD)	17,598	20,094	20,061
Excavation vol.	868k m^3 ?	915k m^3 ?	968k m^3 ?