RD50 participation in HV-CMOS submissions

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Purpose

- There are on-going submissions to make large monolithic sensors in HV-CMOS processes, e.g. by ATLAS pixel and strip projects.
- Some of the submissions are being done as Engineering Runs, which allows to use non-standard wafer resistivity, e.g. 4 values between ~20 Ωcm and ~2 kΩcm.
- RD50 could start participating in such submissions by adding dedicated structures to investigate radiation hardness of silicon for these resistivities.

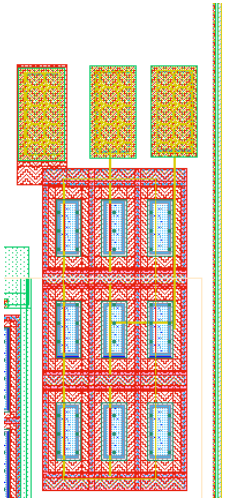
On-going Submissions

- There was an intention to participate in a run this spring with CHESS-2 (ATLAS strips).
  - Interested groups: CERN, Ljubljana, Liverpool, Oxford, Santa Cruz, Glasgow, IFAE Barcelona…
  - The run structure (reticle composition) evolved.
  - The submission is now planned for July.
  - Will include some test structures (next slides).
- The current intention is to use 1 cm^2 area in September run for dedicated RD50 investigations.
- => Please voice your interest and propose structures!

CHESS-2 Examples: Bulk properties

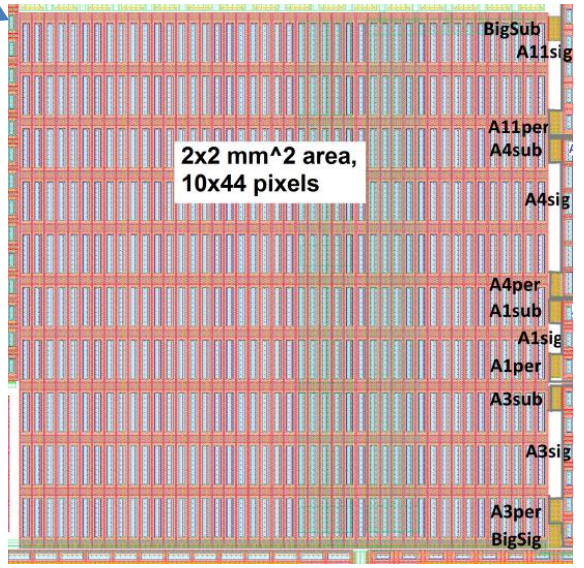
A variation of structures used in CHESS-1 submission, which are relevant for high-ρ substrates:

- **Passive pixel array near edge → for Laser-TCT studies** (presentations from Ljubljana)
- **Large passive pixel array → for CCE studies with a source** (presentations from Ljubljana)
- (possibly) **"pad device" → CV meas**.



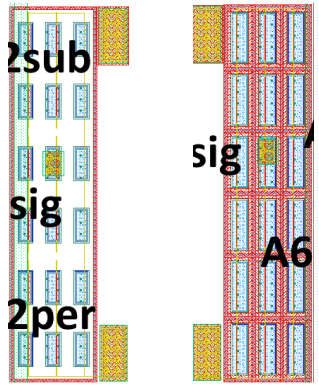
The main goal for including these structures is to investigate the bulk properties in a new resistivity range: *depletion & CCE vs fluence*.

- Our usual high-ρ (~ 3-6 kΩcm) has been studied well.
- First studies of low-ρ (~ 20 Ωcm) have been obtained. Non-trivial phenomena have been seen. More measurements to follow.
- → Now we get to investigate 3 intermediate resistivities to choose the best (least variation or highest minimal CCE vs fluence)



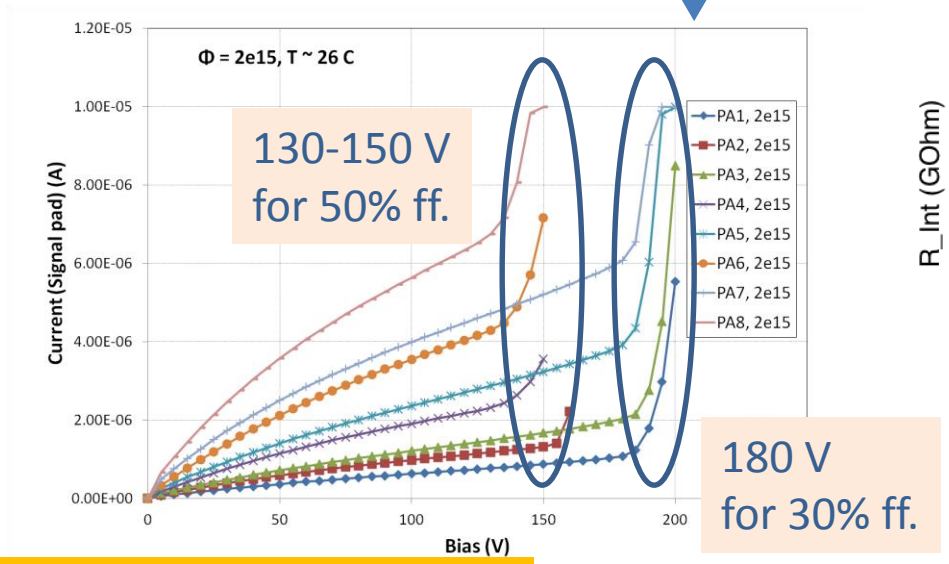
CHESS-2 Examples: Surface properties

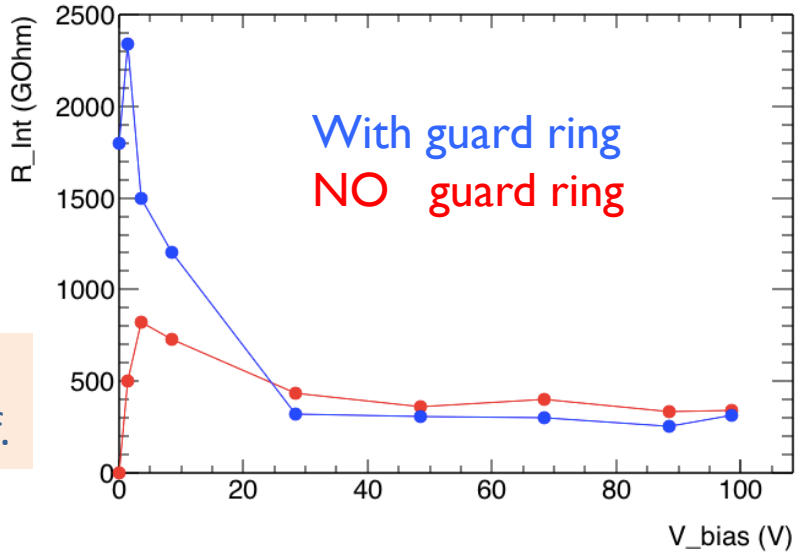
- **Pixel structures with and without "guard rings" → inter-pixel isolation**
- **Similar investigation of V(bd):** Typically rises with fluence. But seems to be stable with top-side biasing due to voltage drop along finite/small distances.
- Transistors, R, C.
- Electronics (0.35 μm): latch-up structures, amplifiers, etc.



NO guard ring

With guard ring





Data from I. Mandic (neutrons).
→ Same V(bd) at 5e15 neq/cm^2

RD50 structures

- The September run:
  - Have 1 cm^2 area to use
  - Multiple resistivities
- Would like to implement strip sensors:
  - In-situ amplification to be able to study the low signal levels present in case of low ρ values.
  - Omission of metal at the end of strips to enable laser scans.
  - → Studies of CCE, depletion, R(inter-strip)
  - → Field distribution with top and back biasing
- Please indicate your interest and propose your structures.