Silicon-on-Sapphire (SOS) Technology and the Link-on-Chip Design for LAr Front-end Readout

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Outline

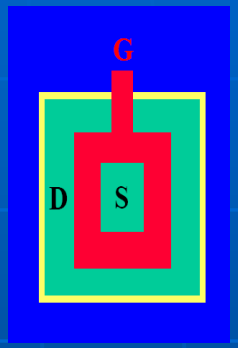
- Introduction
- Silicon-on-Sapphire (SoS) Technology
- SoS Test Chip
- Link-on-Chip Design

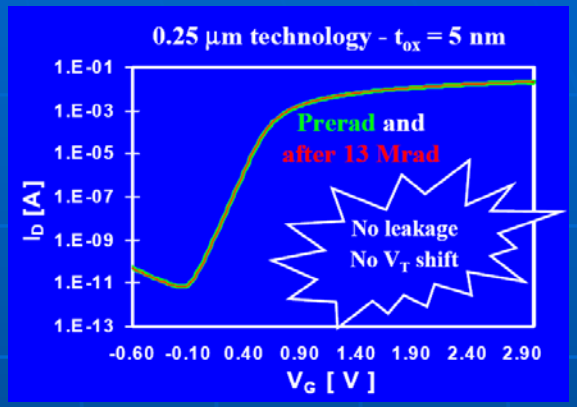
Radiation-hardening-by-Design (RHBD)

- The wide availability of commercial IC processes has led to the philosophy of “radiation hardening by design”.
- Explore circuit topologies and layout techniques to create radiation-tolerant circuits
  - Submicron bulk CMOS
    - inexpensive
  - BiCMOS
    - ideal for mixed-signal design, but very expensive
  - SOI/SOS
    - relatively new, growing in popularity

Radiation Hardening by Design

- Total Dose Effect
  - Enclosed layout Transistors
  - Guarded ring





G. Anelli, 2000 IEEE Nuclear Science Symposium and Medical Imaging Conference

- Single Event Effect
  - Marjory vote circuits
  - Error detection/correction Coding
  - Charge dissipation technique
  - Temporal filtering technique

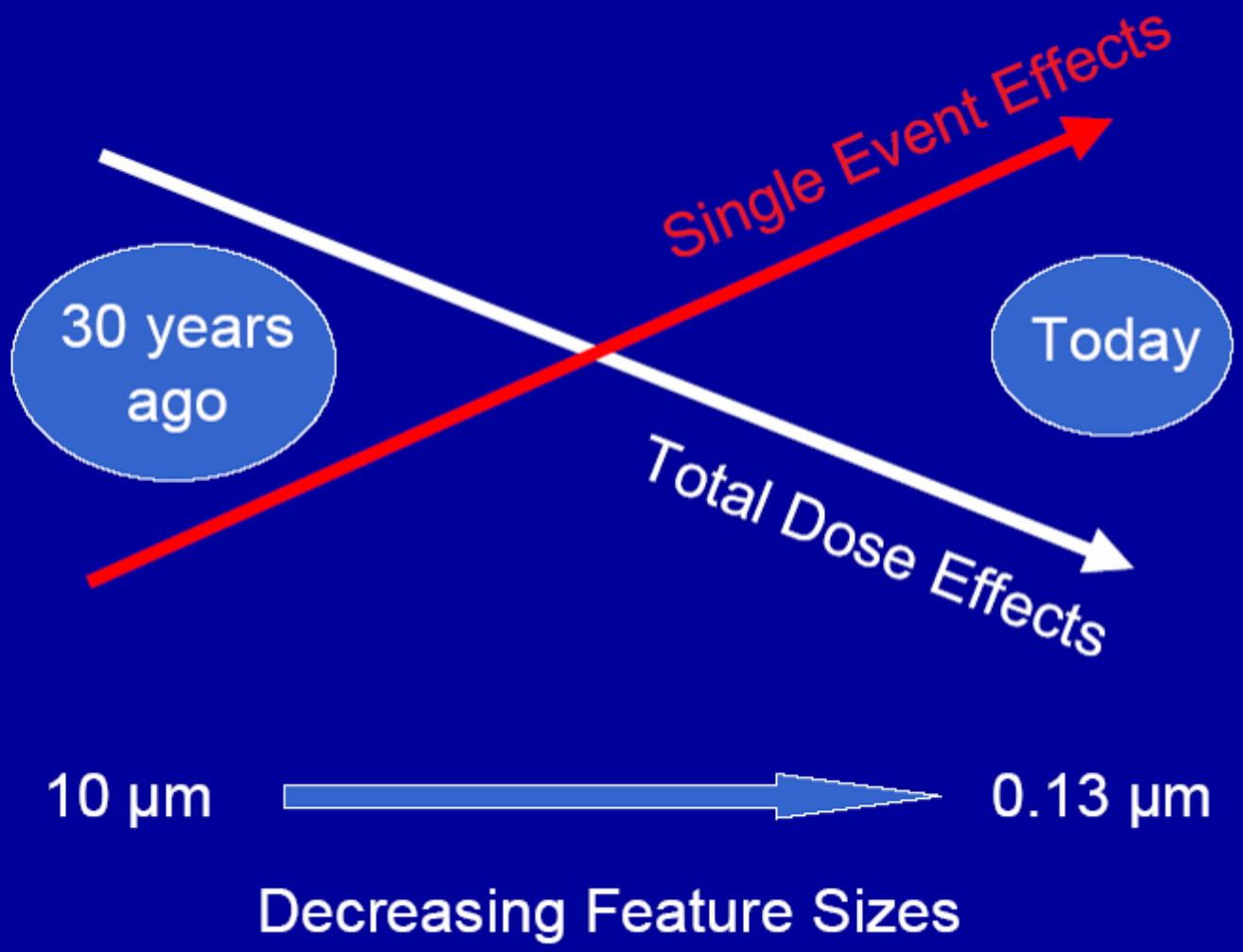
- Trade-off between radiation tolerance, performance, area and power dissipation.

Radiation-hard design challenges

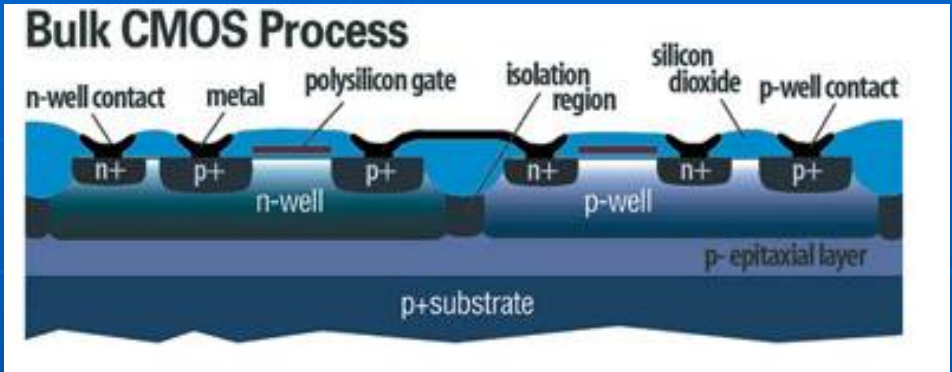
- Techniques that minimize one radiation mechanism may have little or no effect on another.
- Years ago, total dose concerns dominated radiation tolerant design, but they are now secondary to single event effects (SEEs).
- SEEs have grown in importance as feature sizes, capacitances, and operating voltages have been reduced.

IC Feature Size and Radiation Effects

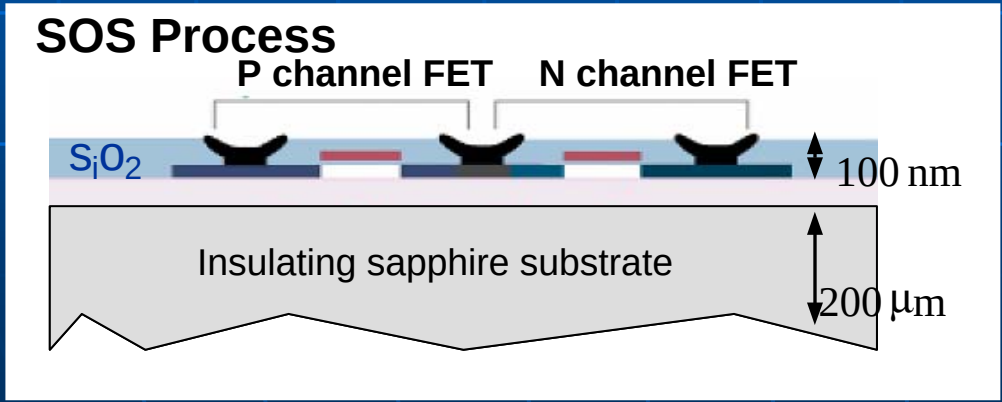
- Thinner oxides and better oxide/silicon interfaces have reduced total dose effects.
- Smaller devices at lower voltages with less charge movement have resulted in increased single event effects.



Peregrine's SOS Technology



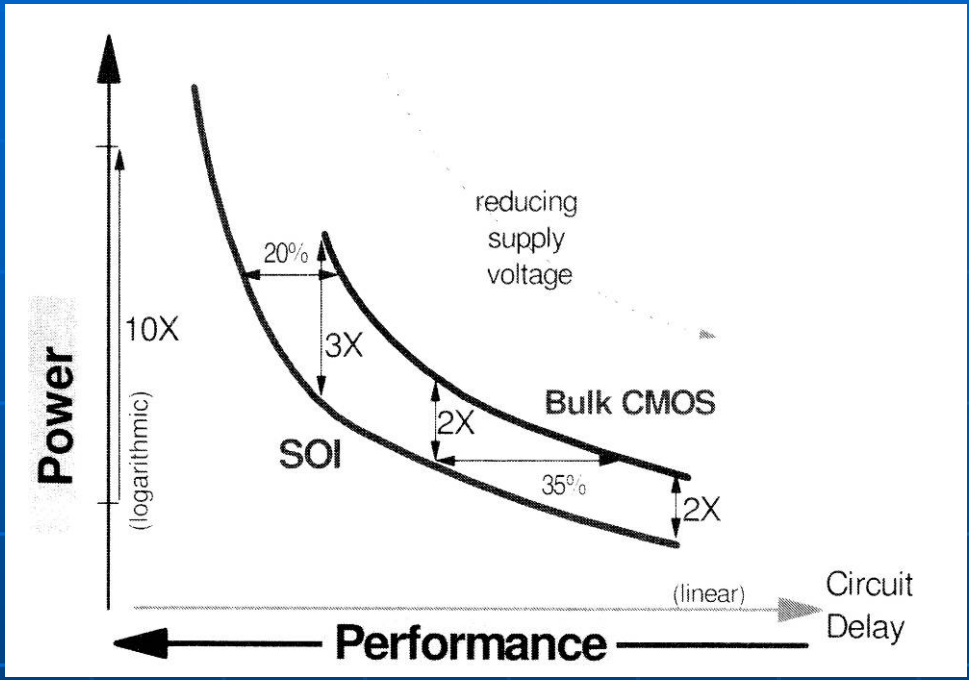
BULK CMOS



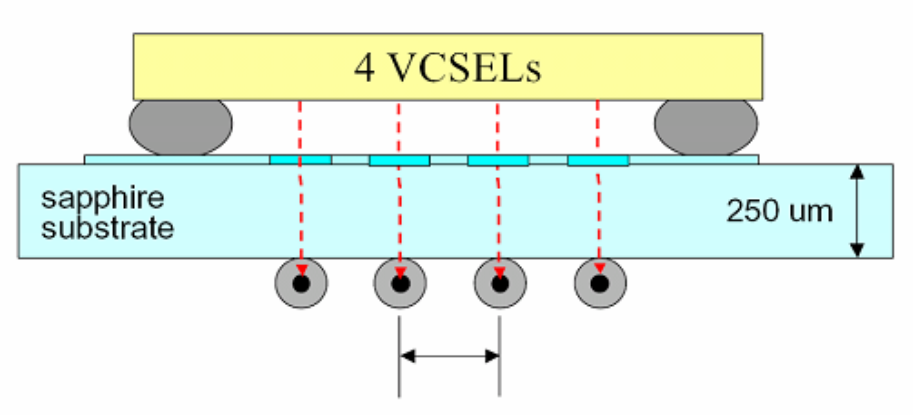
Peregrine's SOS
industry's first and only commercially qualified SOS technology

- No Single-event Latch-up in SoS CMOS!
- Increased immunity to SEE
- Ideal for radiation-tolerant mixed-signal circuit design due to minimum substrate noise

Process Features

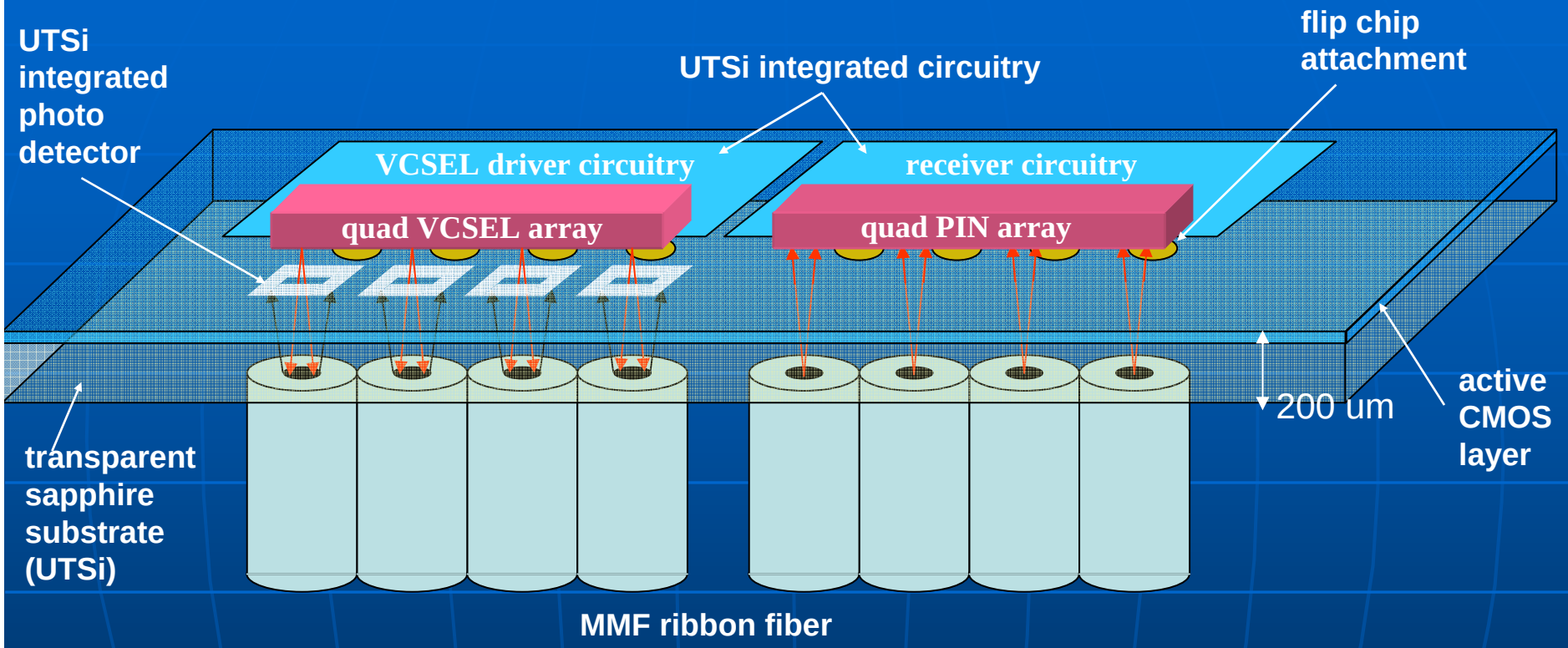


- Minimum substrate noise
  - Higher level integration of RF, mixed-signal and digital circuitry.
- Reduced Parasitic capacitance
- High performance
- Low Power consumption
- Minimum crosstalk



- Widely used in RF and space products
- Transparent substrate allows for compact and simple integration with optical devices

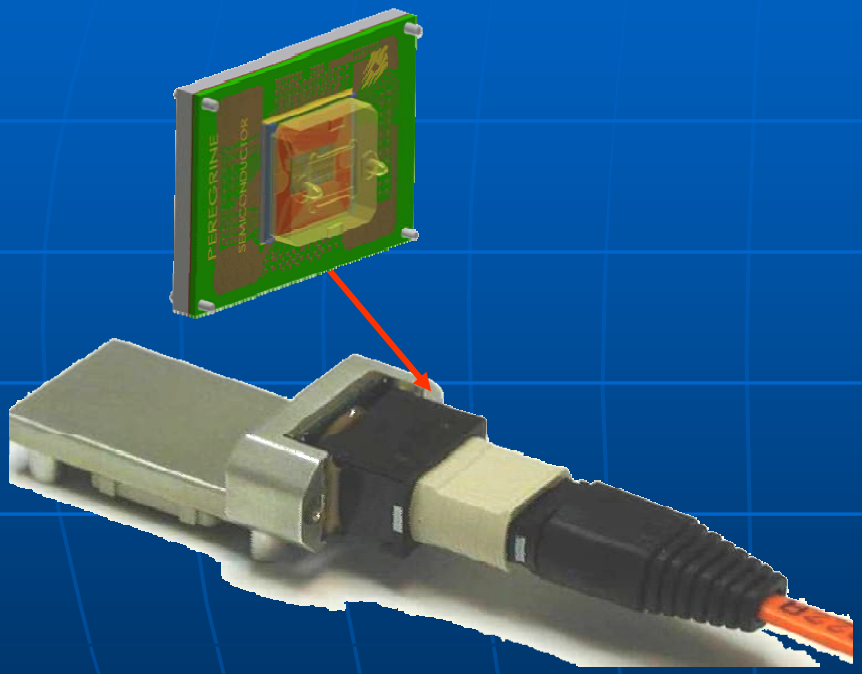
Flipped OE devices on SoS substrate



- Flip-chip bonding of OE devices to CMOS on sapphire
  - No wire-bonds – package performance scales to higher data rates
  - Rugged and compact package

Peregrine Space Optical Transceiver

MTP Connector Module



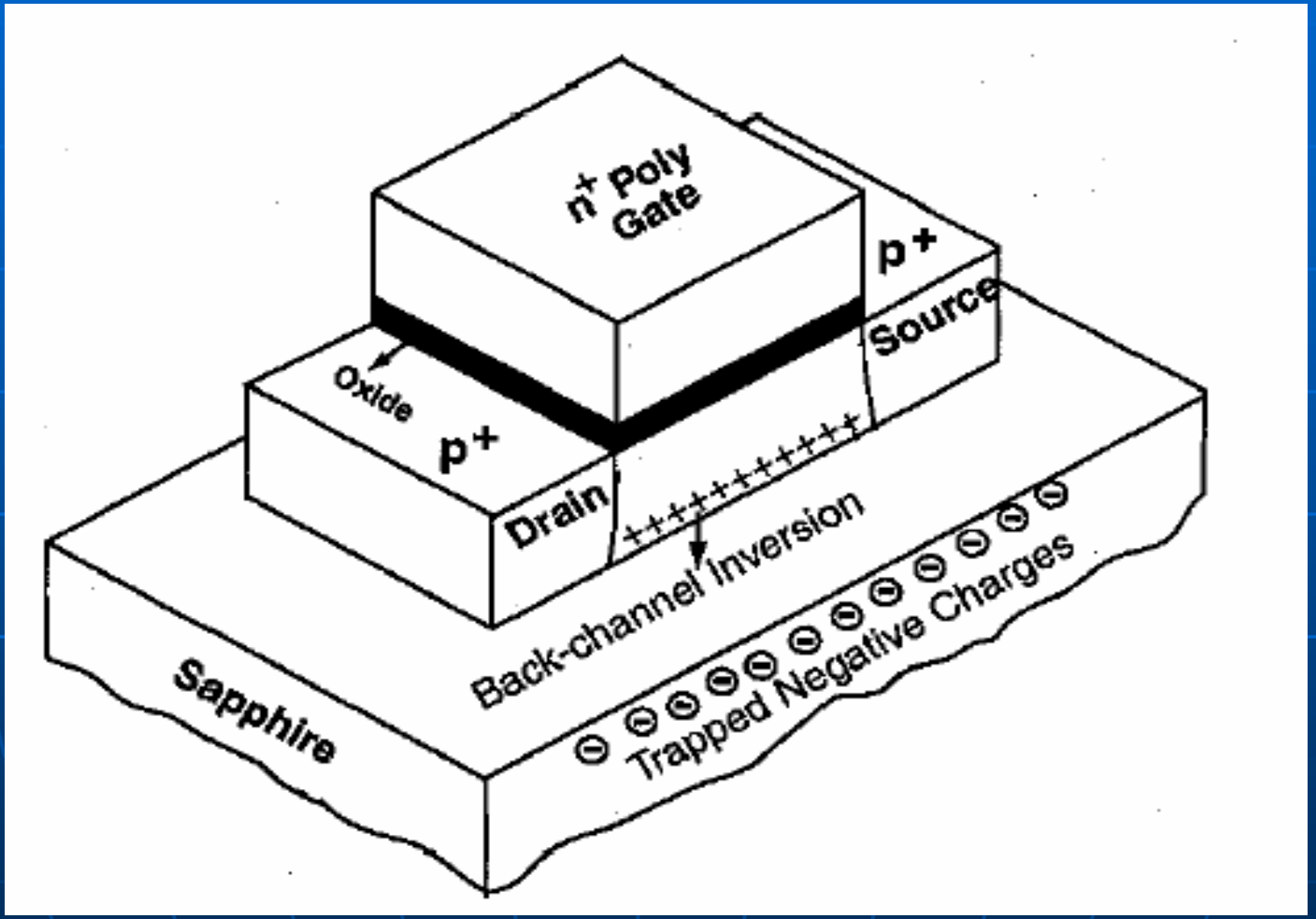
15 mm height
Berg MegArray PCB socket

- 0.5-um SoS
- Single 4+4 transceiver component with variable data rates (CML interface)
  - Minimum data rate – 10 Mbps
  - Maximum data rate – 2.7 Gbps per channel
- Radiation
  - Total Ionizing Dose: 100 kRad(Si)
  - SEU: > 20 MeV-cm2/mg
- 15 year operational lifetime
- 125 mW per channel power consumption (dissipated to panel mount)
- Vibration
  - 15.33 gRMS for 3 minutes total

SoS CMOS v.s. Bulk CMOS

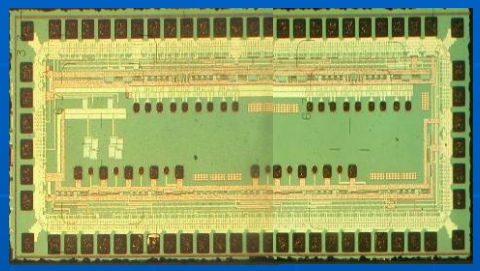
	0.25 μm SoS	0.13 μm Bulk CMOS
Performance	Up to 10 GHz	Up to 10 GHz
Leakage Current	Substrate as an insulator (10^{14} ohm/m at room temperature). Reduced substrate junction capacitance leads to lower leakage current.	High Leakage current
Power Dissipation	Reduced parasitic capacitance also leads to a lower power dissipation	
Crosstalk	Minimum crosstalk due to reduced substrate capacitance	Substrate noise causes crosstalk between channels
Cost	$100k for wafer mask set; $1000 per wafer	$800k for wafer mask set; $800 per wafer

Back-channel Leakage Current in SOS

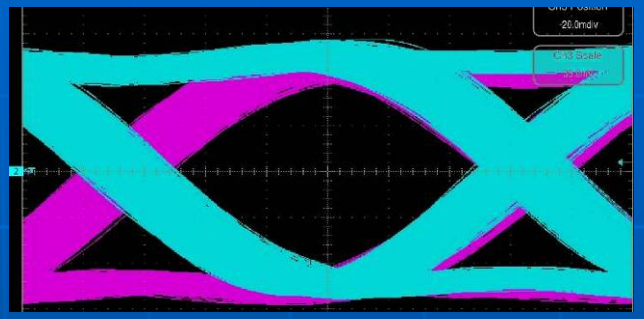


Possible Leakage path along the Si/Sapphire interface

Preliminary Radiation Test Results on 0.5-µm SoS CMOS Technology

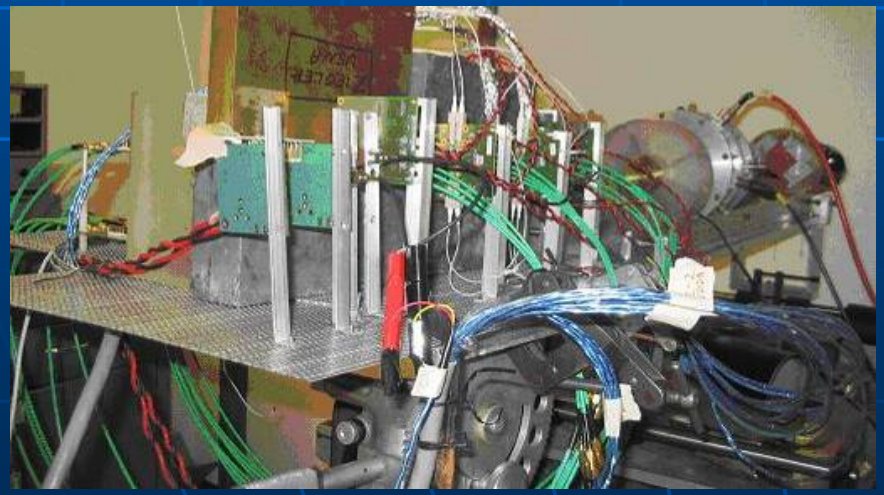


Transceiver chip made in 0.5um SoS CMOS Technology



2.5Gbps Before radiation

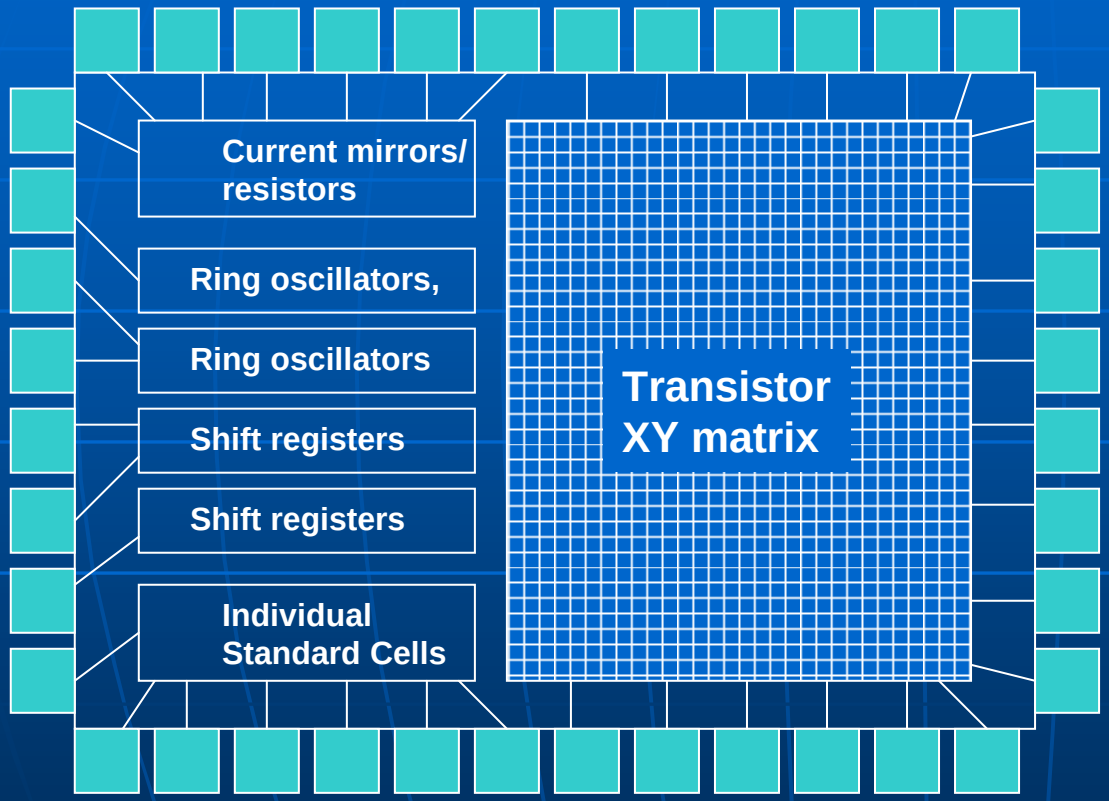
2.5Gbps Post-rad 100Mrad



Radiation test setup at the Northeast Proton Therapy Center

1.6 Gbps Post-rad 100Mrad

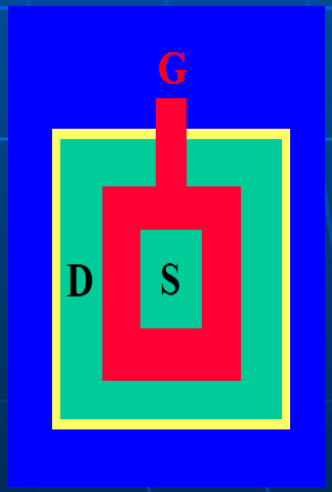
Dedicated Radiation Test Chip for a 0.25-µm SOS CMOS



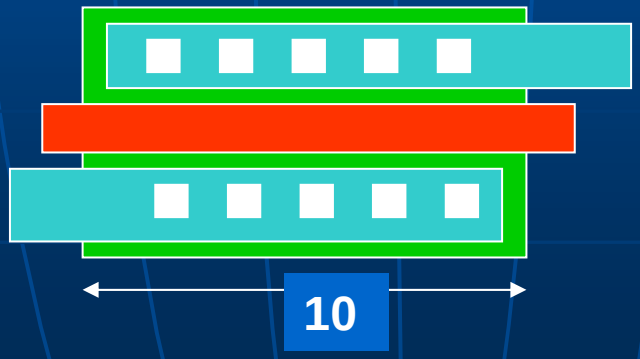
- Single NMOS and PMOS
- Ring Oscillators
  - to characterize the performance and power dissipation
- Shift registers to characterize SEE
  - Standard layout, edgeless layout, majority vote circuit, resistively hardened cells
- Digital Standard cells
- Current mirrors
- Resistors

Transistor Test Structures

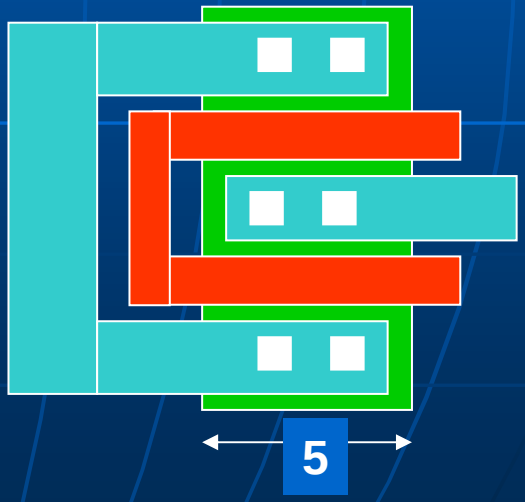
- NMOS and PMOS Array
  - PMOS and NMOS with different size
    - Different lengths to characterize back-channel leakage current
  - Each transistor implemented in four layouts
    - Standard, edgeless (ELT), two-finger and four-finger layout to characterize edge leakage current



Edgeless (ELT)

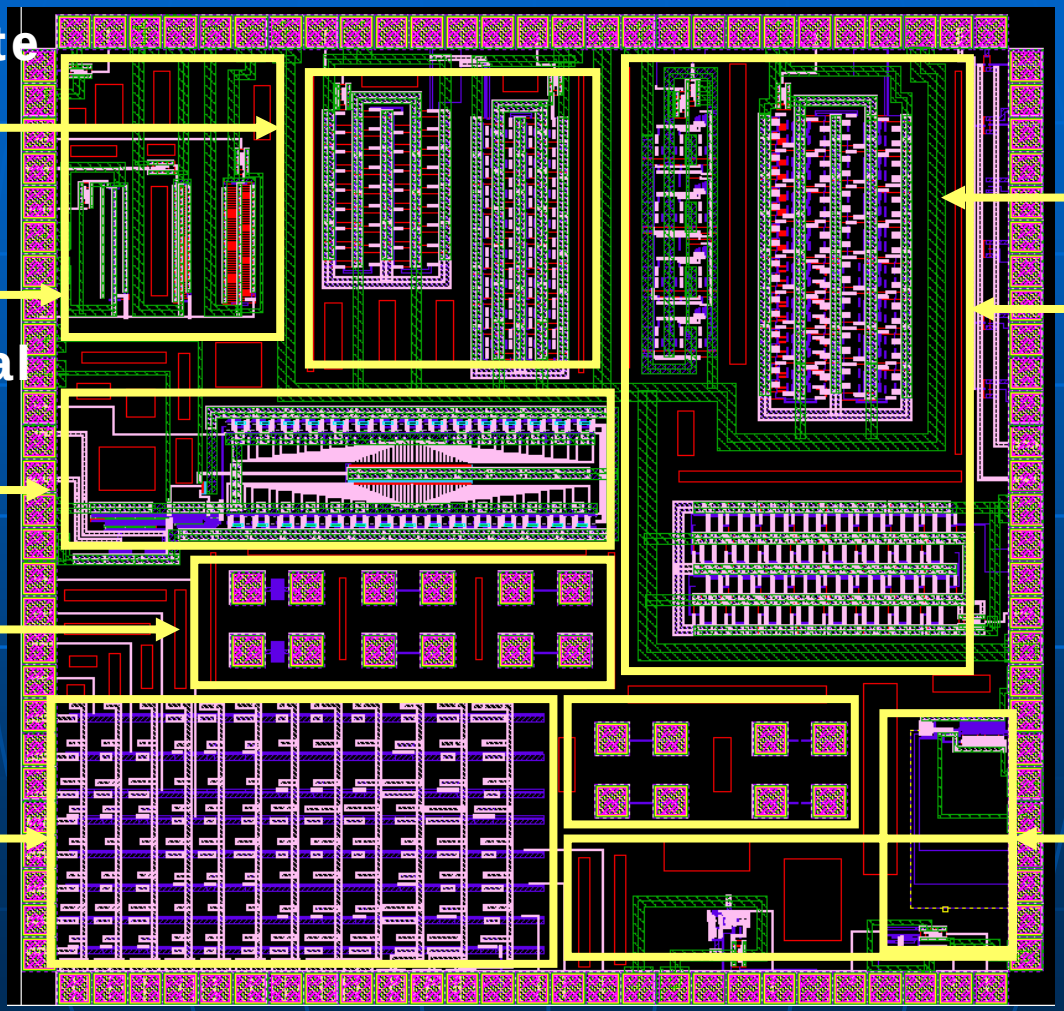


One-finger



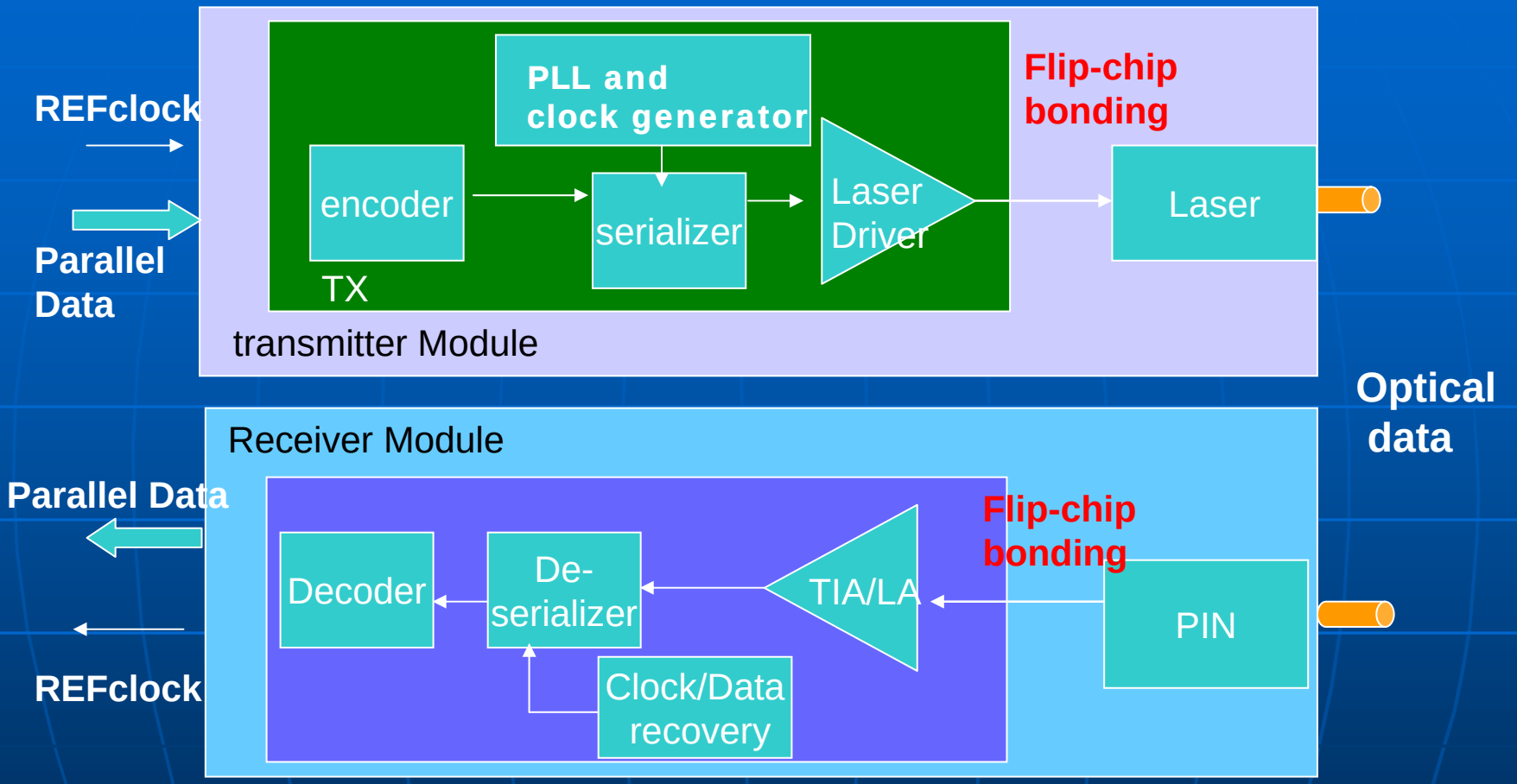
Two-finger

SOS Rad-hard Test Chip Layout



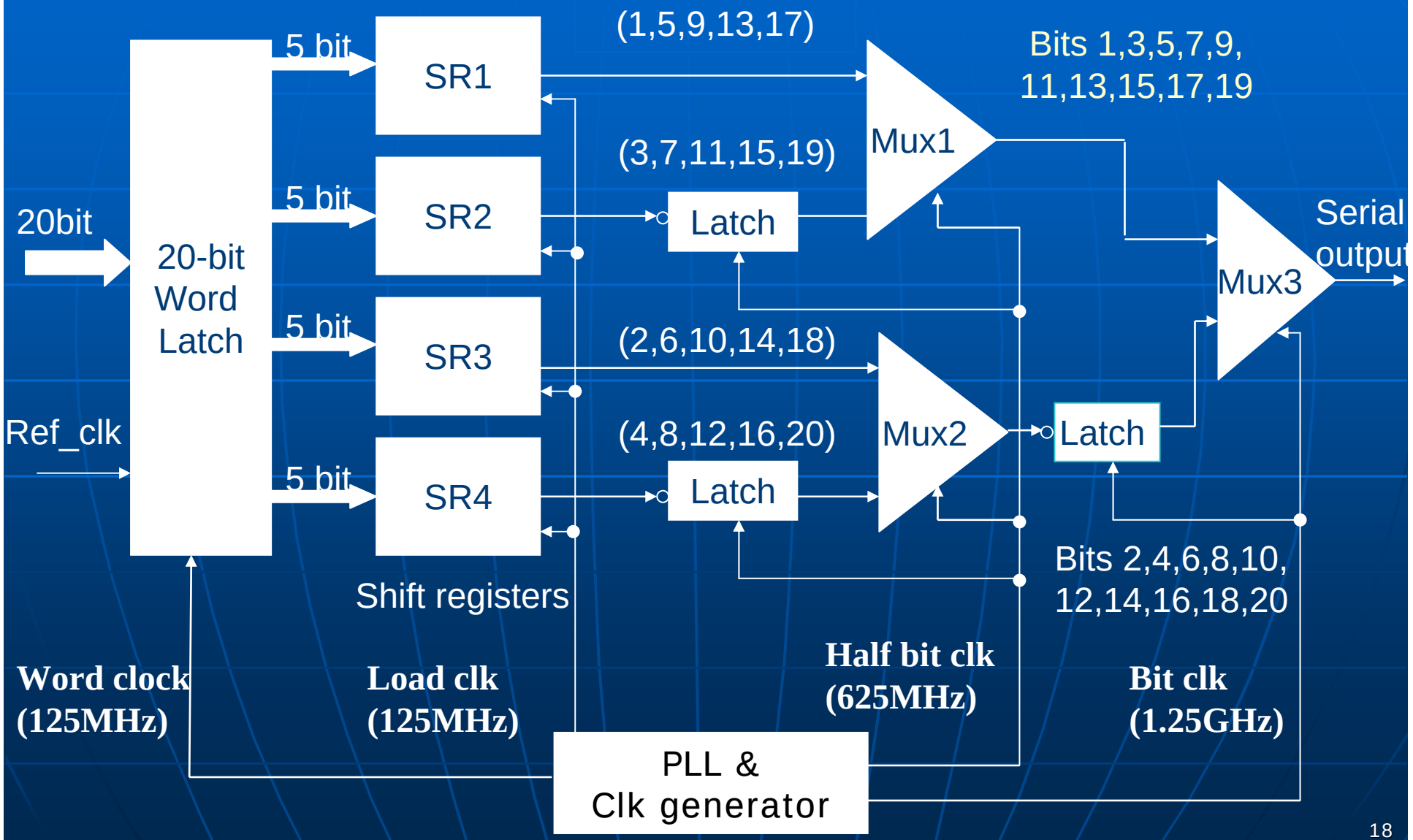
Chip was submitted for fabrication in Oct. 2005

Link-on-Chip Architecture

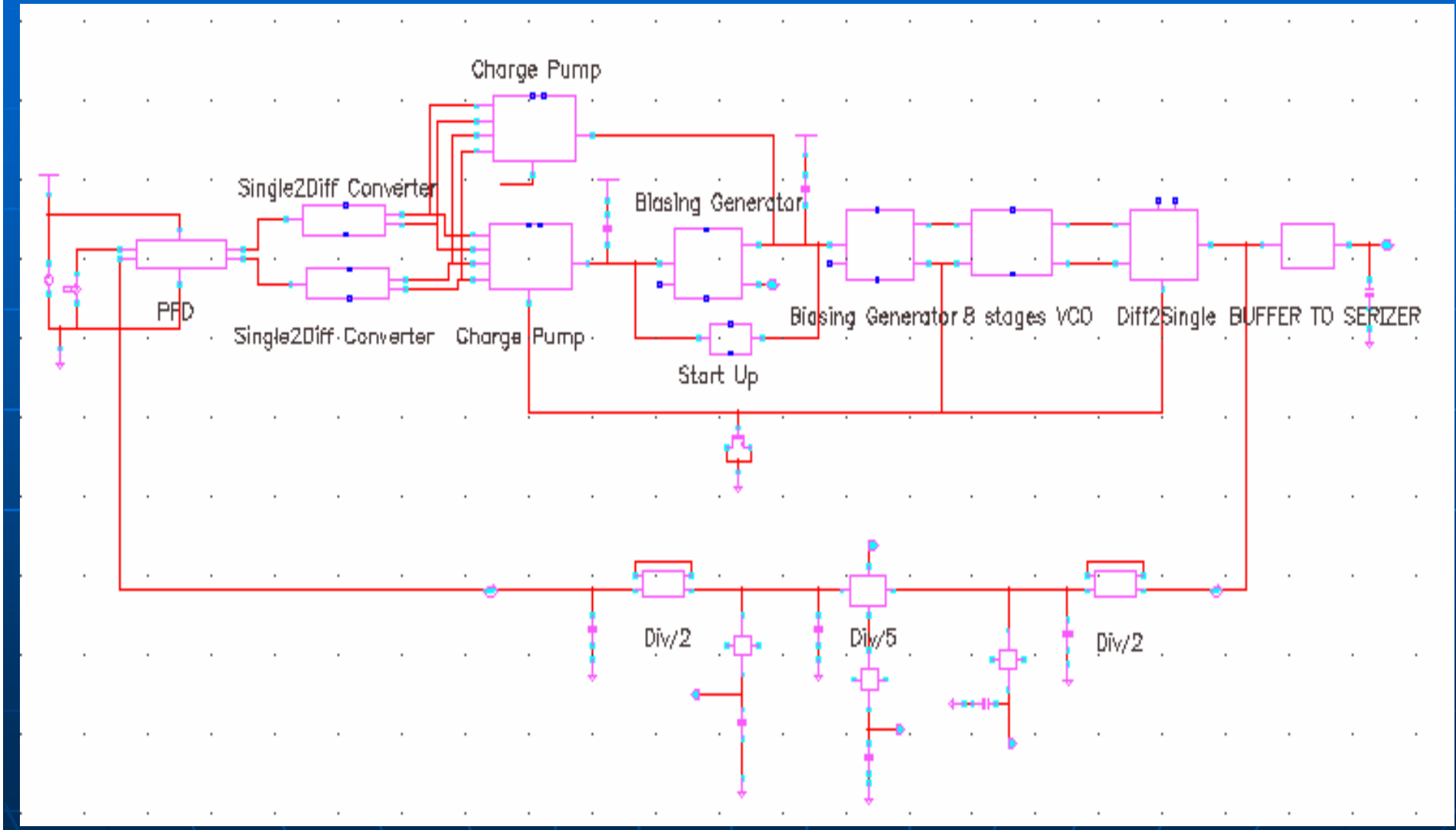


- **Improve performance**
  - No off-chip high speed lines
  - Flip-chip bonding reduces capacitance and inductance
- **Reduce power consumption**
  - No 50-Ohm transmission lines between chips

2.5-Gbps Serializer Architecture



PLL and Clock Generator

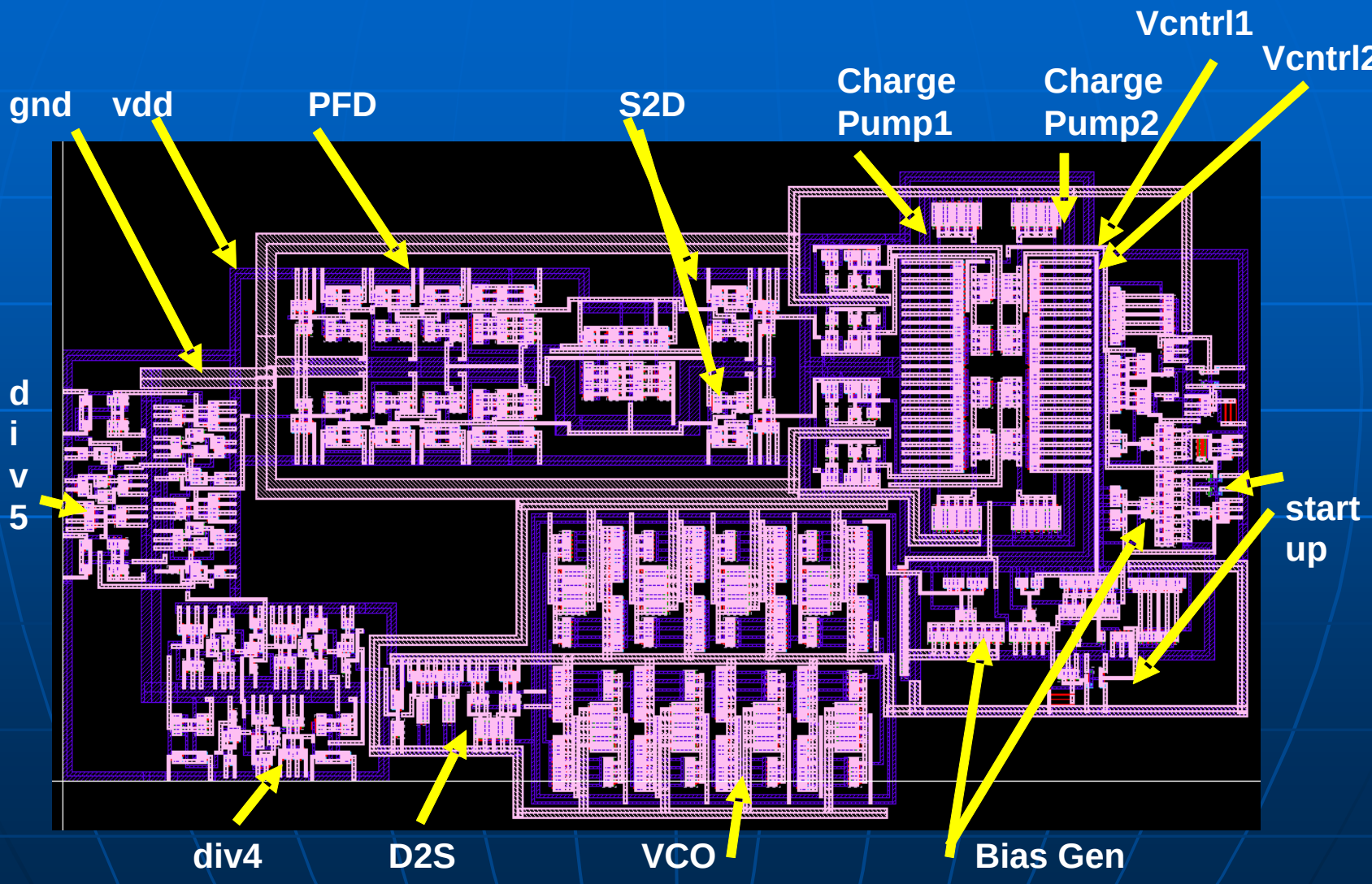


Phase-Locked Loop

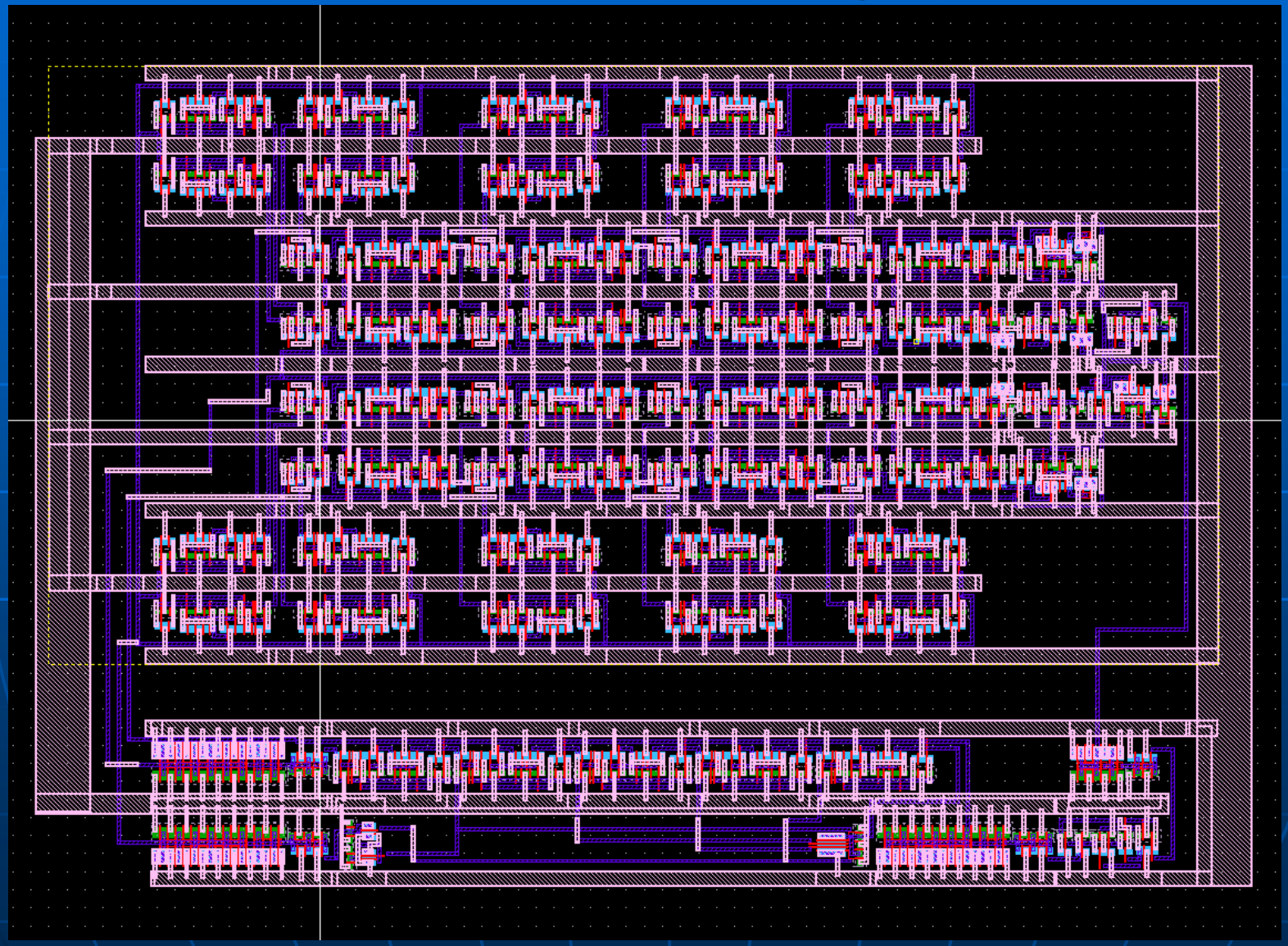
- Self-biasing structure [1]
  - Remove process technology and environmental variability, low input tracking jitter, Wide operating frequency range
- Phase-frequency detector
  - with equal short duration output pulses for in-phase inputs
- Charge-pump with symmetric load
- VCO with differential buffer delay stage with symmetric loads
- Loop filter

[1] J. G. Maneatis, "low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE JSCC, Vol. 31, No. 11, Nov. 1996.

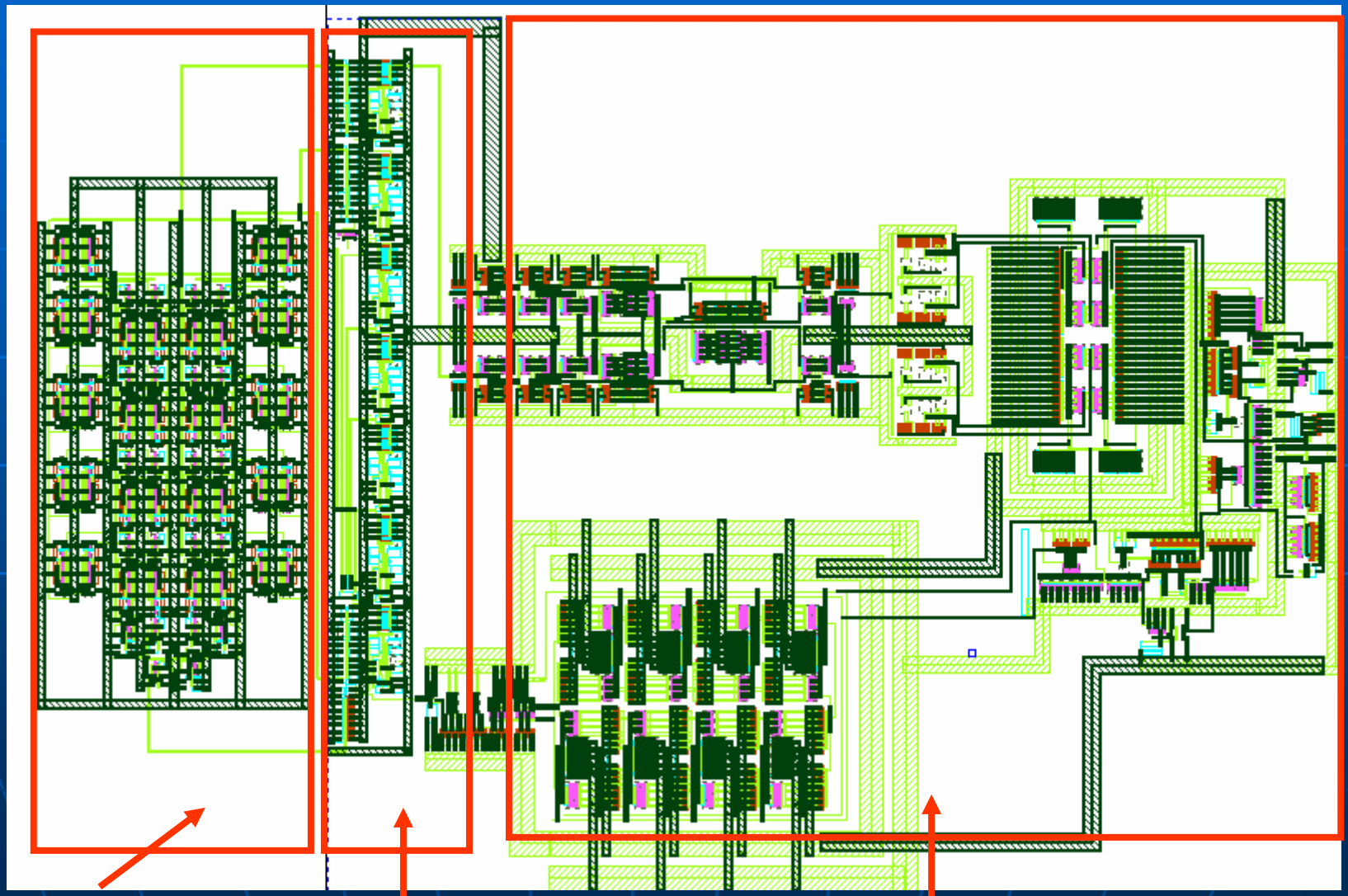
PLL Layout


gnd
vdd
PFD
S2D
Charge Pump1
Charge Pump2
Vcntrl1
Vcntrl2
div5
start up
div4
D2S
VCO
Bias Gen

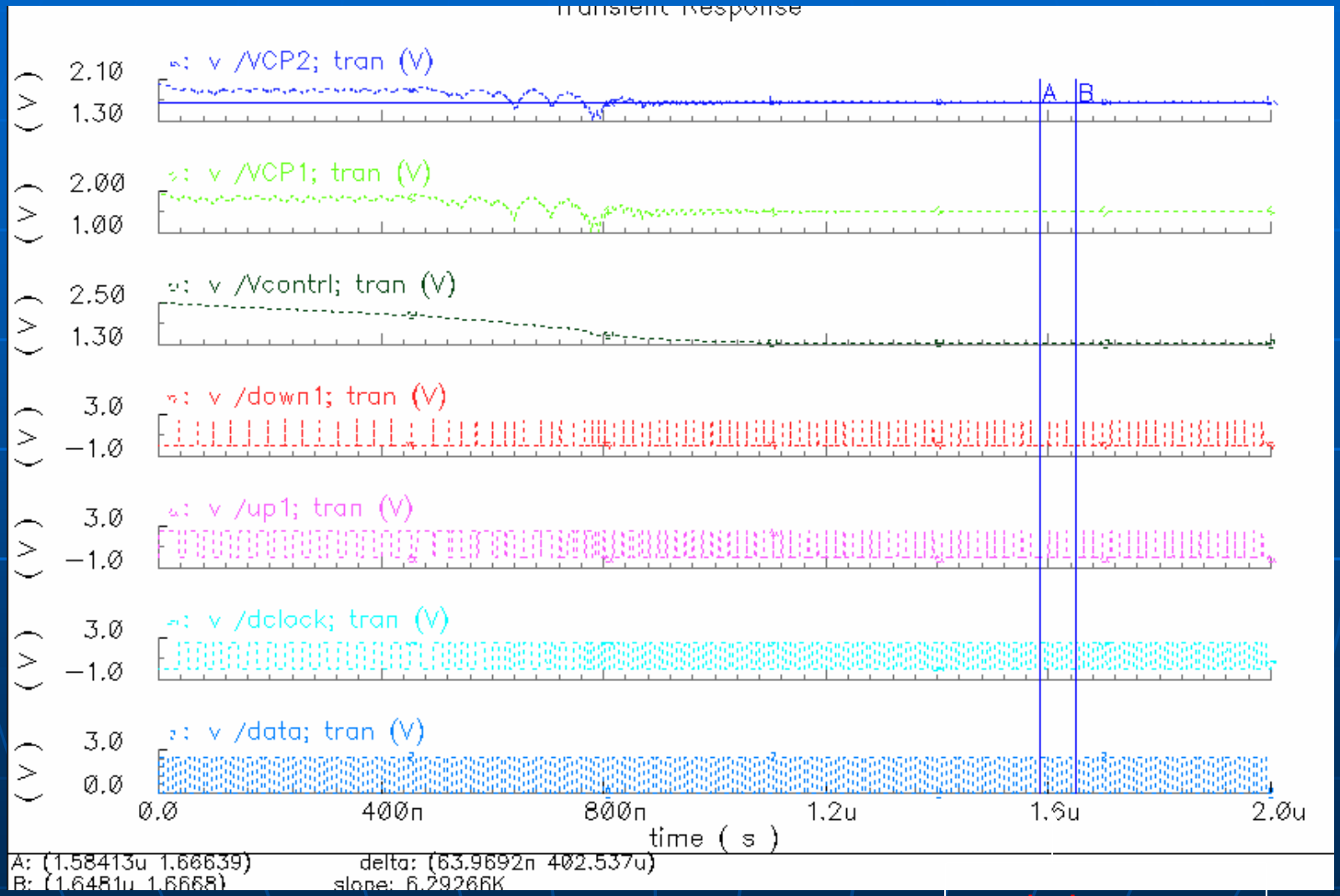
Serializer Layout



Serializer + PLL & Clock Generator

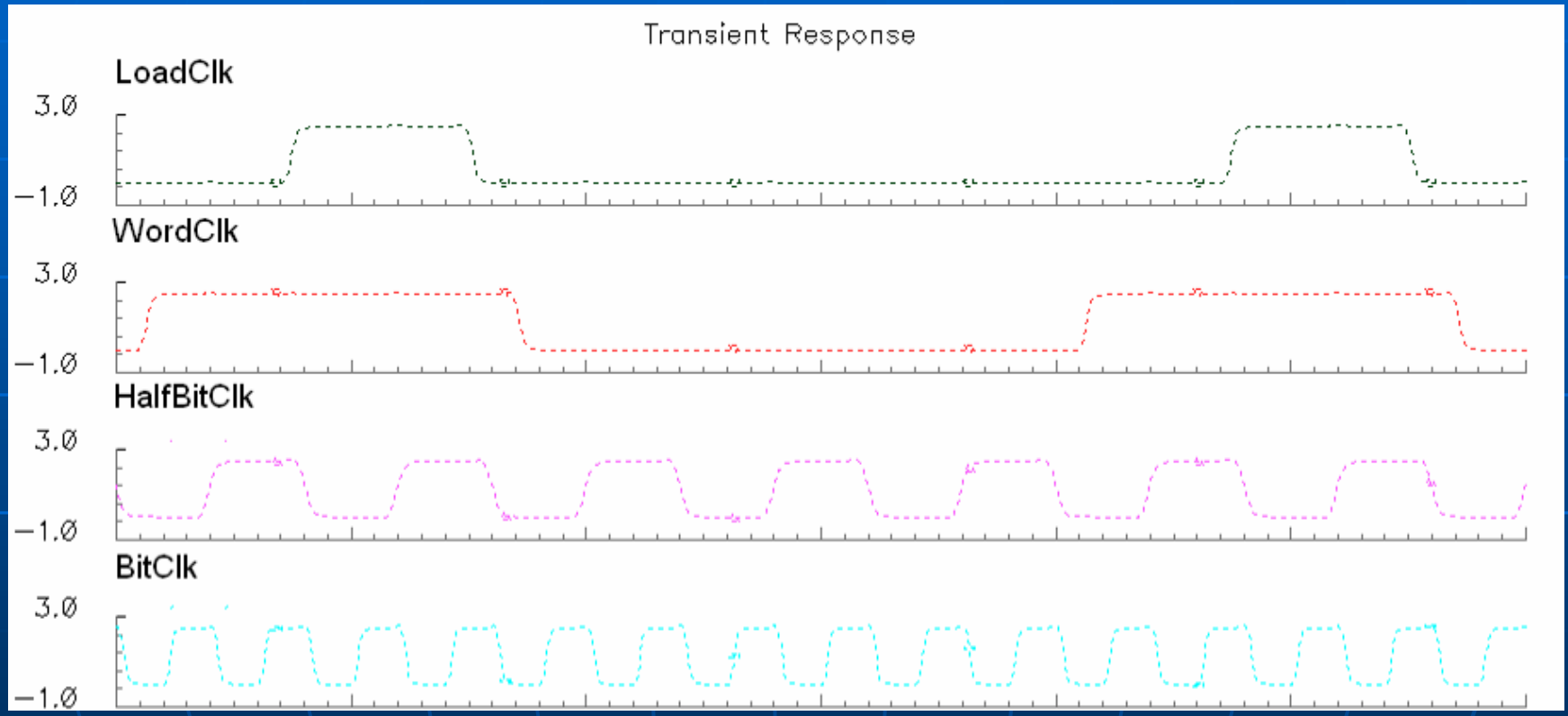


1.25GHz PLL Simulation Results

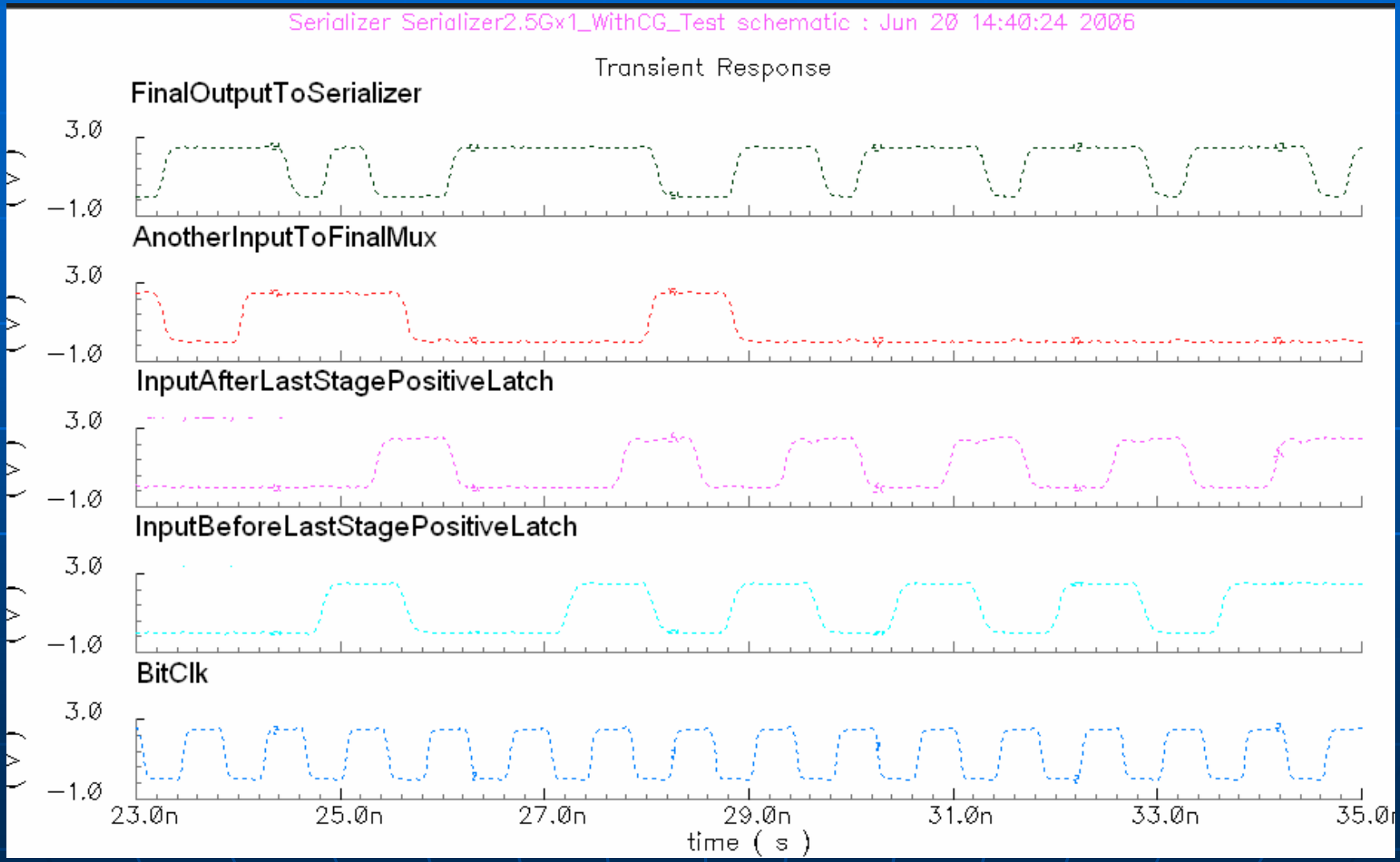


Lock time=1.5us

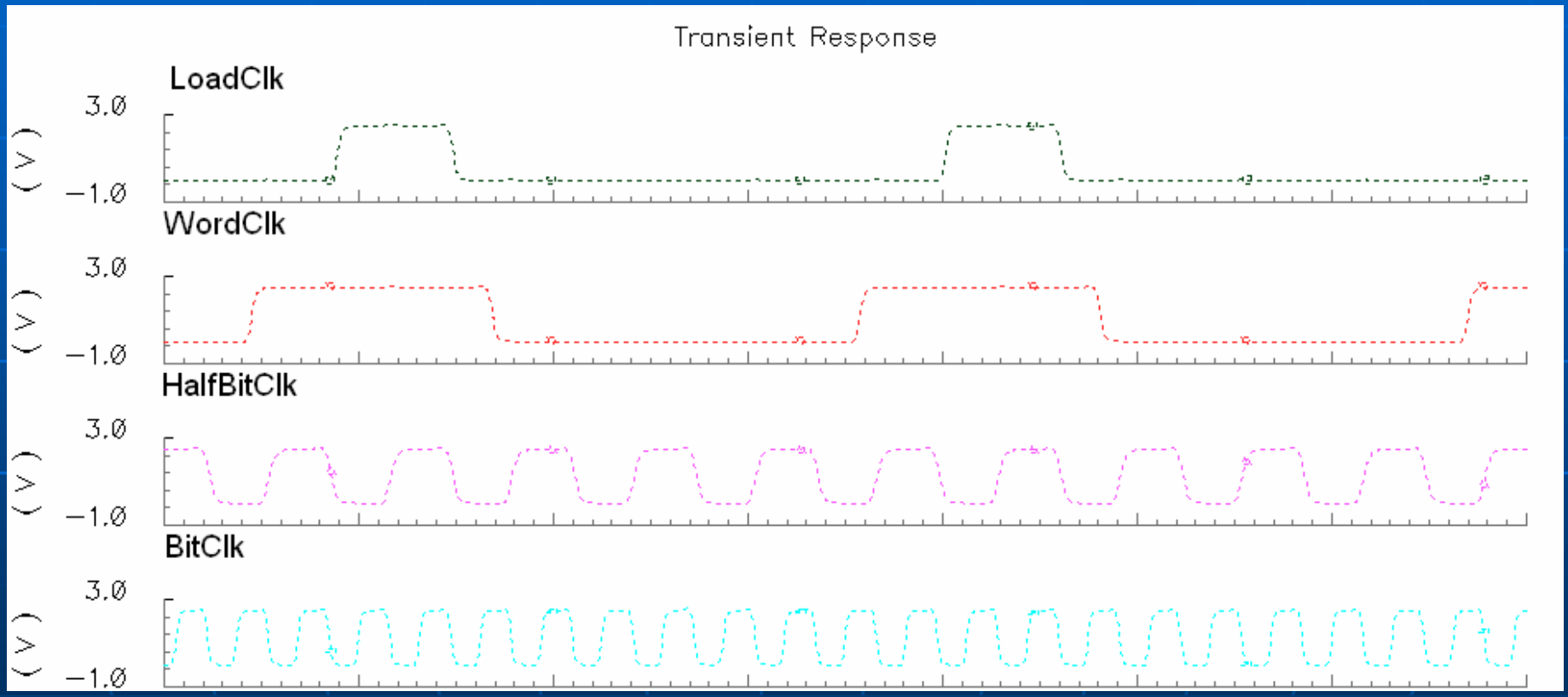
Clock Generator Output @ 1.25GHz



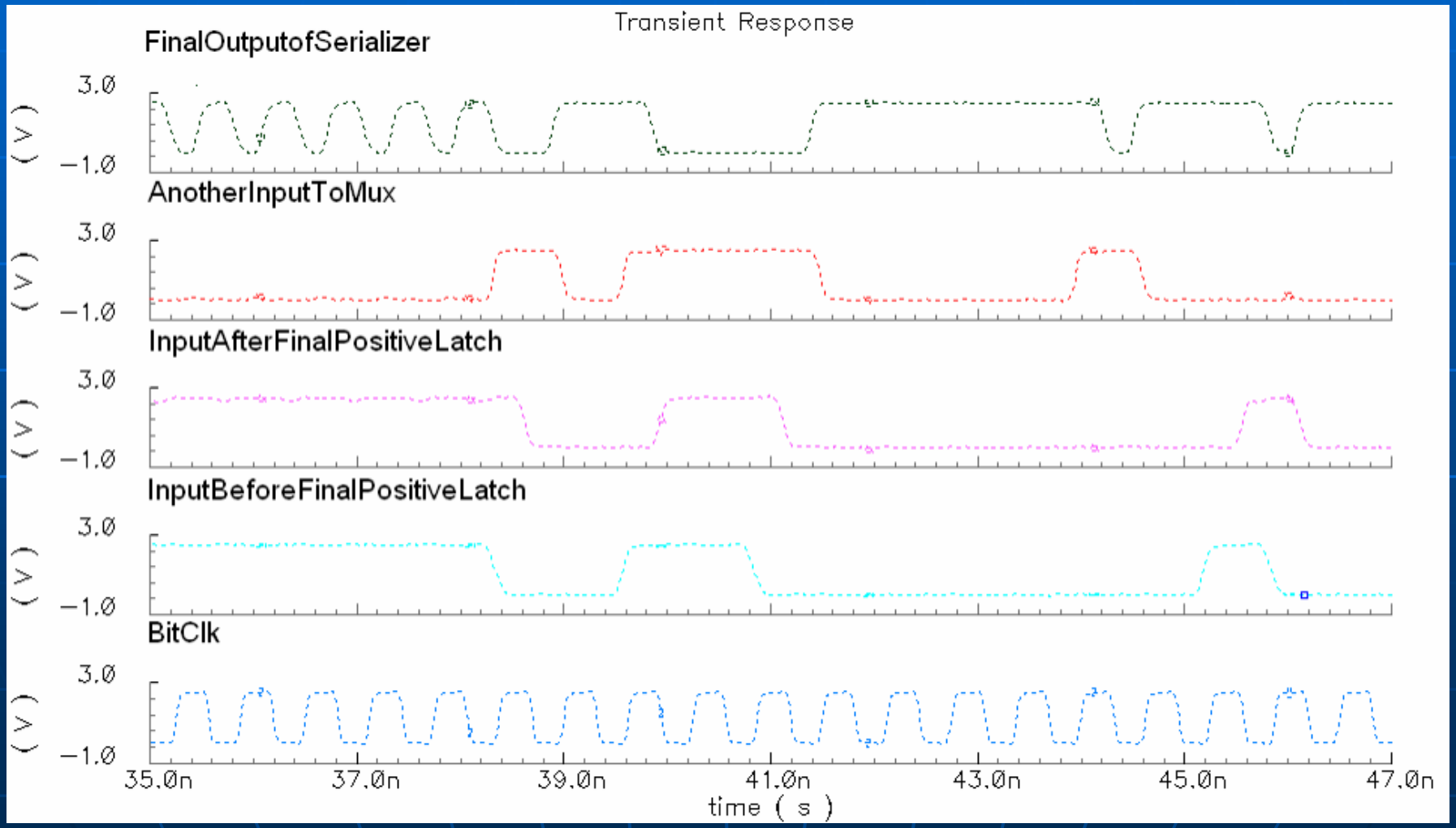
Serializer Simulation at 2.5-Gbps



Clock generator simulation @ 1.6GHz



Serializer Simulation @ 3.2Gpbs



Conclusion

- Dedicated test Chip lab has been tested and fabricated
- Lab and radiation testing is in progress
- Link-on-Chip serializer and PLL & clock generator components are completed.

Acknowledgement

- Paulo Moreira at CERN-EP/MIC for sharing GOL link design and many useful discussions
- Peregrine for sharing the cost of the chip fabrication

Thank You!