CMS Calorimeter Trigger Main Processor Board: MP7 Based Demonstrator

Imperial College London

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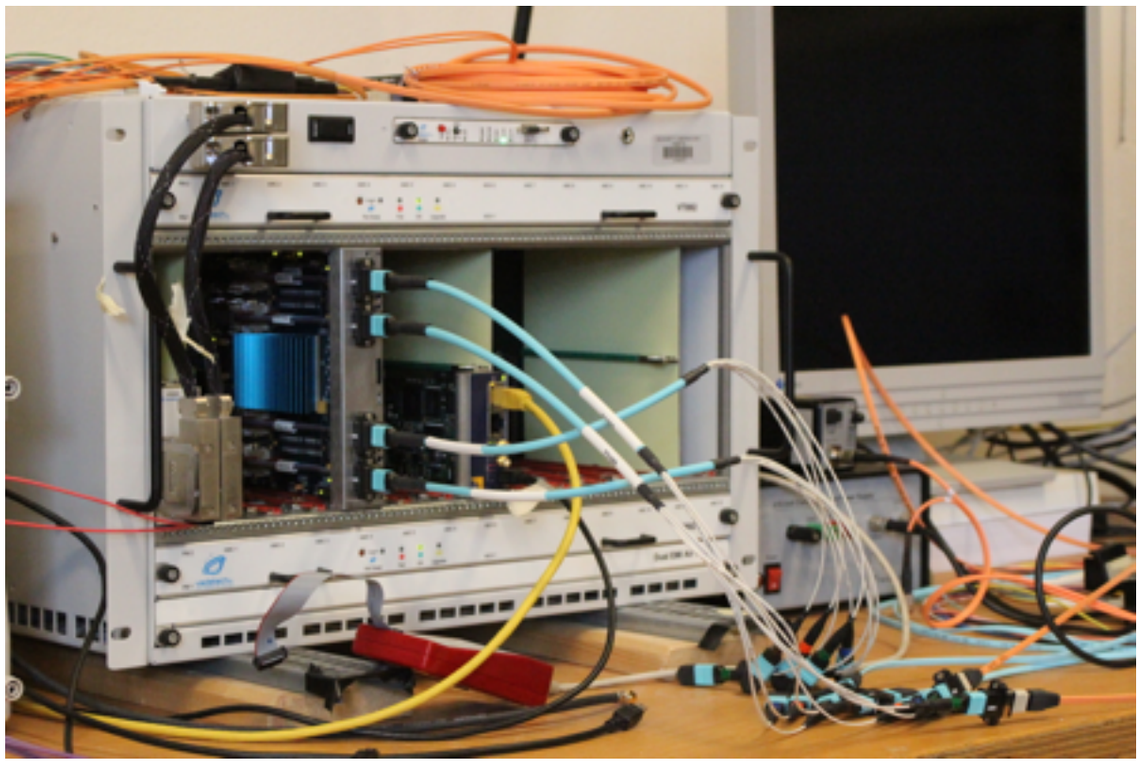

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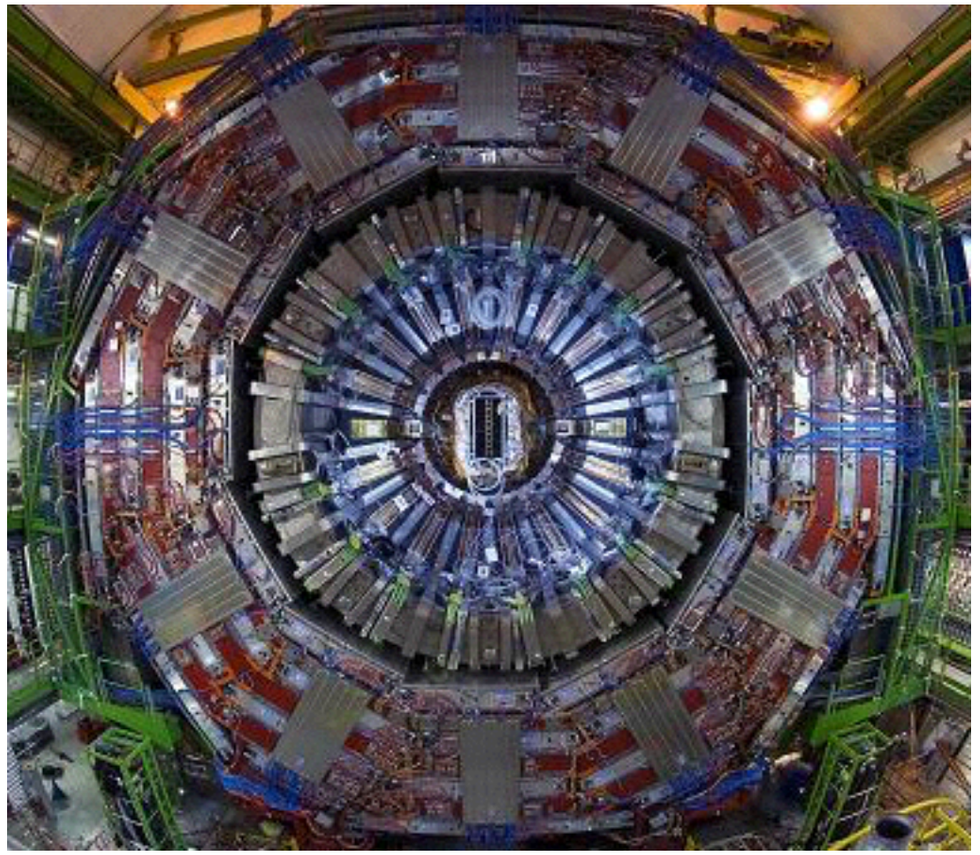
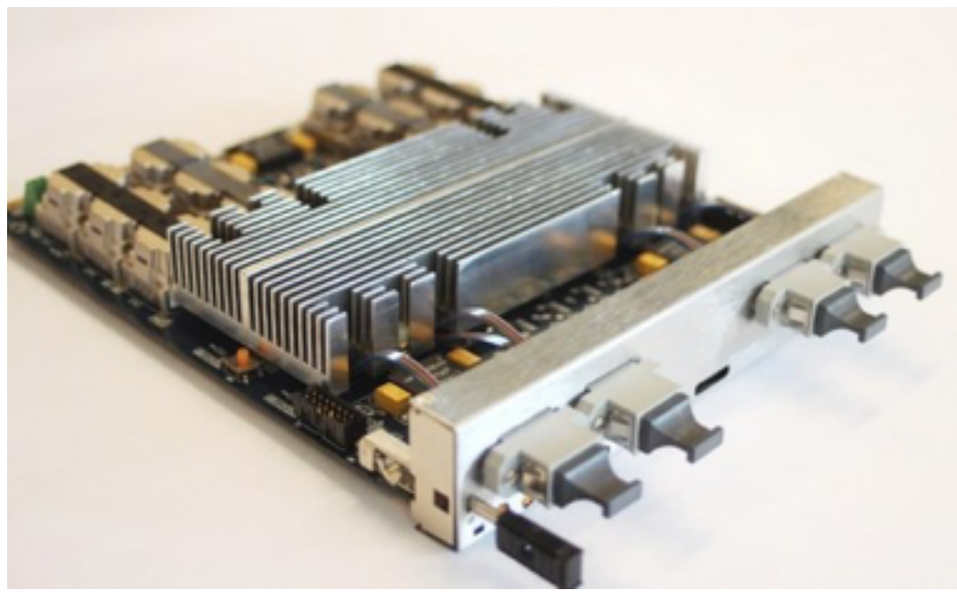
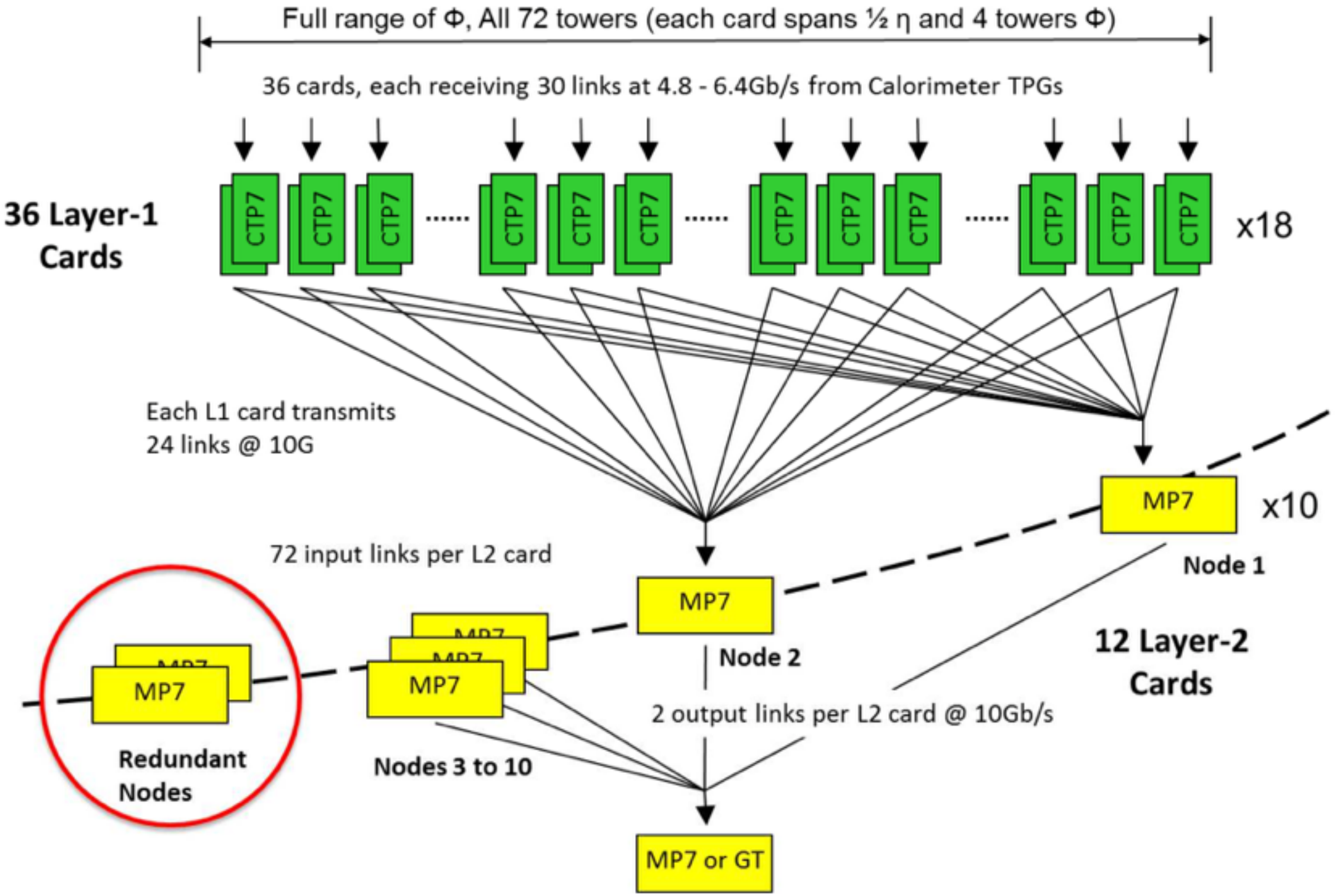
Introduction

- LHC upgrades increase lumi & pile-up dramatically
- Rates using current L1 trigger rise by factor of 6
- For 100 kHz L1 rate upgraded trigger requires:
  - ➡ pile-up subtraction
  - ➡ improved isolation of electromagnetic objects
  - ➡ improved jet finding
  - ➡ improved hadronic tau identification
  - ➡ needs to be flexible and scalable
- Imperial MP7 (Master Processor Virtex 7) board utilises huge programmable logic to very quickly identify jets & e/gammas from HCAL & ECAL towers
- Upgrade uses novel time multiplexed architecture to fit whole detector at full resolution in one board



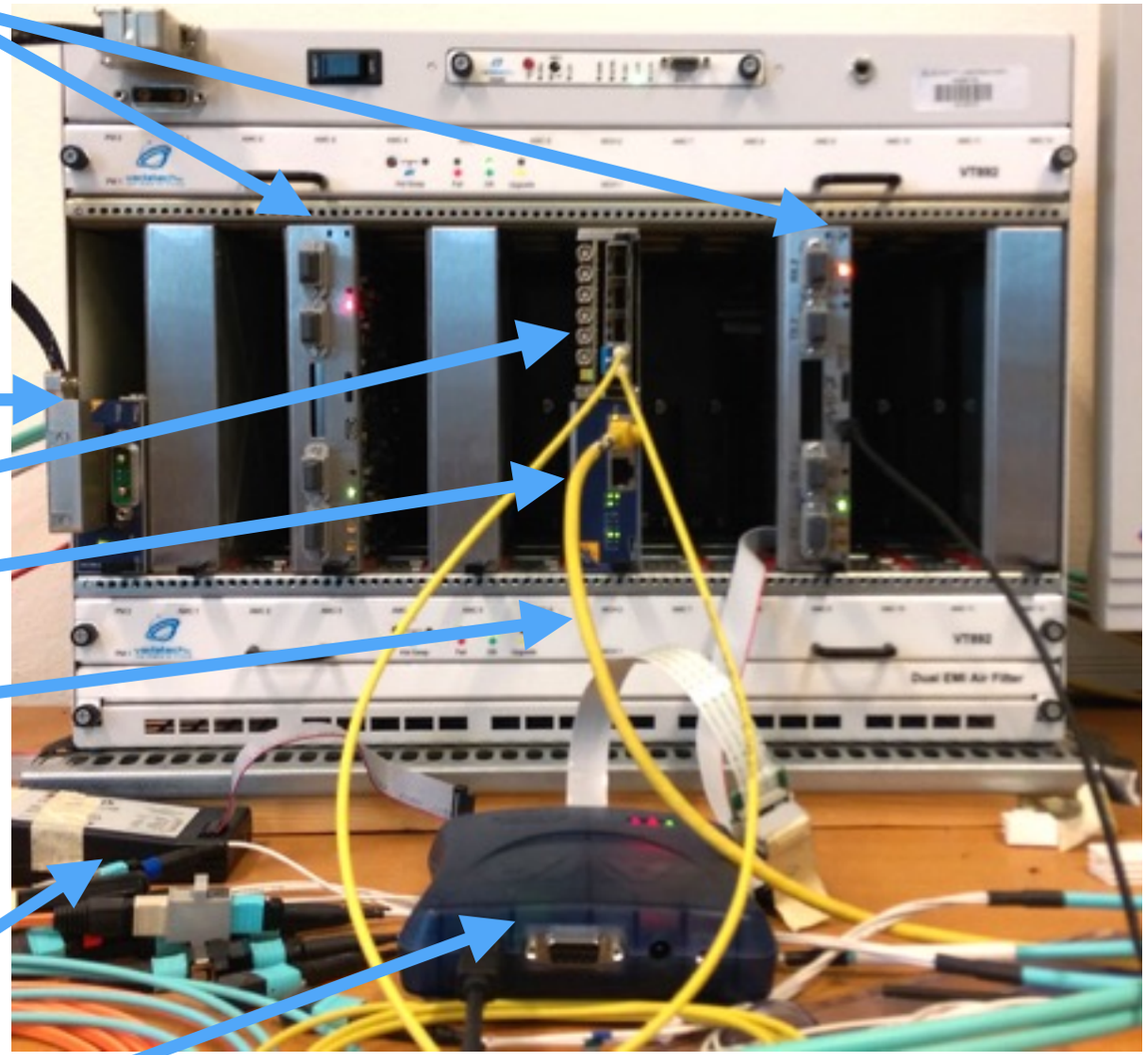


Calo Trigger Architecture



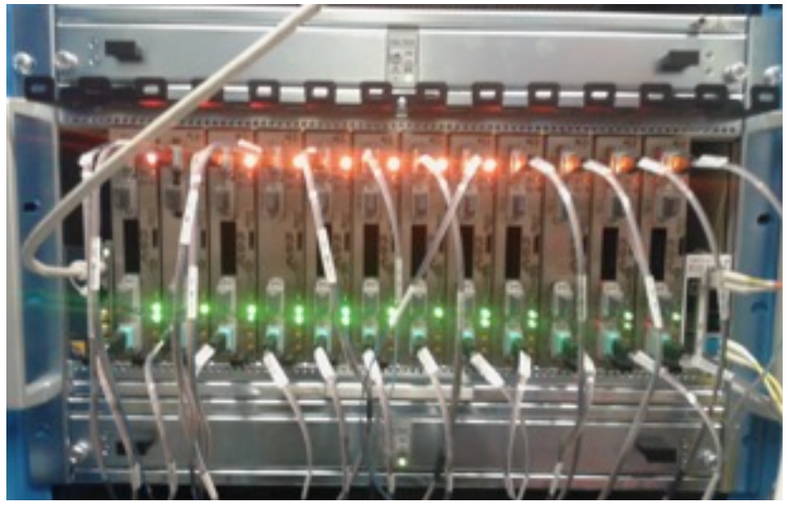
The Demonstrator

- Testing and development of the MP7 board and associated firmware and software not trivial!
- Requires a stable infrastructure comprising
  - ➡ microTCA crate with power supplies
  - ➡ AMC13 providing TTC, DAQ & TTS
  - ➡ MCH - microTCA carrier hub
  - ➡ ethernet connection to linux PC
  - ➡ MP7 software package
  - ➡ Reliable firmware builds
  - ➡ Xilinx programmer for FPGA & CPLD
  - ➡ AVR debugger for programming MP7 microcontroller



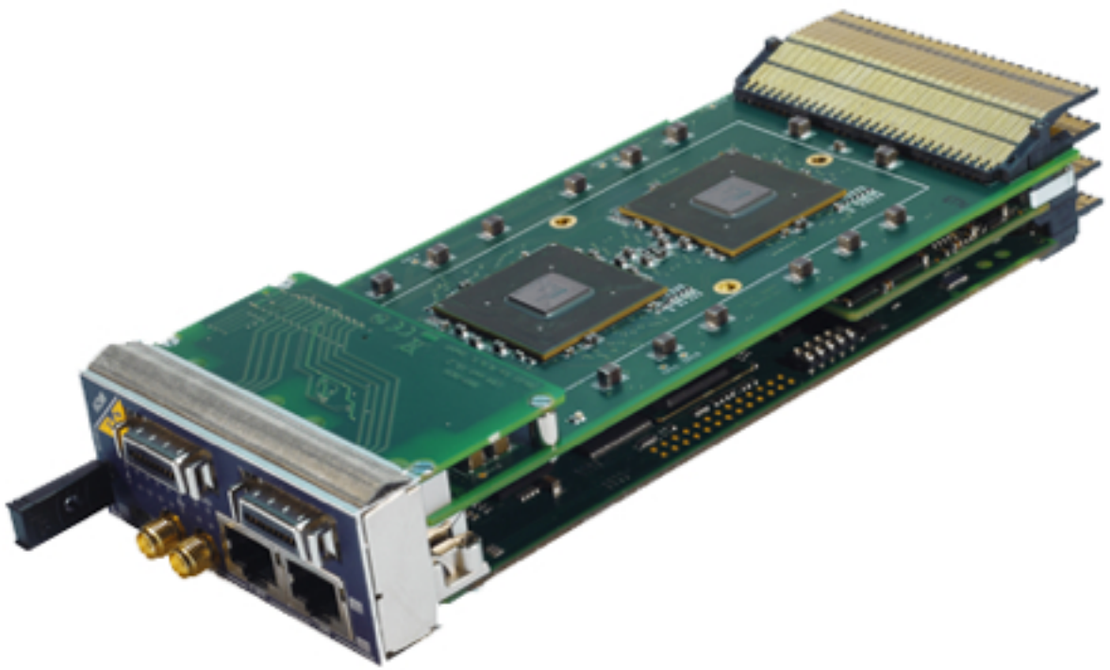
microTCA Crate

- Trigger upgrade hardware mostly moved from VME to microTCA form factor
- Part of AdvancedTCA family
- Telecommunications standard
- Small, flexible form factor, modular system
- Multiple high speed serial links
- Significantly higher backplane bandwidth
- Native support for multiple comm protocols:
  - ➡ Gigabit ethernet, SATA/SAS, PCIe, SRIO
- Expandable backplane connectivity
- Space for multiple optical connectors & large heatsink
- Dual power modules get 48V & supply 12V to AMCs and provide redundant power to all cards



✳ Although uTCA is generally a well supported standard, still issues with standardisation between vendors

MCH



- MicroTCA Carrier Hub
- Supports and manages all 12 AMCs, AMC13, fan trays and 4 power modules
- Provides Gigabit Ethernet connection for crate and board control from Linux PC over backplane to MP7 IPbus core
- Monitors AMC sensor info over IPMI (I2C)
- Stores FRU/SDR info for all AMCs
- Performs safety shutdown when sensors go over critical thresholds, e.g. FPGA temp
- Provides very useful board management from command line, i.e. to recover boards if they get stuck in an unusual state

✓ We have used both Vadatech and NAT MCHs and found NAT generally more reliable

✓ Very important to keep firmware on MCHs up-to-date, as frequent bug-fixes are released

AMC 13

- Mounts in redundant MCH slot of MicroTCA crate
- Distributes 40.xxx MHz LHC clock on MicroTCA CLK1 (M-LVDS)
- CLK40 input through front panel SFP, optical fibre from Trigger, Control and Distribution System
- Distributes Level-1 trigger accept signal and BC0 (zeroth bunch crossing)
- Collects DAQ data from all AMCs

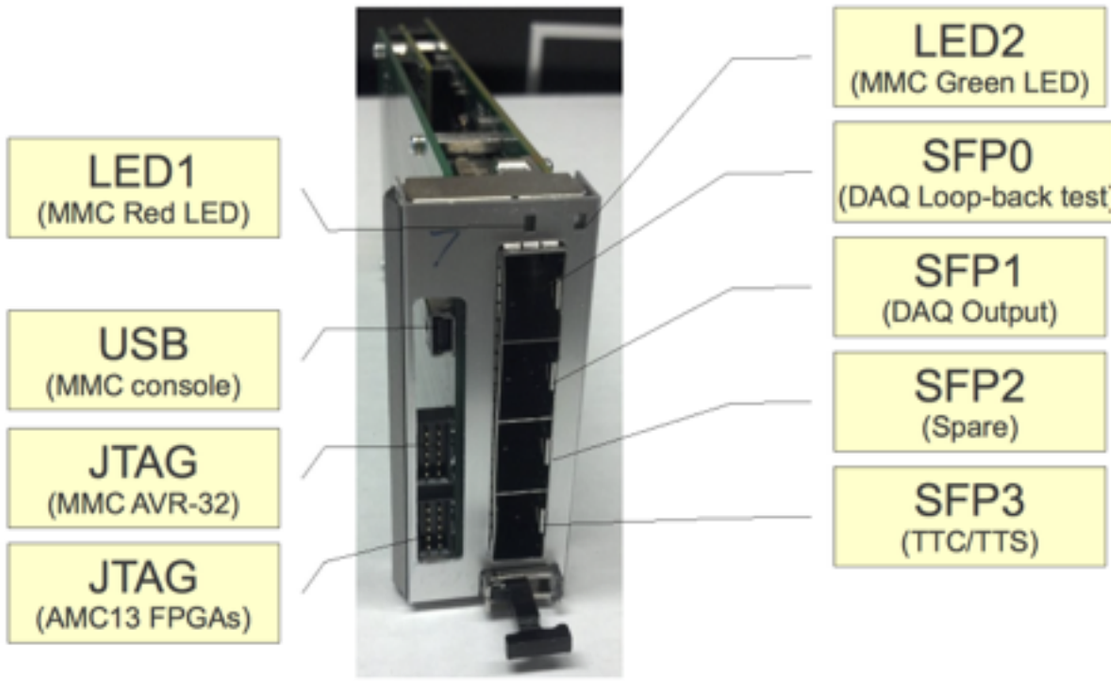
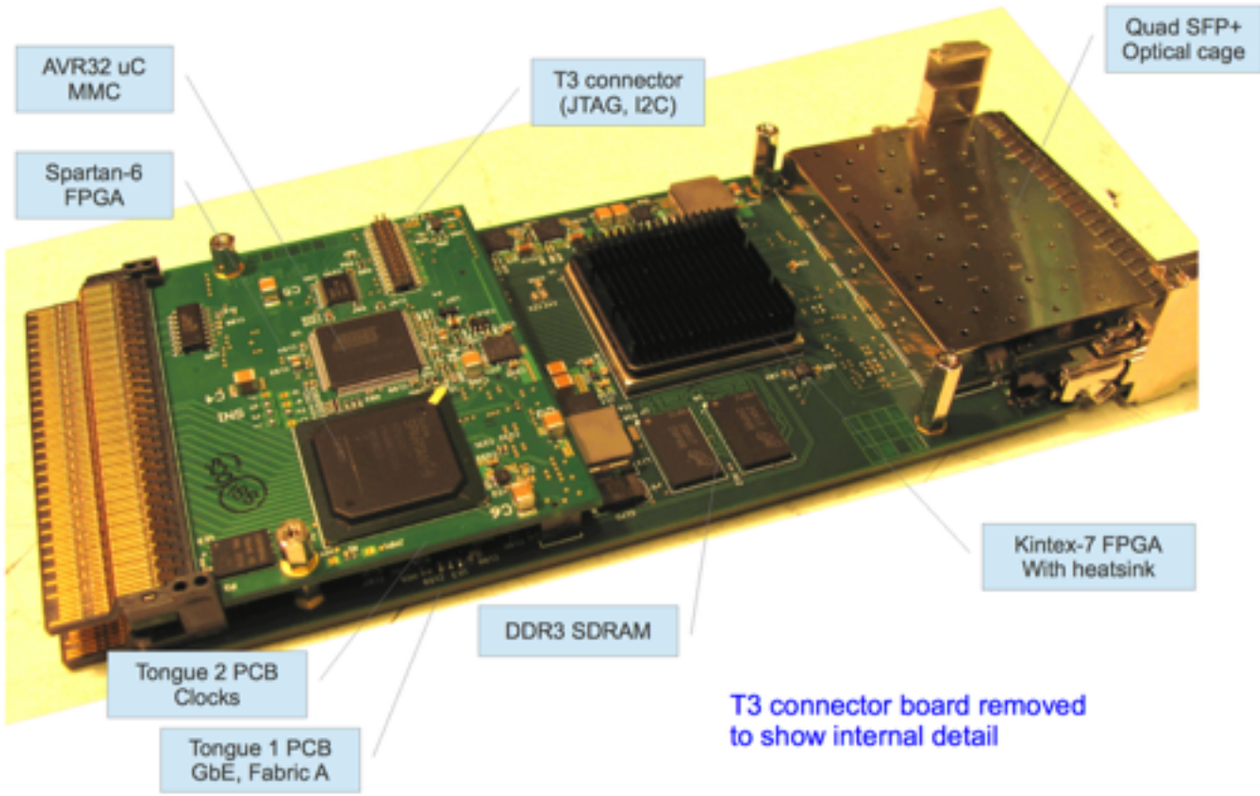
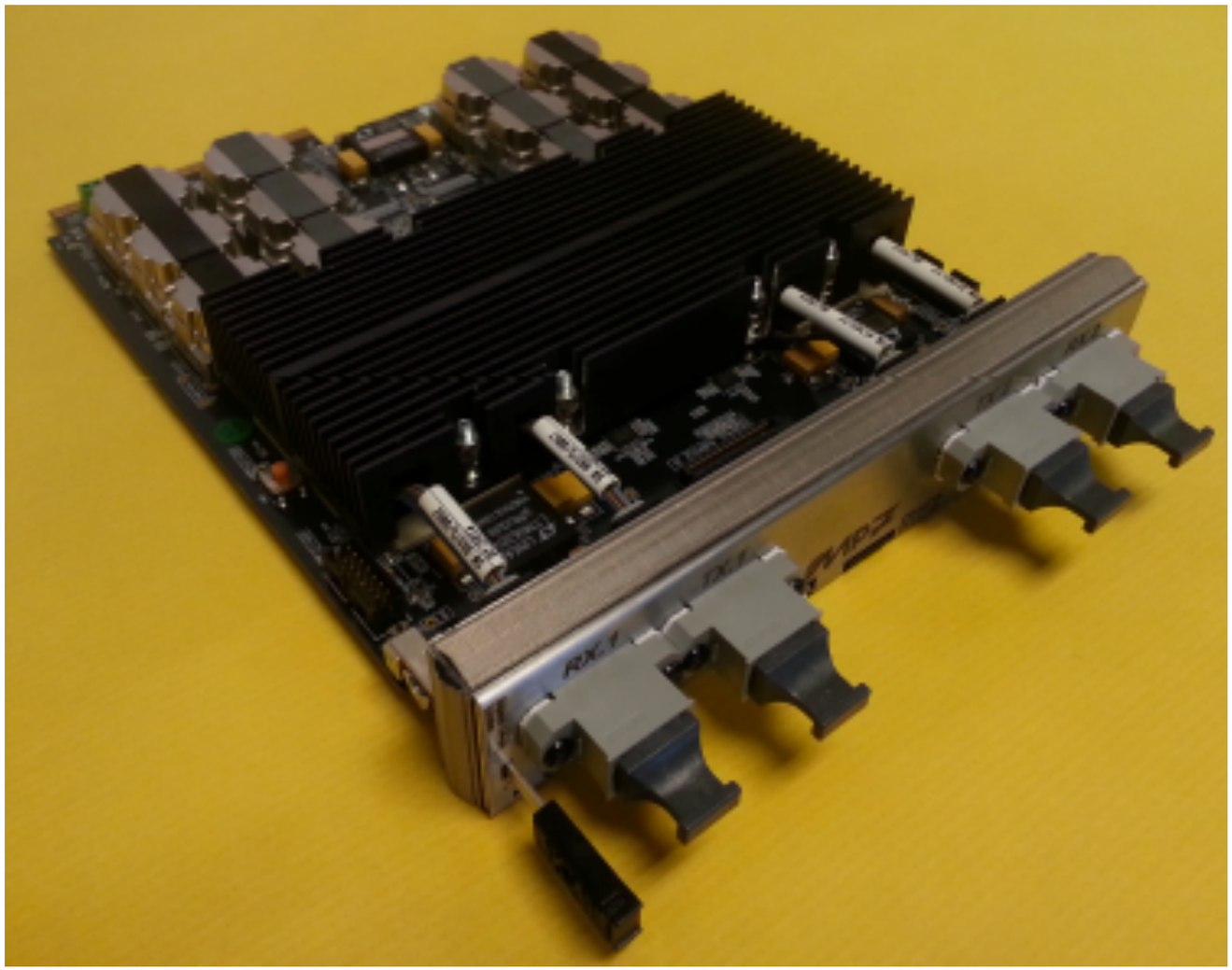


Illustration 1: AMC13 Front Panel



MP7

- Main workhorse for the calorimeter trigger
- 1.5 Tb/s signal processor board
- Xilinx XC7VX690T FPGA
- 72 Tx + 72 Rx links @ 10 Gb/s
- Average MiniPOD embedded optics
- uTCA form factor
- GbE, AMC13TTC/TTS, PCIe, SATA, SRIO backplane links
- ACR UC3A3256 microcontroller
- MicroSD for FPGA booting & firmware repository
- Very well understood
- Software and firmware in advanced stages

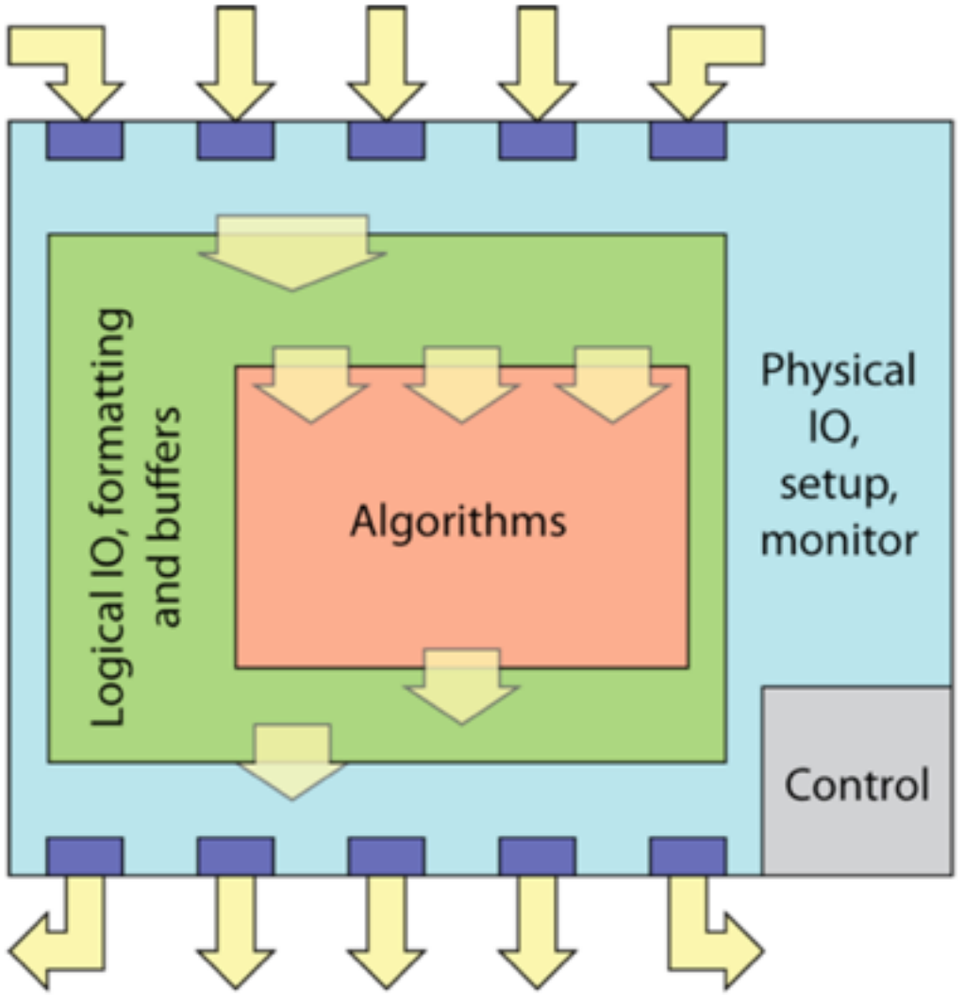


MP7 Firmware

- MP7 is a generic data-stream processor suitable for many applications
- For flexibility to be maximised, firmware must also be sufficiently generic
- Firmware abstracted into distinct regions to facilitate user development

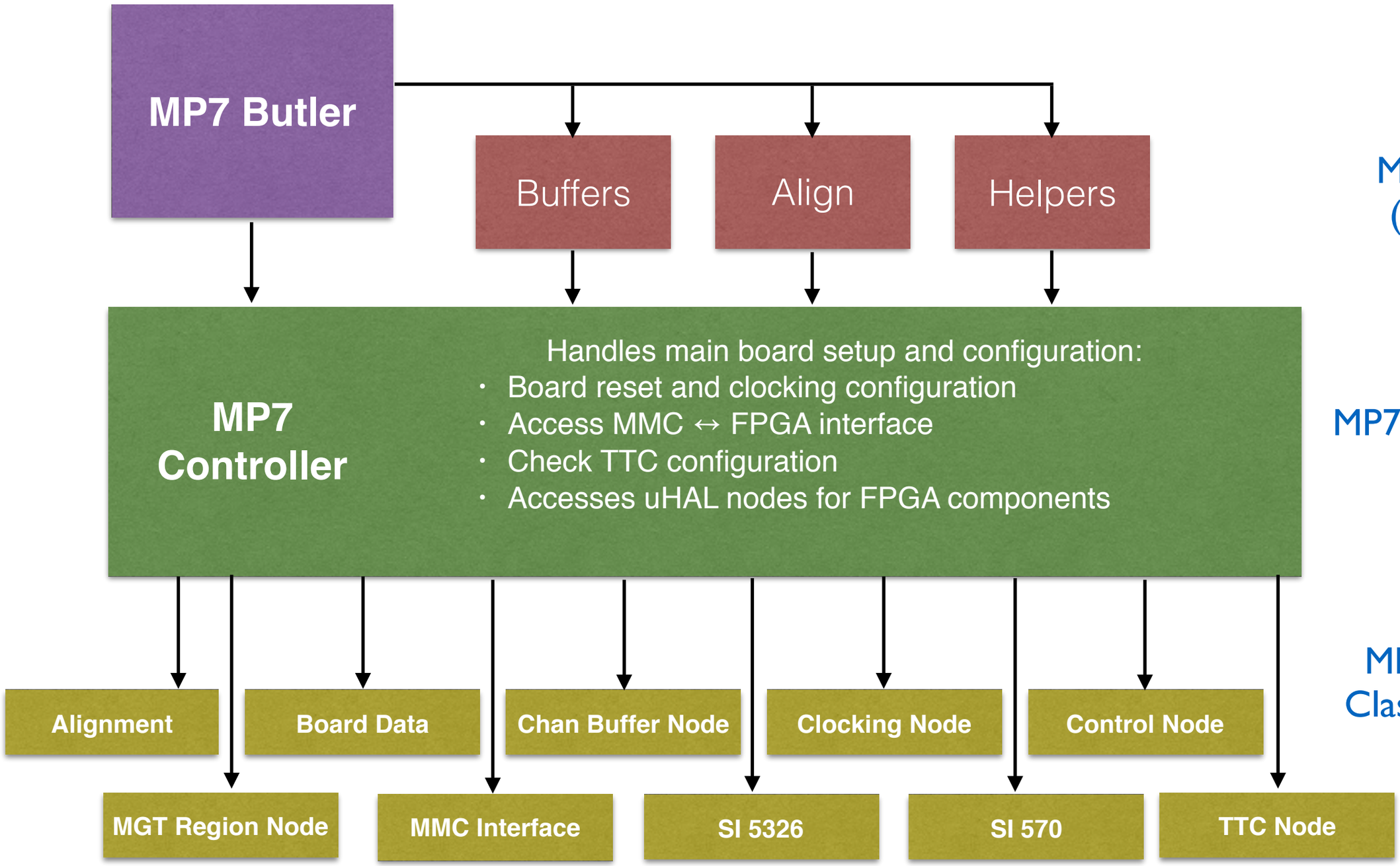
Core firmware is composed of following:

- Data enters/leaves FPGA through multi-gigabit transceivers and DAQ buffers
- Global (latency/alignment) and local (protocols, line rates, error checking) link control via dynamic reconfiguration ports
- FPGA control/configuration is done over IPbus
- Clock routing (one of main challenges)
- Microcontroller interface (access to uSD)



MP7 Software

Main control script (python)
Run from command line



MP7 tools (python)

MP7 Controller (C++)

MP7 Driver Classes (C++)

IPbus

slide credit: Tom Williams

- IPbus: A simple Ethernet-based control protocol
  - Designed for controlling Ethernet-/IP-based hardware – i.e. read/write registers, etc.
- Suite of firmware and software:
  1. IPbus firmware core
     - Reference VHDL implementation of IPbus 2.0 UDP server
     - Complete system-on-chip implementation
     - Interprets and implements IPbus transactions (read, write, …) on FPGA
  2. uHAL library
     - C++ and Python end-user Hardware Access Library
     - Design mimics recursive modularity of firmware blocks
  3. ControlHub
     - Software application analogous to VME crate controller
     - Mediates/Arbitrates simultaneous hardware access from multiple clients
     - Implements IPbus reliability mechanism
- Widely used: CMS, ATLAS & ALICE upgrades; FNAL g-2, SOLID, COMET, COMPASS
- Documentation, installation instructions, etc – http://cactus.web.cern.ch

Lessons learned

- Essential to have a coherent firmware development framework
  - ➡ very easy to lose track of what has changed in large complex project
- Software and firmware must be developed alongside one another
  - ➡ facilitates the testing of system & validation of new features
- Key is to have accessible lightweight software framework
  - ➡ worth investing time in modularisation
  - ➡ hugely facilitates modifications and additions further down the line
- Important to have remote access for all functions
  - ➡ speeds up development & allows support when required
- Careful tracking of seemingly small reliability issues that bite later
  - ➡ comprehensive ‘ticketing’ of bug fixes also a must
- Pay close attention to specifications & standards otherwise compliance issues arise

Future Prospect

- Many wider current and future applications for MP7 design: very flexible and powerful board that can be used in wider contexts
- 1 Tb/s source and sink of optical data can be utilised for future projects
- Current applications in CMS:
    - L1 Calorimeter trigger demultiplexer card
    - uGMT global muon trigger & uGT global trigger processor card
    - muon drift tube track finder
- Future applications:
    - 16 MP7's can simulate the entire tracker output (!)
    - Main processor for track-trigger Phase-2 upgrade
    - Requests from neutrino experiments: correlations between FE PMTs
    - Directly applicable to radio astronomy (e.g. SKA): require enormous optical bandwidth for beam-forming

Summary

- MP7 board has been a very successful transition from VME to MicroTCA
  - ➡ already in use / commissioning in a number of roles in CMS
- Non-trivial to develop firmware, especially for very large FPGAs
  - ➡ Absolutely essential to have a reliable test bench
- A flexible system is a key factor in the success of the MP7
  - ➡ Modularised firmware infrastructure makes it much easier to update/add/fix and for multiple developers to contribute efficiently
  - ➡ Flexible software architecture allows quick updates to accommodate changes in firmware without breaking system
- Already being commissioned in various roles for CMS upgrade
- Discussions ongoing for use in other areas of HEP and astronomy