Beam Tests of 3D Vertically Interconnected Prototypes

Matthew Jones (Purdue University)
Grzegorz Deptuch, Scott Holm, Ryan Rivera, Lorenzo Uplegger (FNAL)

PURDUE UNIVERSITY

Fermilab

This work supported by NSF CAREER award 6807134.

VIPIC Project

Vertically **I**ntegrated **P**hoton **I**maging **C**hip

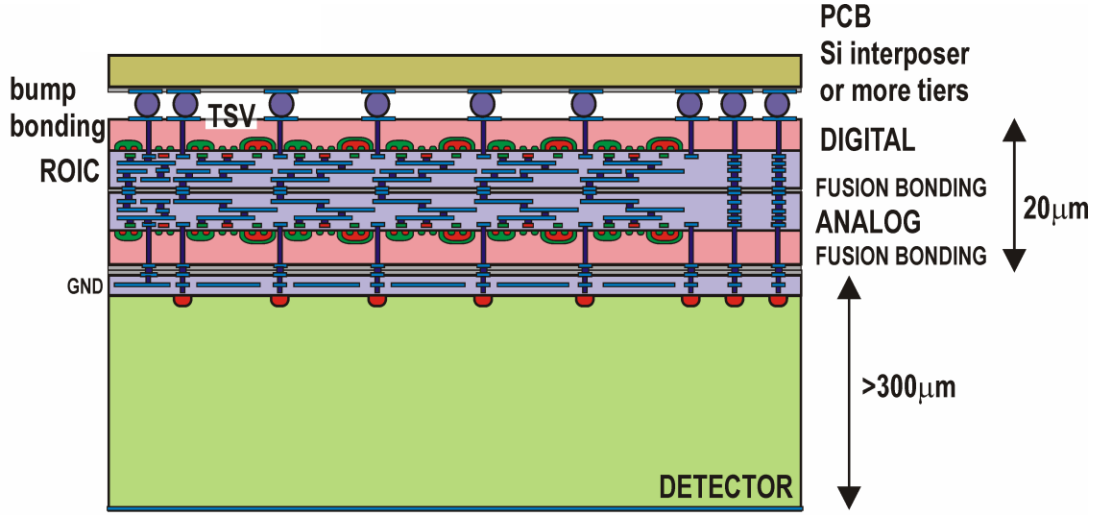
- Targeting X-ray photon correlation spectroscopy:
  - Current generation of cameras has 1 kHz frame rate
  - Next generation would like
    - Large detector area
    - Dead-time-less readout
    - Time resolution of 10 ns
    - Frame rates approaching 100 kHz
- Collaborating Institutes:
  - BNL, FNAL (US) and AGH-UST (Krakow Poland)
- Disclaimer:
  - Grzegorz Deptuch and others are the real experts

INFIERI Demonstrator

- We developed the test beam facility, but not the VIPIC chip
  - We worked closely with the developers on their integration
- First example of a 3D pixel device read out in a test beam with protons (as opposed to x-rays at Argonne)
- Excellent example of a WP6 demonstrator:
  - Novel device architecture
  - General purpose test facility
- Community benefits:
  - Moving this technology closer to being regarded as mature enough to be considered for future projects

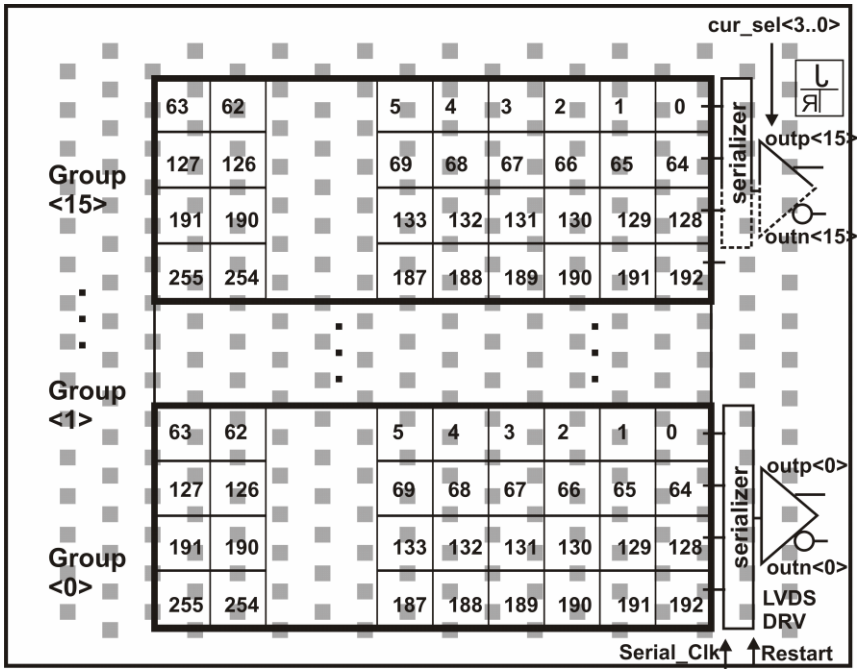
Technology

- Analog and digital circuits fabricated on different layers, interconnected using through silicon vias, wafer thinning, fusion bonding
- No dead areas at the edges – multiple devices can be butted together



Design

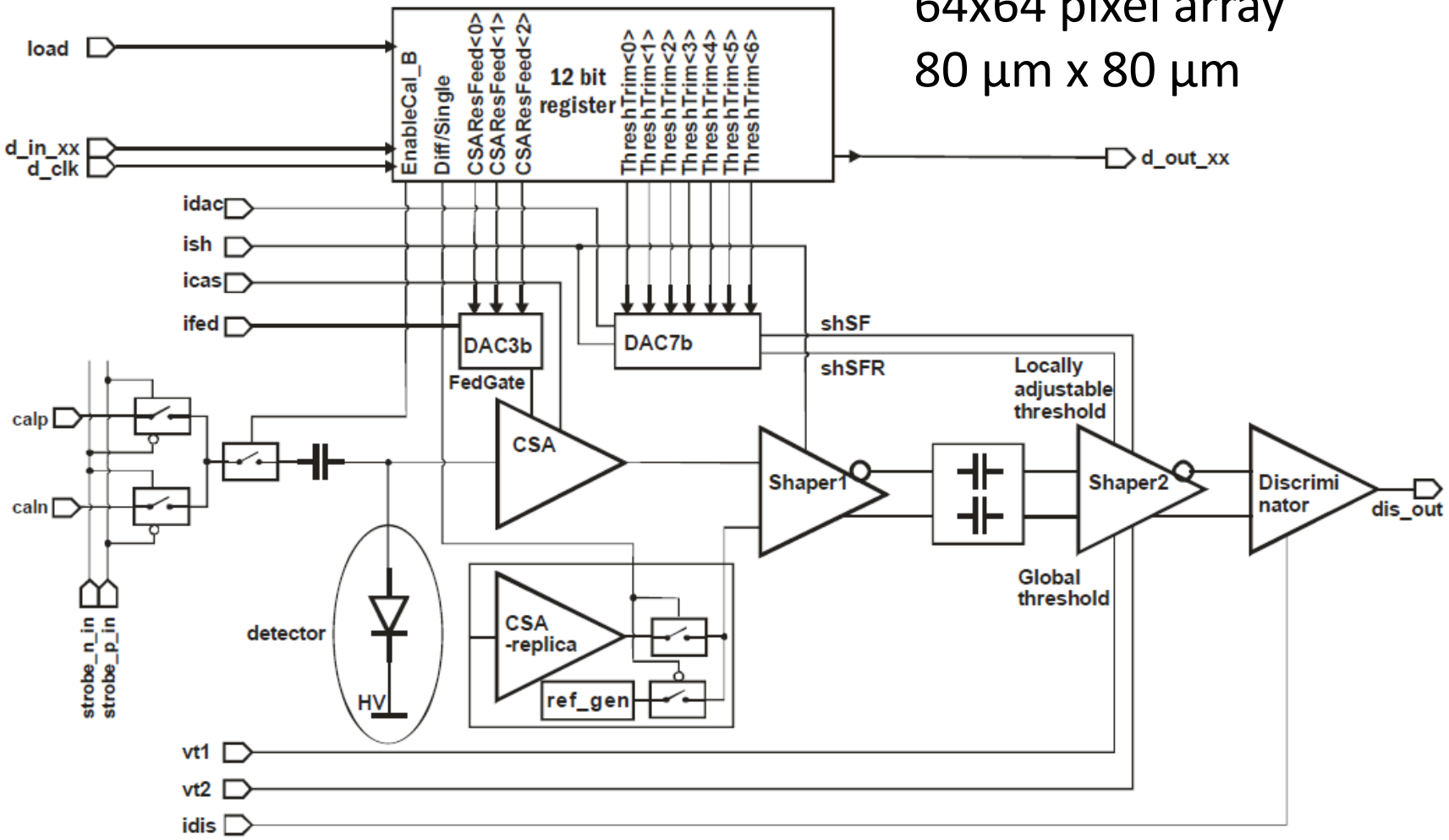
- 5120x5120 µm^2
- 64x64 pixel array (80 µm pitch)
- Readout divided into 16 groups of 256 pixels
- Priority encoder selects hit pixels for readout



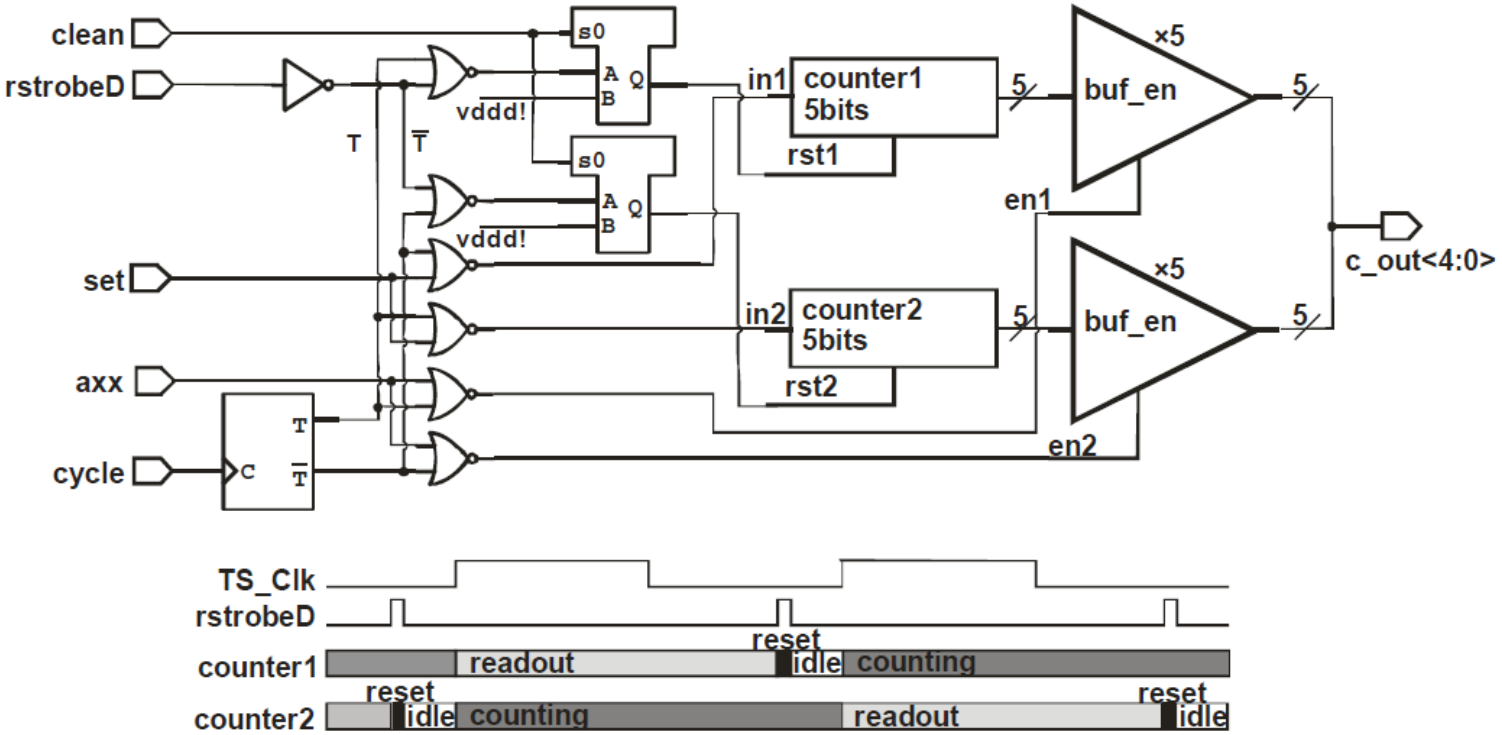
- Single threshold discriminator
- 2 5-bit counters per pixel
- 12-bit configuration register per pixel
- 1-bit mask-off register
- 1-bit mask-on register

Analog Section

64x64 pixel array
80 µm x 80 µm



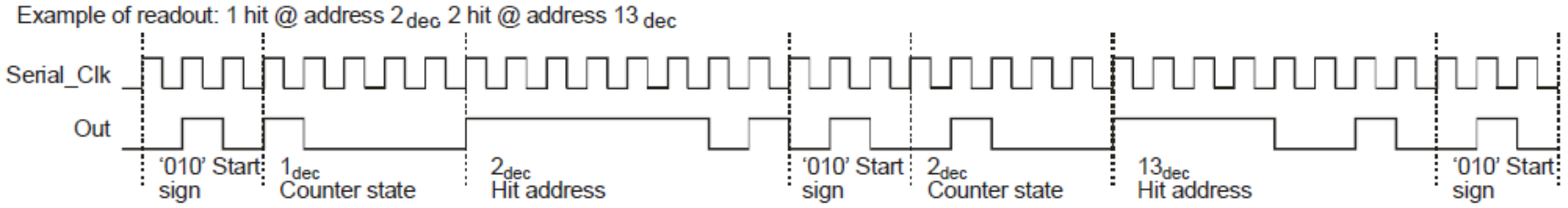
Digital Section



- Two 5-bit counters count pulses between *TS_Clk* edges with no deadtime.
- Counters alternate on rising edge of *rstrobe* signal.

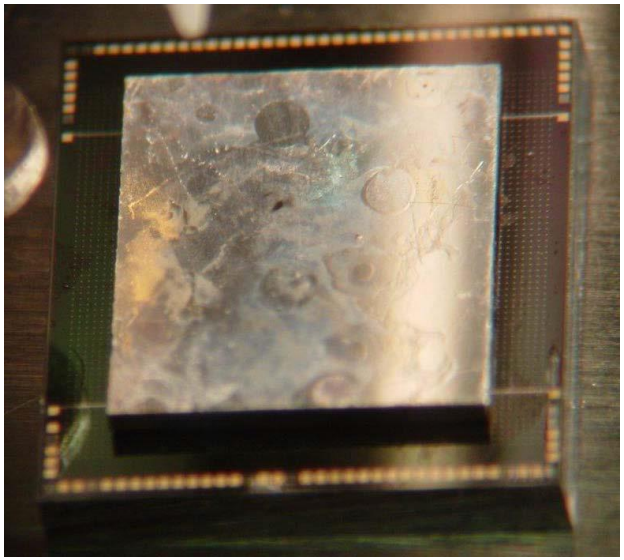
Digital Section

- 16 independent channels of 256 pixels
- Sparsification engine selects highest address of pixel with non-zero counts
- rstrobe signal switches counter of current pixel
  - If new count is zero, then another pixel is selected by the priority encoder
  - When all counters are zero, the *hit_or* signal goes low
- Serial data can be read out at around 100 MBPS:



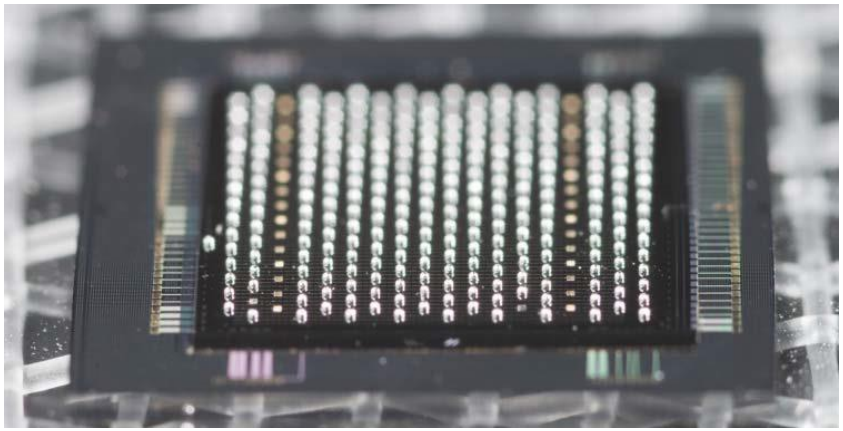
VIPIC Evolution

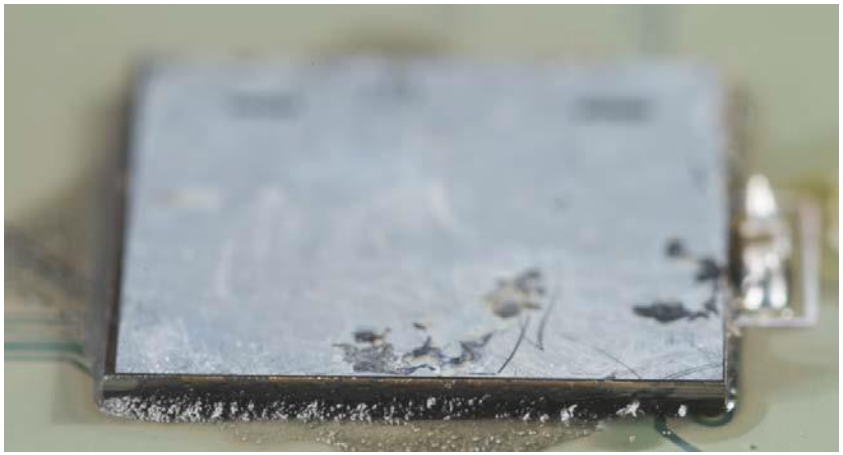
Previous versions



VIPIC bump bonded to 300 µm thick sensor, wire bonded to carrier board. Sensor had 32x38 pixel array.

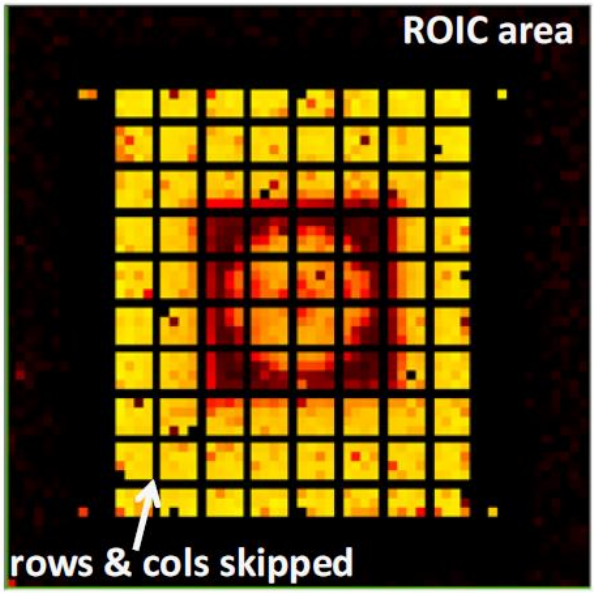
Now…

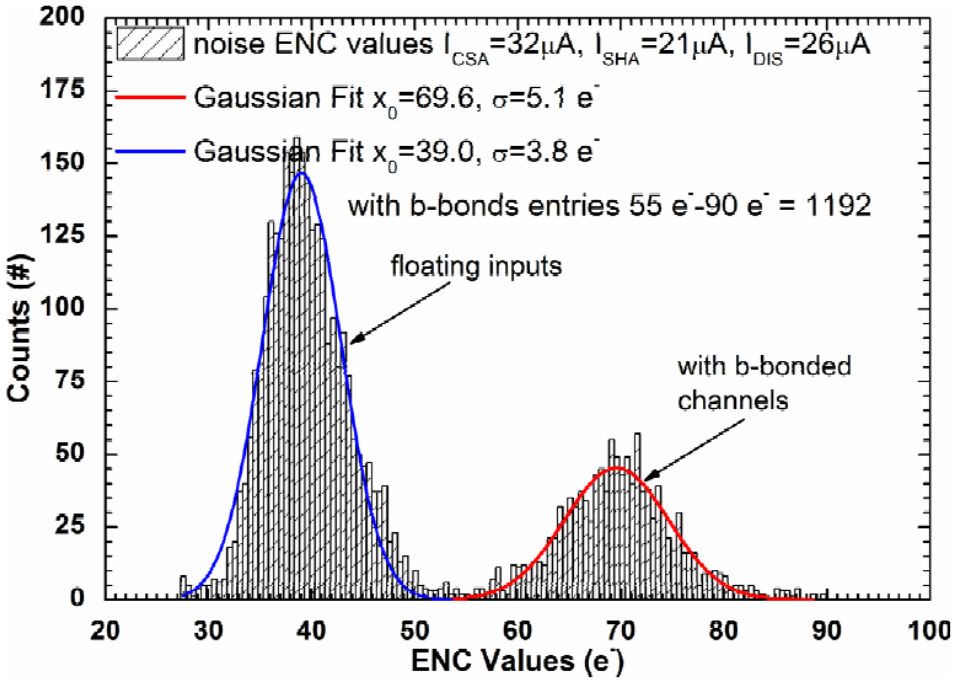




Directly bonded to 500 µm thick sensor and bump bonded to carrier board.

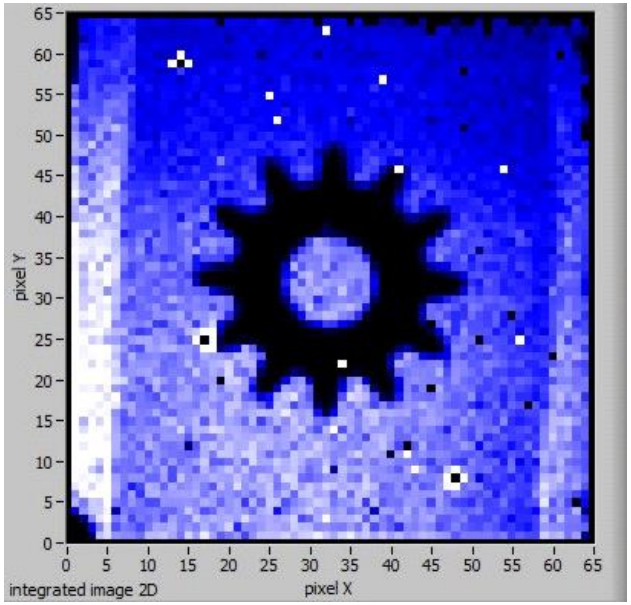
VIPIC1 Performance

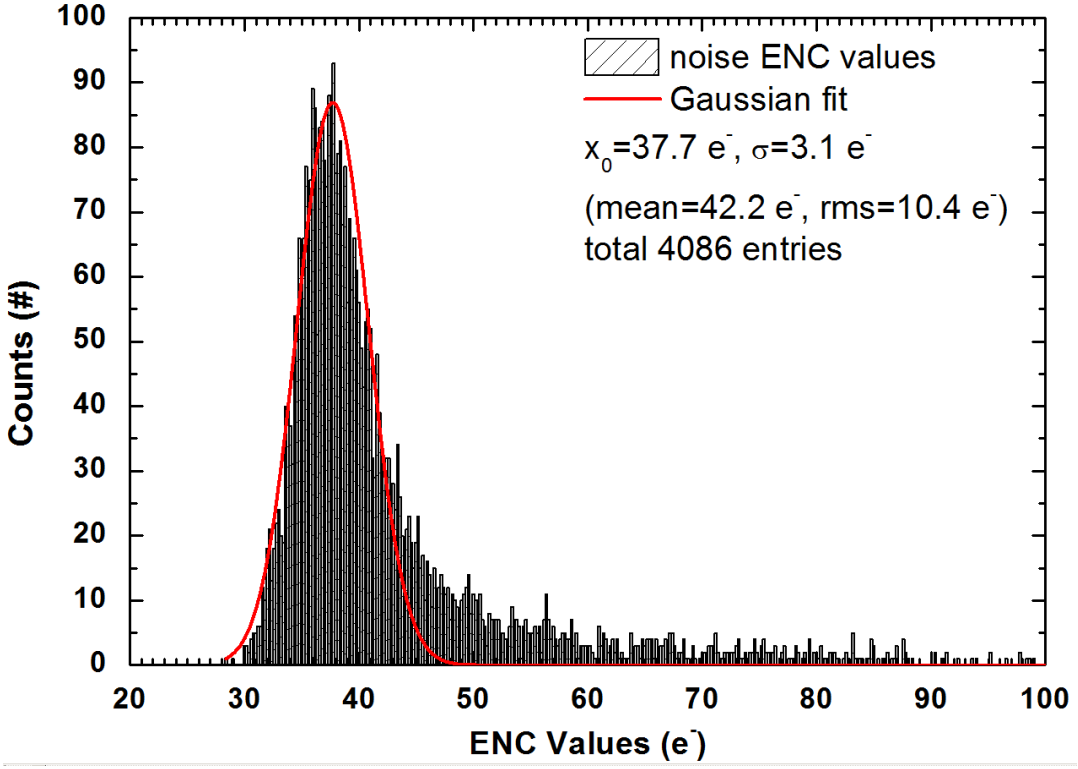




- Calibration charge injection corresponding to 4.5 keV x-ray
- Connected pixels see larger input capacitance

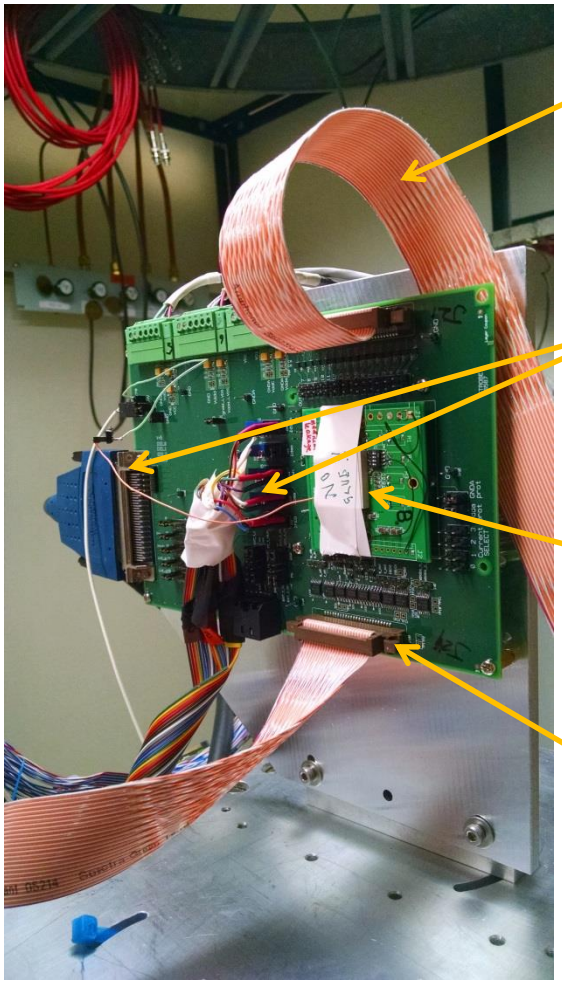
VIPIC Performance





- Much lower input capacitance when pixels are directly bonded to sensor Ni-DBI

Electrical Interface



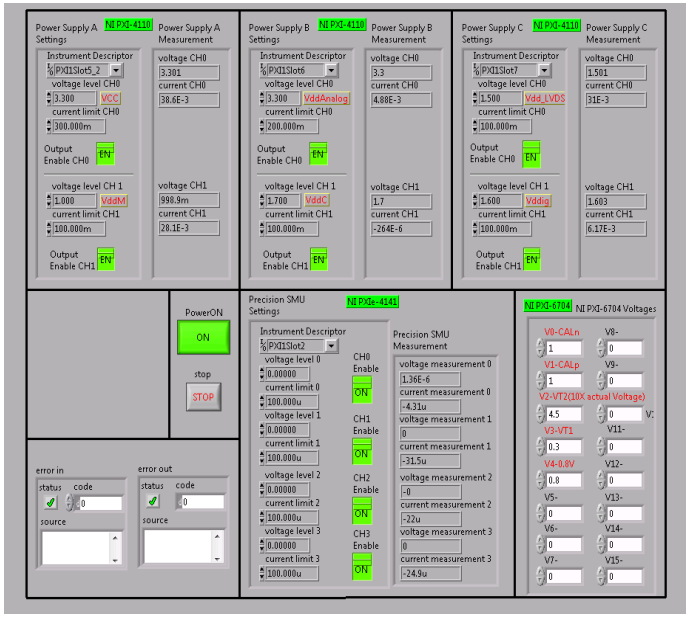
16 LVDS serial data

Power and analog voltages

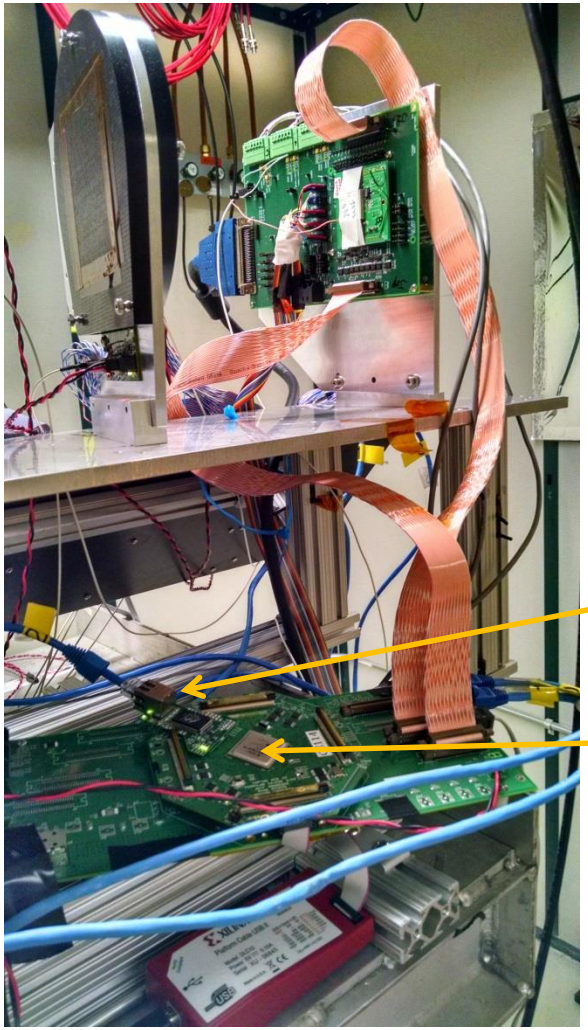
VIPIC chip

Control signals

Analog voltages, discriminator threshold are configured using National Instruments hardware with a Labview interface.



Electrical Interface



Same FPGA interface used for reading out the strip sensors in the telescope

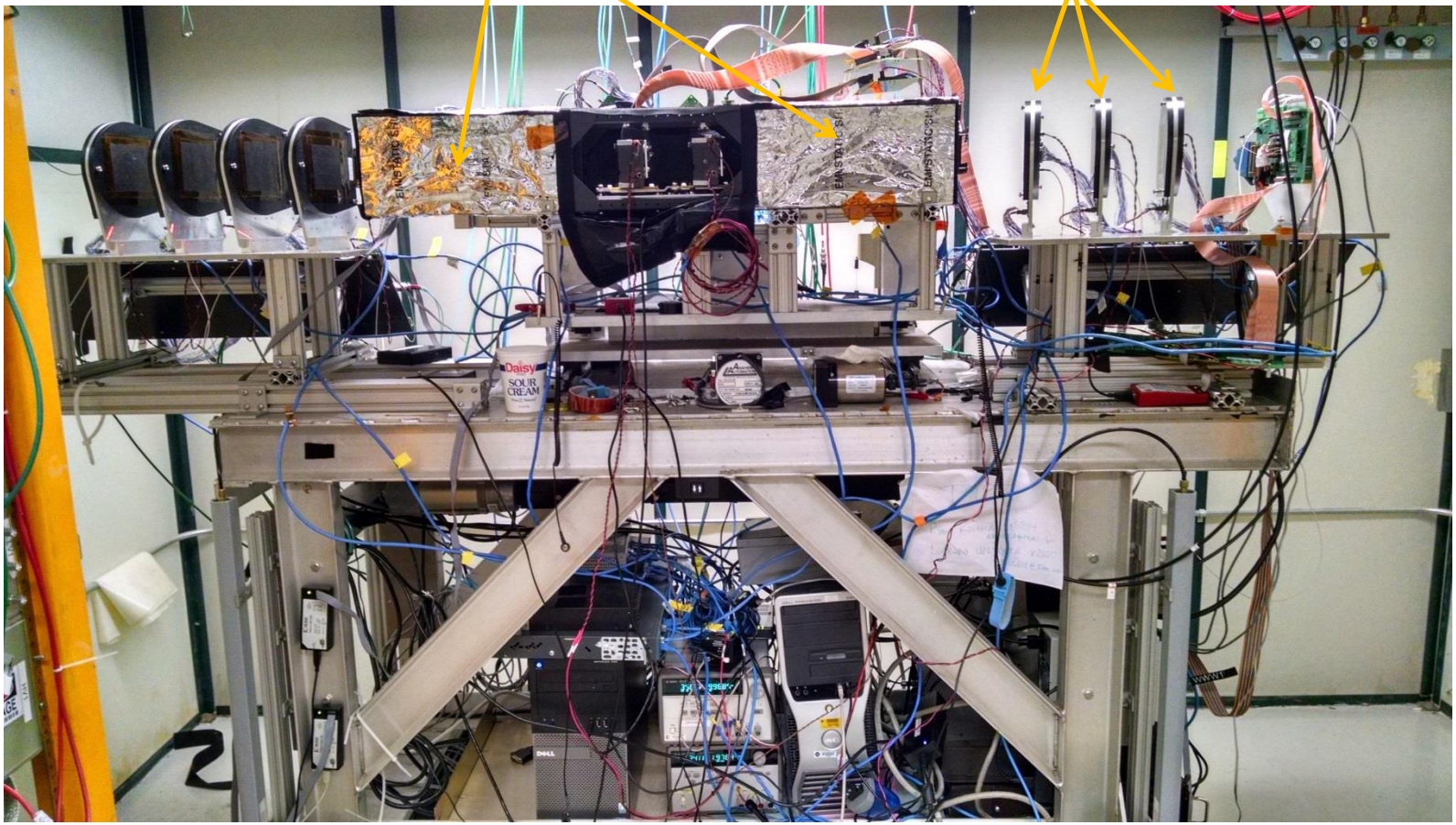
1 GbE network interface

FPGA for configuration, clock generation and readout.

Telescope

Pixel telescope for PSI46 readout (legacy hardware)

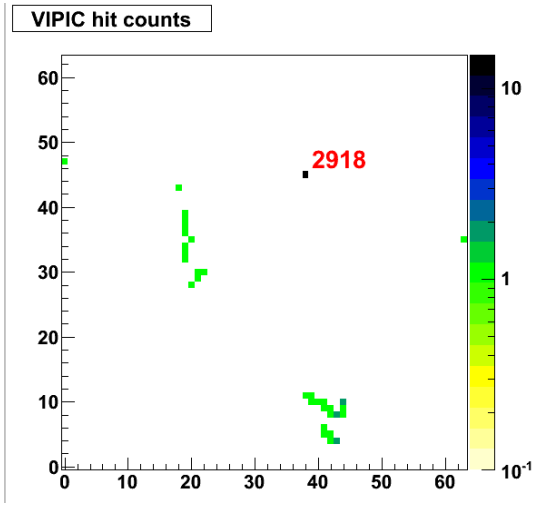
Only 3 downstream x-y planes used to extrapolate tracks into the VIPIC.



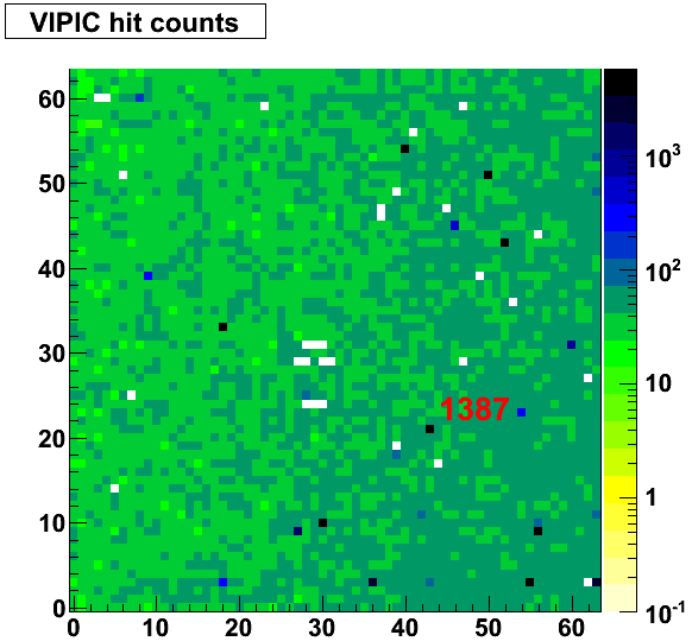
Telescope

- Readout of the strips is distributed over 3 FPGA's
- *TS_clock* in the VIPIC readout is distributed to the other FPGA's over Cat-5 cable
- No trigger – continuous dead-time-less readout of VIPIC and strips
- All hits are tagged with a 48-bit bunch counter with 80 ns period, common to all FPGA's
- Data is streamed over the network, assembled into events and analyzed offline

Noisy Pixels

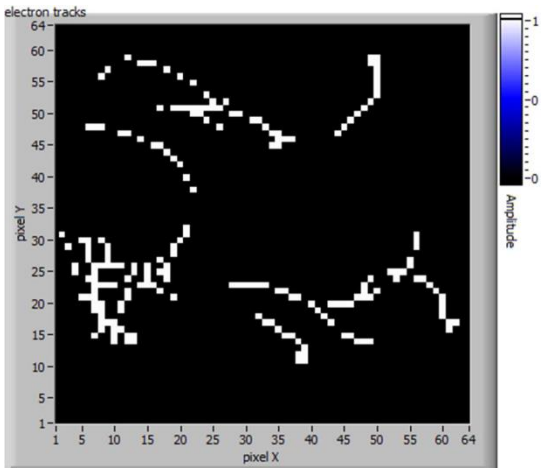


Tracks from cosmic rays.



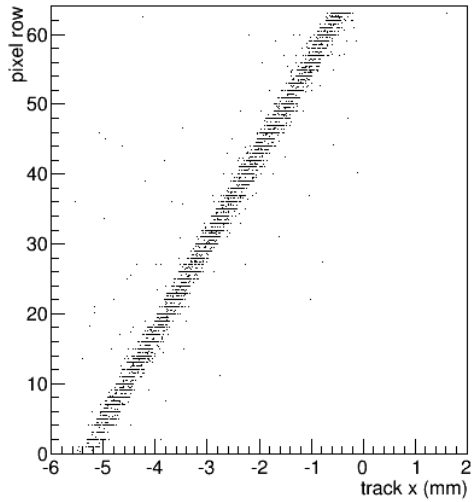
Occupancy from test beam.

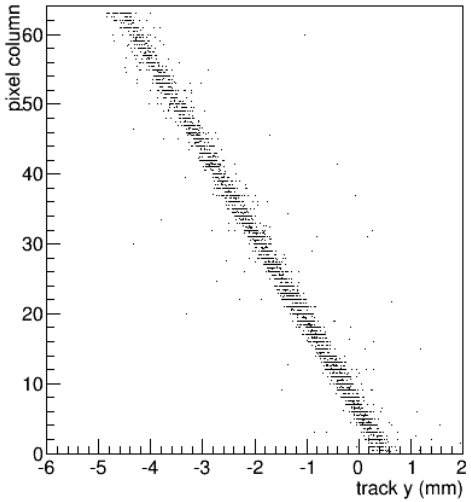
- Black pixels are noisy.
- White pixels are masked off.

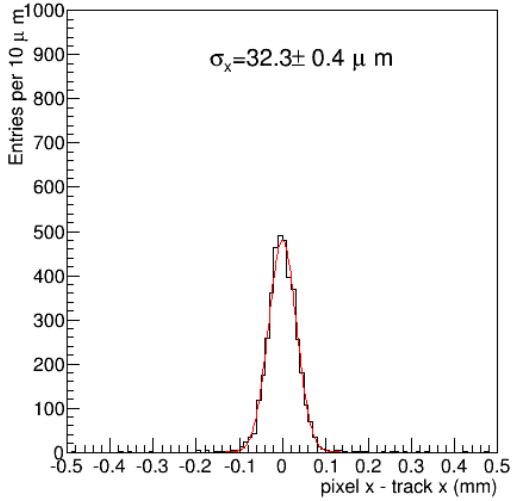


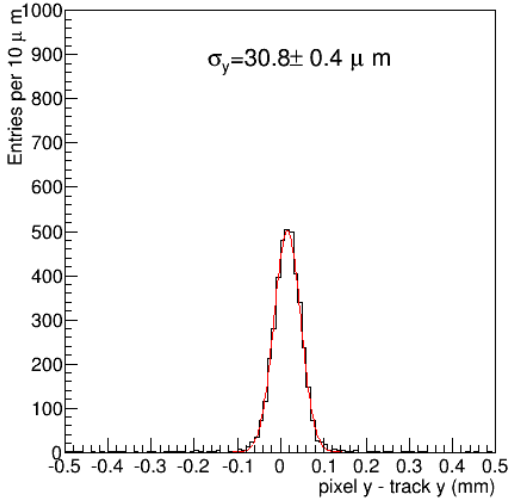
Electron tracks from Sr-90 source

Preliminary Telescope Alignment









December 3rd runs taken with 32 GeV protons – normally prefer 120 GeV.

Intrinsic resolution expected to be $(80\ \mu m)/\sqrt{12} = 23\ \mu m$.

Alignment of the telescope is preliminary and some improvement is expected.

Not prepared to quantify efficiency yet – several noisy pixels were masked off and should be skipped in the analysis.

What's Next

- Would like to understand efficiency:
  - Continue analysis of data recorded in December
  - Next opportunity for new data in June
- Next phase of the VIPIC project:
  - 1 Mpixel VIPIC system is now funded by DOE-BES
  - Multi-laboratory effort: BNL-FNAL-ANL + AGH-UST
  - 2017 targeted completion date
- Good example of integrating new hardware into the test beam DAQ system.

Summary

- Successfully integrated readout of VIPIC with test beam data acquisition.
- Recorded over 10^8 tracks over several hours of parasitic running at 32 GeV
- Preliminary alignment performed
- Remaining studies:
  - Accurate efficiency measurement
  - Increase *Serial_clk* frequency
  - Timing characteristics
- Successful WP6 demonstration