Status of Tracking Trigger Demonstration Test Bench Development at FNAL

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Fermilab

on behalf of the AM-FPGA team

Outline

- Overview of L1 tracking trigger project
- Plans for partial and full-scale demonstration
- Highlight of the recent progress in each of the areas needed for demonstration
  - Pulsar 2B status
  - IPMC/XVC work and remote access
  - Data sourcing and data delivery
  - Pattern recognition mezzanine card
- Summary

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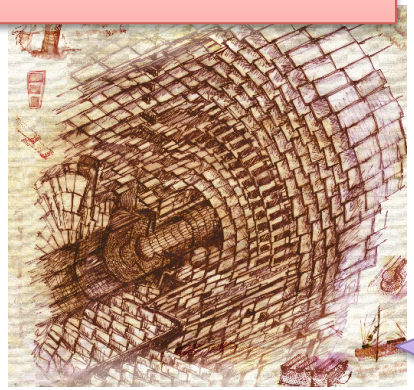
L1 Tracking Trigger challenges at HL-LHC

Detector design for triggering



Data transfer

Data formatting

Partition detector into trigger towers

Pick your favorite method:

Associative Memory Approach,
Hough Transformation,
Tracklet-based,
Adaptive Pattern Recognition,
Biology Inspired …

Pattern Recognition

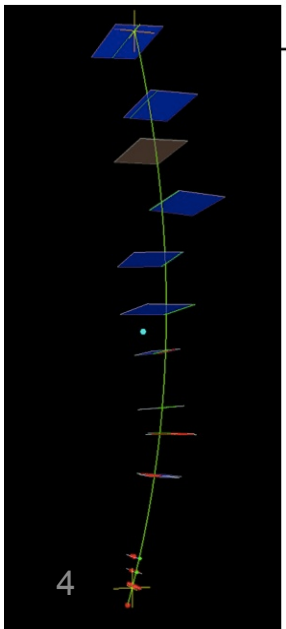
Finer pattern recognition

Track Fitting

- *Challenging issues*
  - *(1) Data Reduction at detector/sensor stage*
  - *(2) Data Transfer (rad hard, high bandwidth, low power link)*
  - *(3) Data Formatting*
  - *(4) Pattern Recognition*
  - *(5) Track Fitting …*

} Tracking Trigger

This talk will only cover the AM+FPGA approach

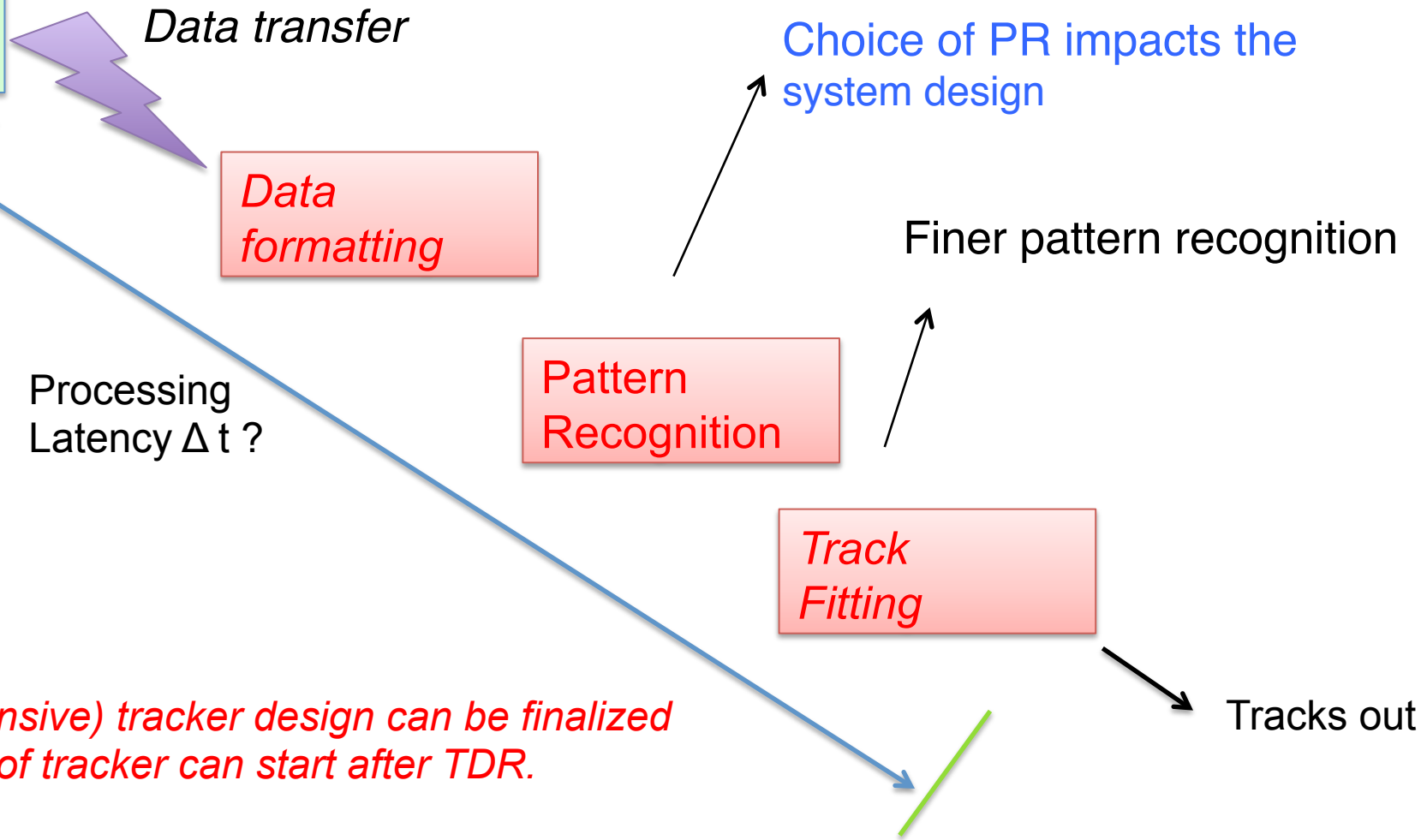


Detector design for triggering

L1 Tracking Trigger demonstration

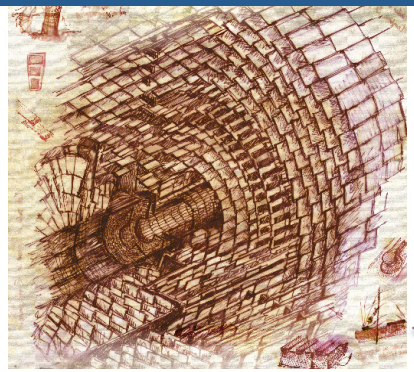
Emulate tracker output using HL-LHC simulation data

The feasibility of CMS L1 Tracking Trigger has to be demonstrated before TDR (~2017), using today's technology and then extrapolate into future

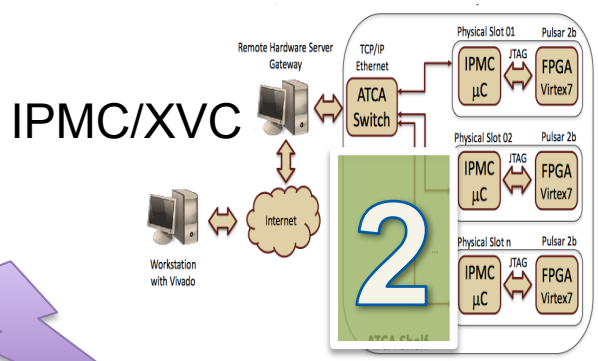


So that the (expensive) tracker design can be finalized and construction of tracker can start after TDR.

FNAL AM+FPGA based Tracking Trigger R&D for HL-LHC

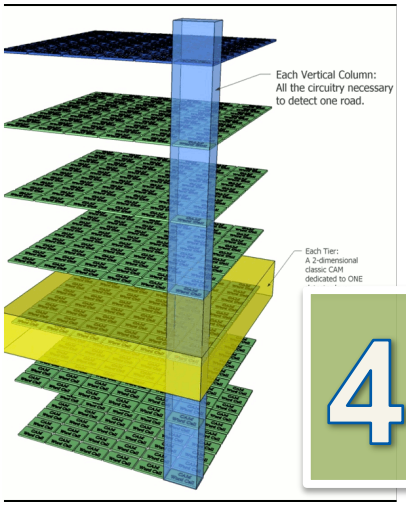


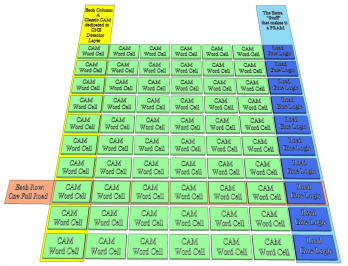
L1 Track Trigger architecture

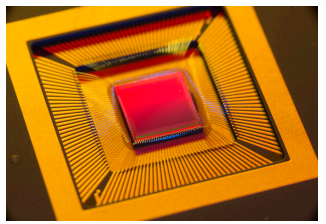


Data formatting

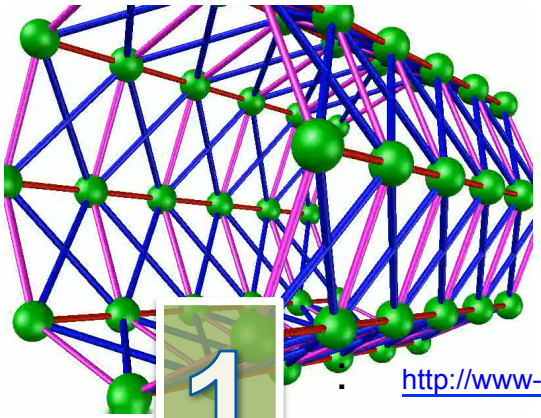
VIPRAM in 3D (DOE CDRD)





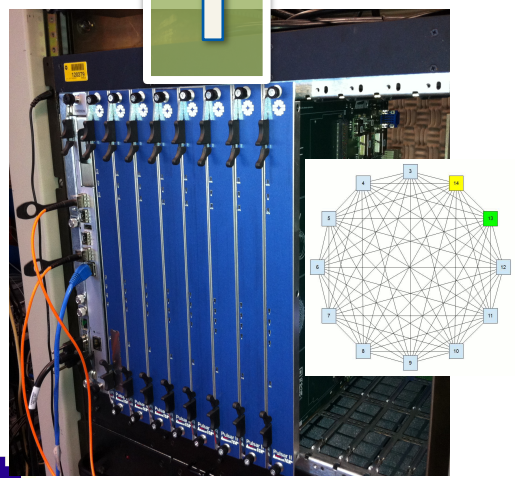


VIPRAM:
Vertically Integrated Pattern Recognition Associative Memory
http://www.sciencedirect.com/science/article/pii/S1875389212019165

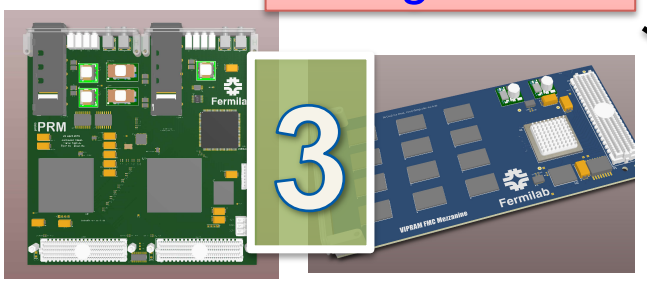


Pattern Recognition

ATCA
http://www-ppd.fnal.gov/EEDOffice-w/Projects/ATCA



Track Fitting



Tracks out

Pattern Recognition Mezzanine (PRM)

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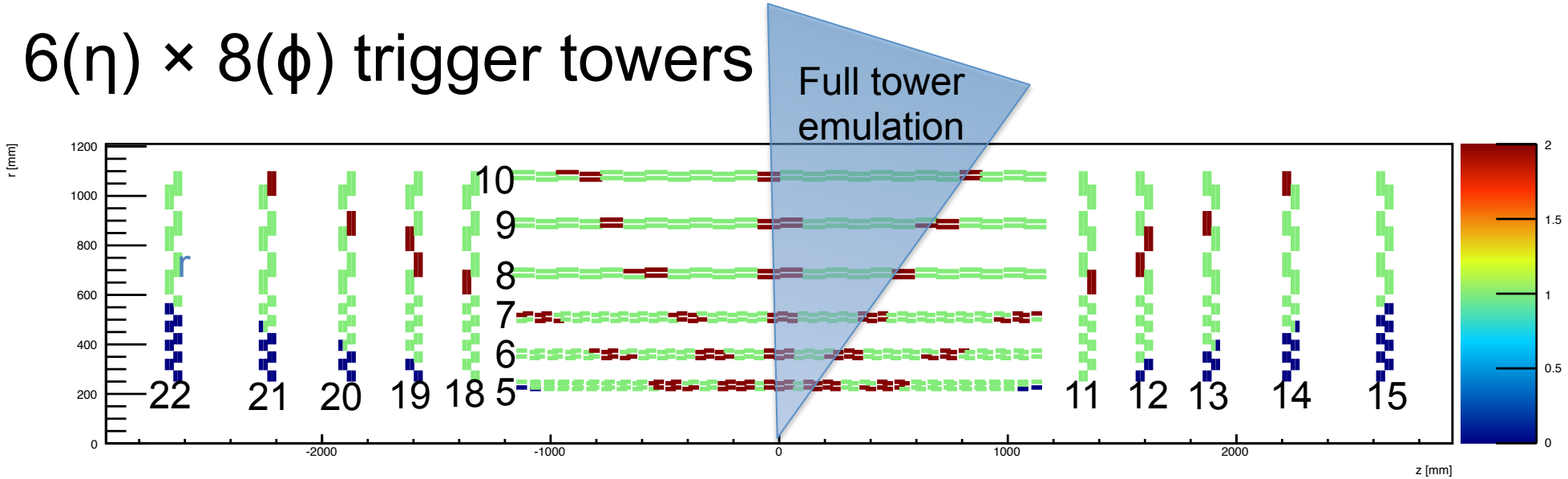
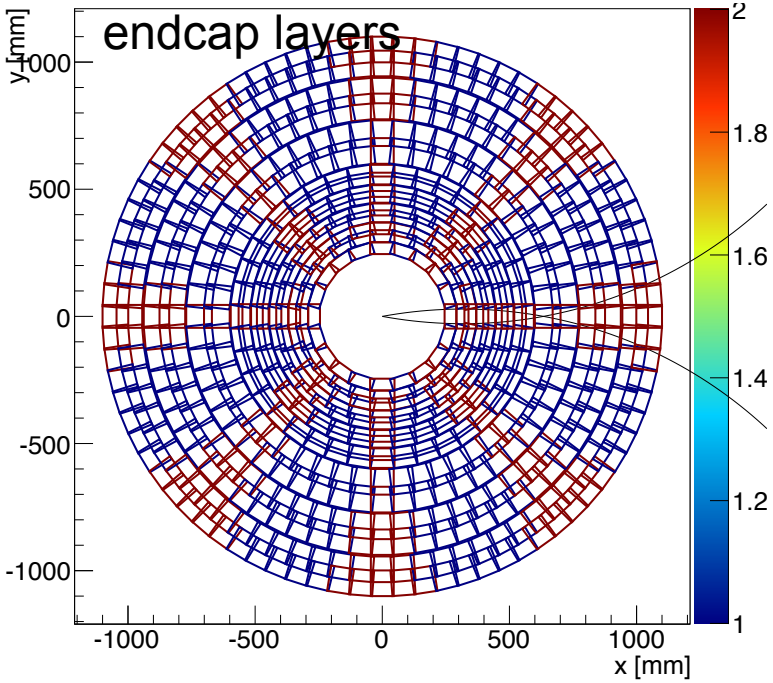
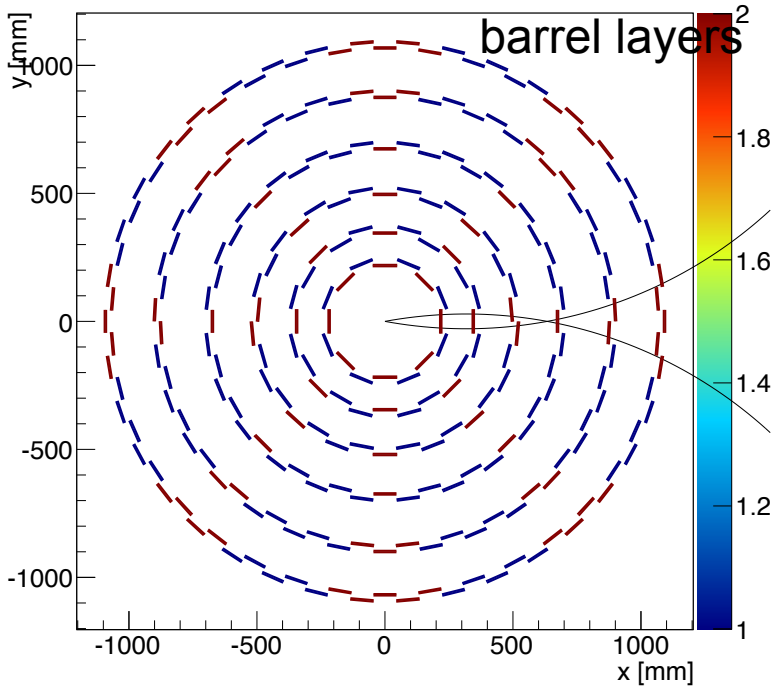
CMS outer tracker and trigger towers

- 6(η) × 8(ϕ) trigger towers







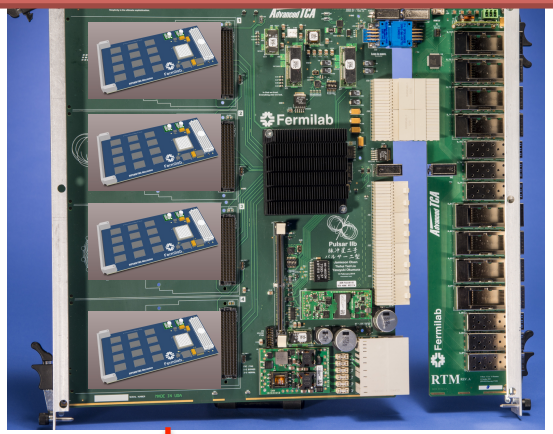
Trigger tower details: http://mersi.web.cern.ch/mersi/layouts/.repository/TechnicalProposal2014/trigger_cpus.html

Full-Scale Demonstration in 2016

- Data Source crate will emulate the output of DTC: 400 fibers worth of data from one Trigger Tower
- Includes neighbor data needed for this Trigger Tower

All 10 PRBs take turn to process events

Pattern Recognition Board (PRB)



Data Sourcing Boards

400 optical links

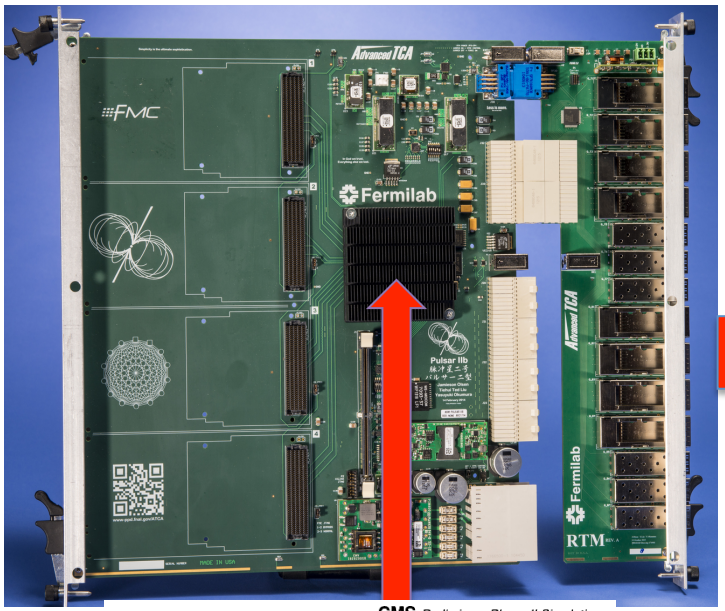
via full-mesh backplane

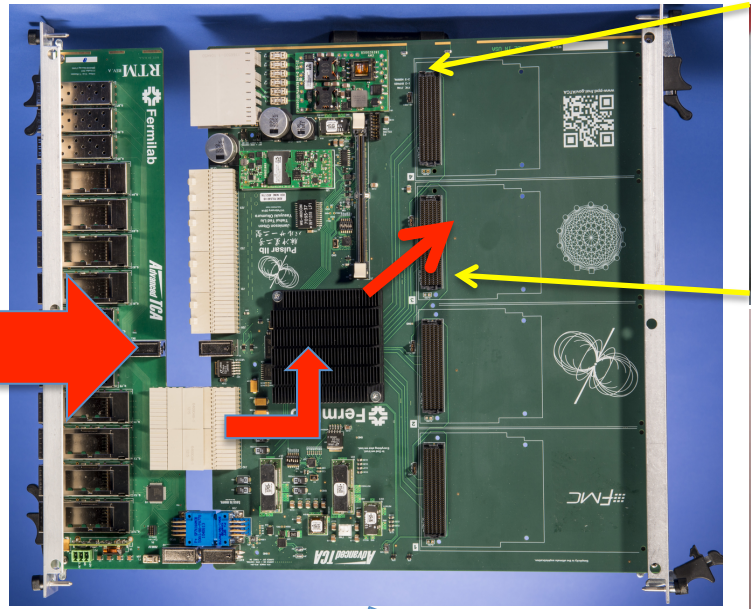
Target PRB

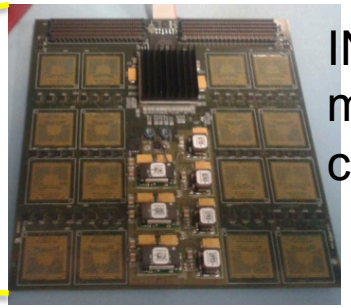
Initial Demonstration in 2015

Data Source:
emulating ~40 modules

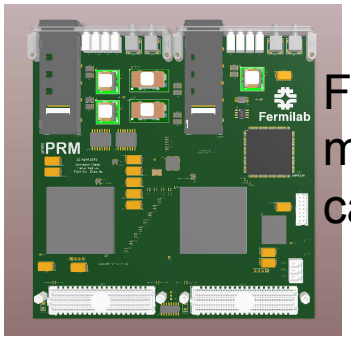
Δt1 (Data Delivery) + Δt2(AM) + Δt3 (TF)



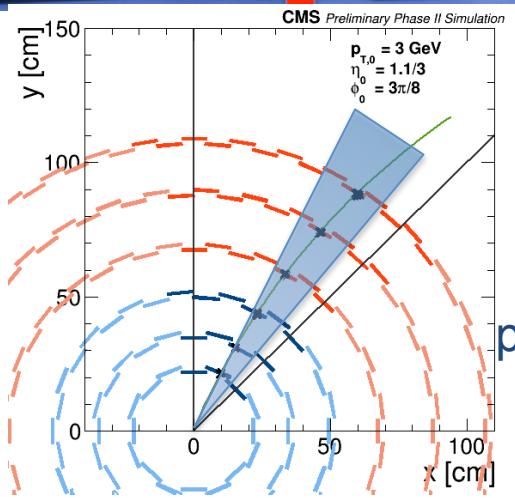




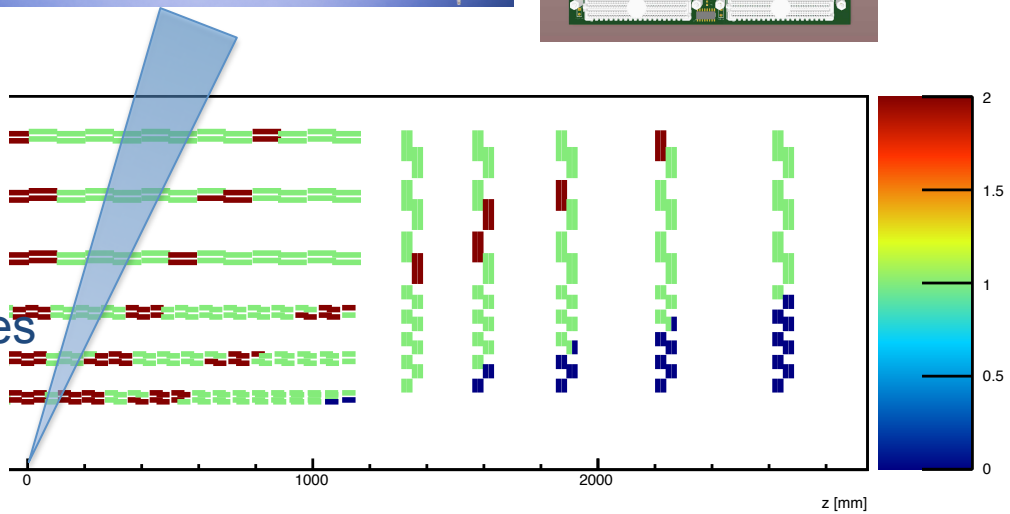
INFN mezzanine card



FNAL mezzanine card



pick ~40 modules



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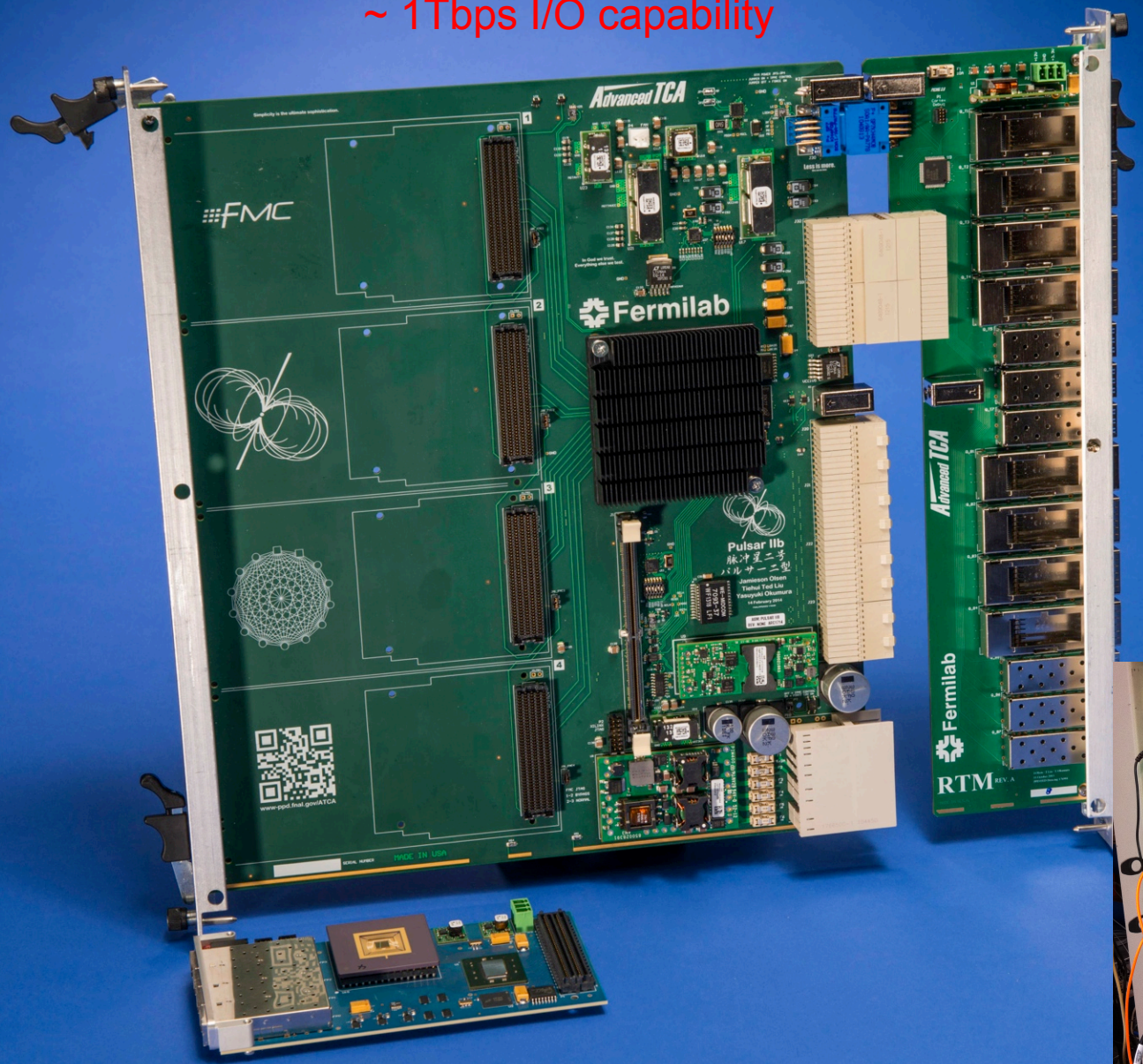
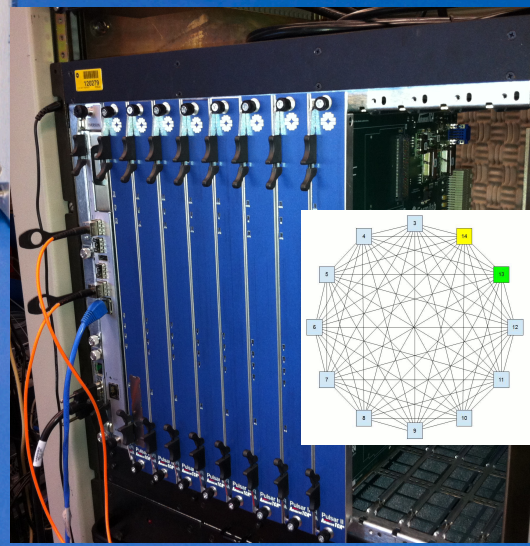
Pulsar II Web page: http://www-ppd.fnal.gov/EEDOffice-w/Projects/ATCA/
User information: https://twiki.cern.ch/twiki/bin/view/Main/PulsariibTesting

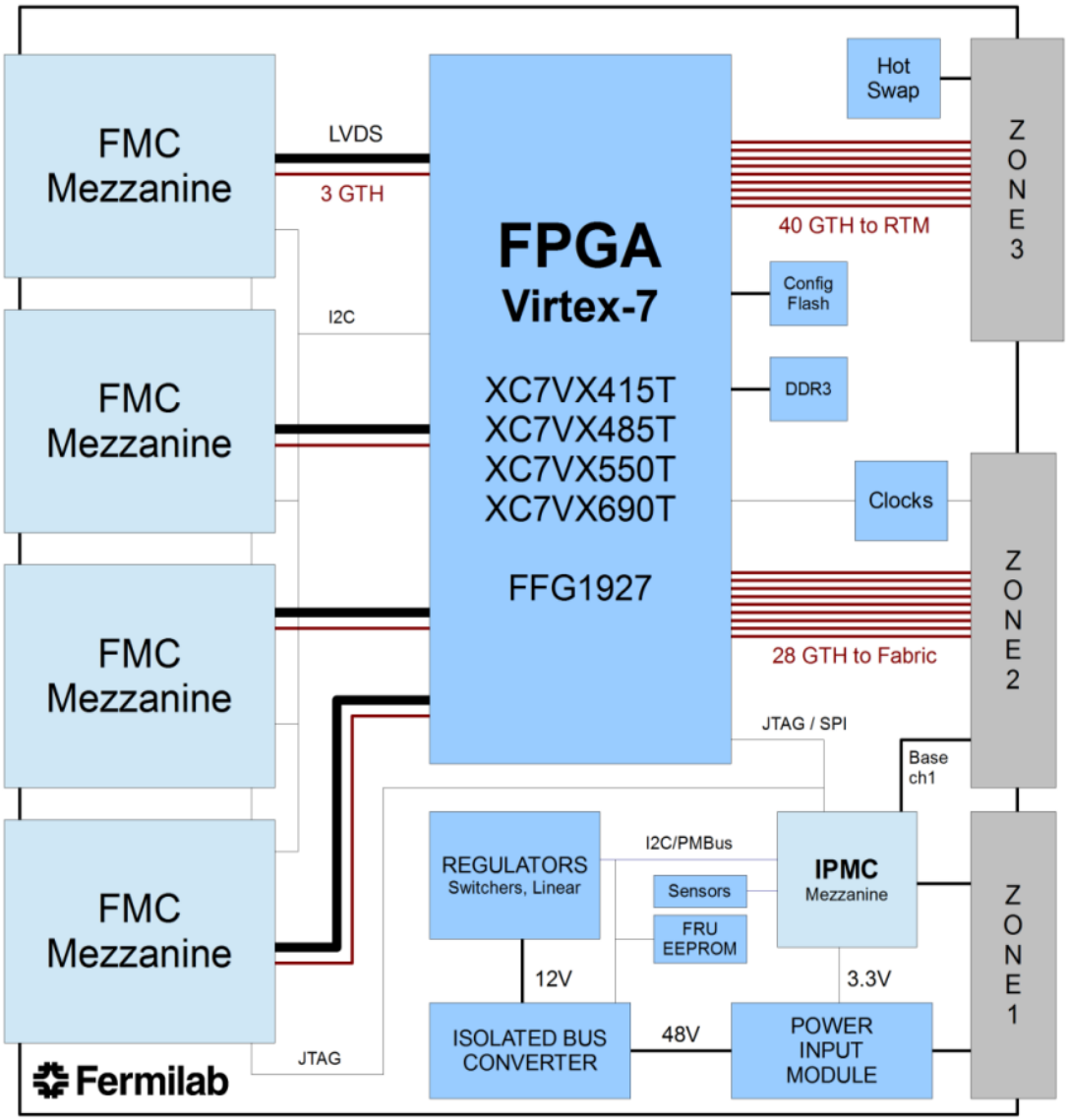
~ 1Tbps I/O capability





First board received on May 2013. So far no problem found after ~ 2 years extensive testing…

Pulsar 2B Features



Xilinx Virtex 7 FPGA

Up to 80 GTH transceivers

- 13.1 Gbps (in -3 speed grade)
- 40 for RTM (Rare Transition Module)
- 28 for Full Mesh Fabric
- 12 for Mezzanines

Four FMC Mezzanine Cards

- 35W, up to 60W possible
- LVDS up to 34 Gbps unidirectional
- 3 x GTH up to 30 Gbps bidirectional

DDR3 256MBytes

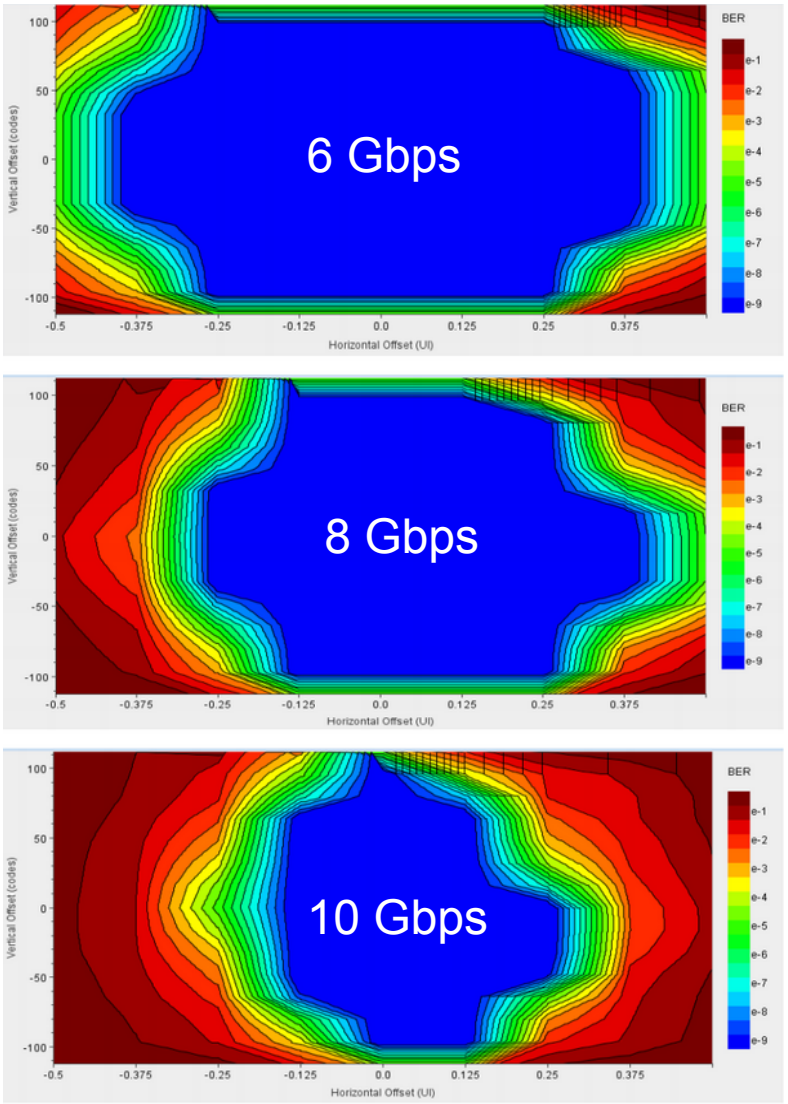
IPMC Mezzanine Card

Backplane clock distribution

This is the original Pulsar 2B board design.
No revisions or “green wire” modifications have been required thus far.

Analyzing Transceiver Performance

- The quality of all 80 GTH transceiver channels tested with the Xilinx IBERT tool (Chipscope ISE or Vivado 2014.4)
- Statistical “eye diagrams” based on Bit Error Ratio measurements determine RX margins
- **Blue = BER < 10^{-9}**
- Several parameters to tune the link:
  - TX_DIFF_SWING
  - TX Pre/Post Emphasis
  - RX termination voltage
  - RX Low Power Mode (LPM)
  - RX Decision Feedback Equalization (DFE)
- Link diagnostics are non-destructive and may be run during normal data taking operations



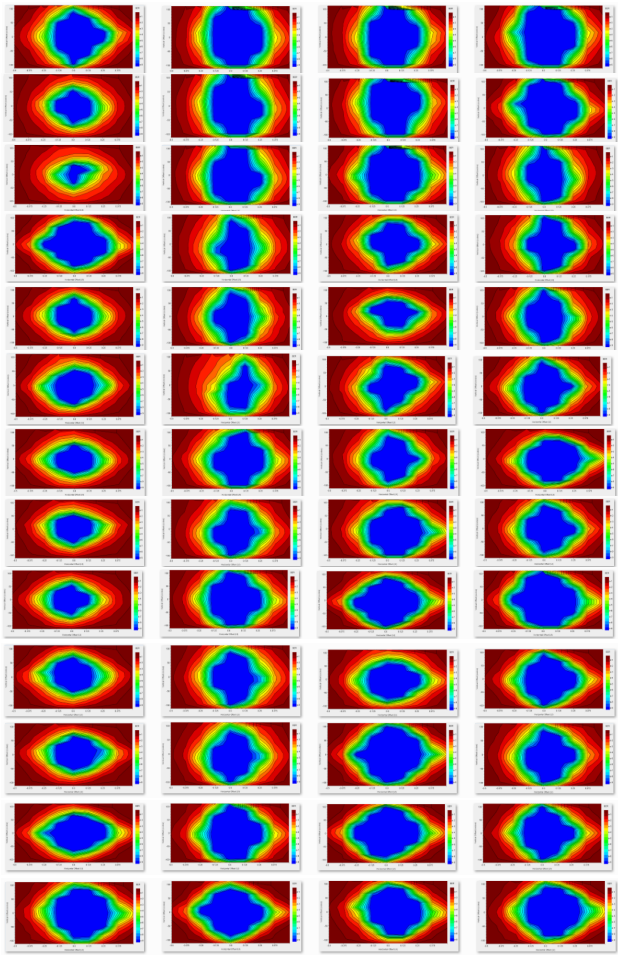
An example of three statistical eye diagrams generated by Xilinx Chipscope. This RTM link looped back at 6, 8, and 10Gbps.

ATCA Shelf Evaluation

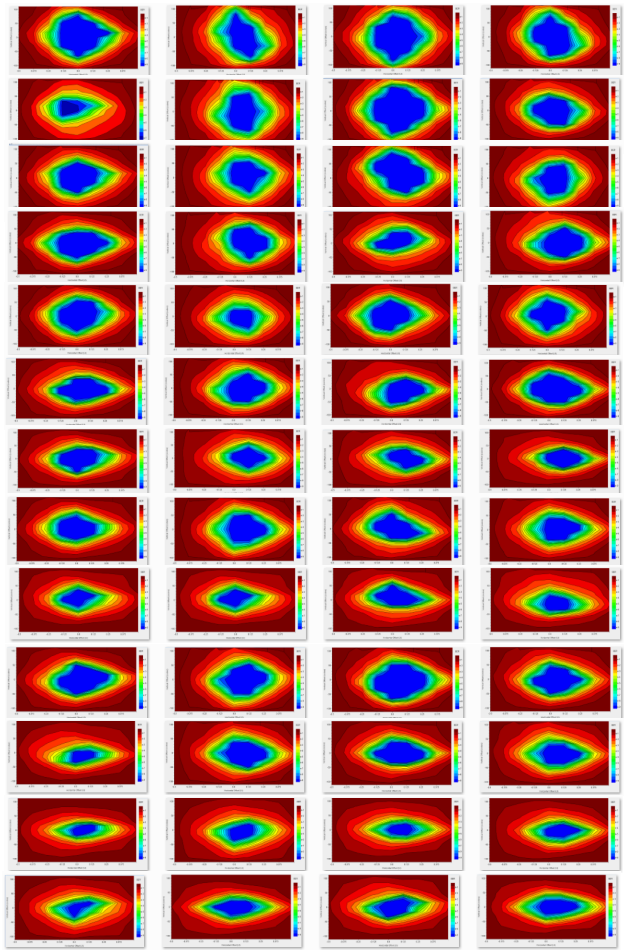
- We have evaluated **full mesh** 14 slot ATCA shelves from:
  - ASIS-PRO
  - Schroff / Pentair
  - COMTEL
  - ELMA
- ATCA Backplane speed rating
  - "10G" = 4 channels @ 2.5Gbps
  - "40G" = 4 channels @ 10Gbps
  - **"100G" = 4 channels @ 25Gbps**
- Shelf cooling capacity
  - Push/Pull fan configuration
  - 350W/slot standard
  - 500W/slot (hurricane!)
- Power Configuration
  - 48VDC input
  - AC/DC redundant power supplies (adds 1U in height)

Early shelf test @ 10Gbps

Shelf A



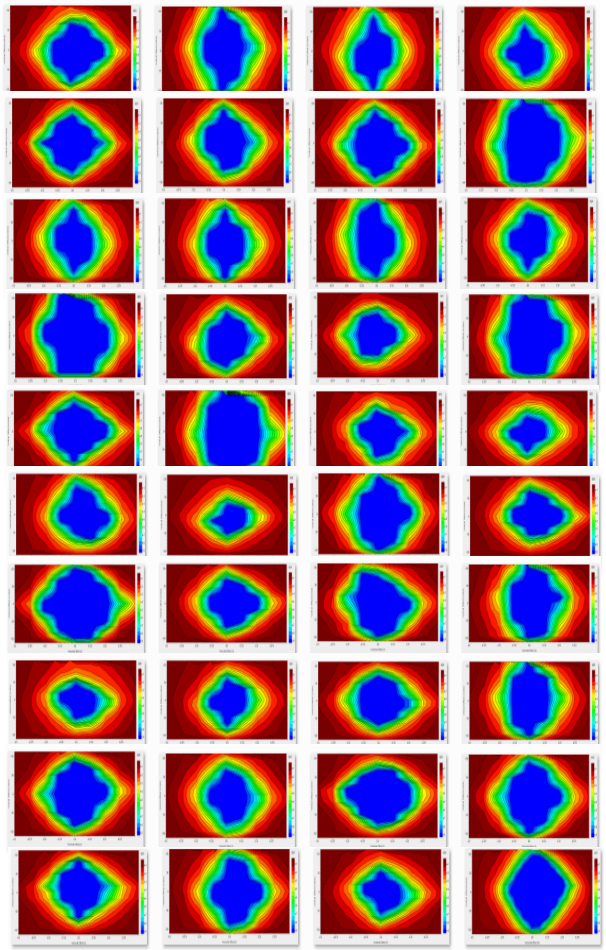
Shelf B



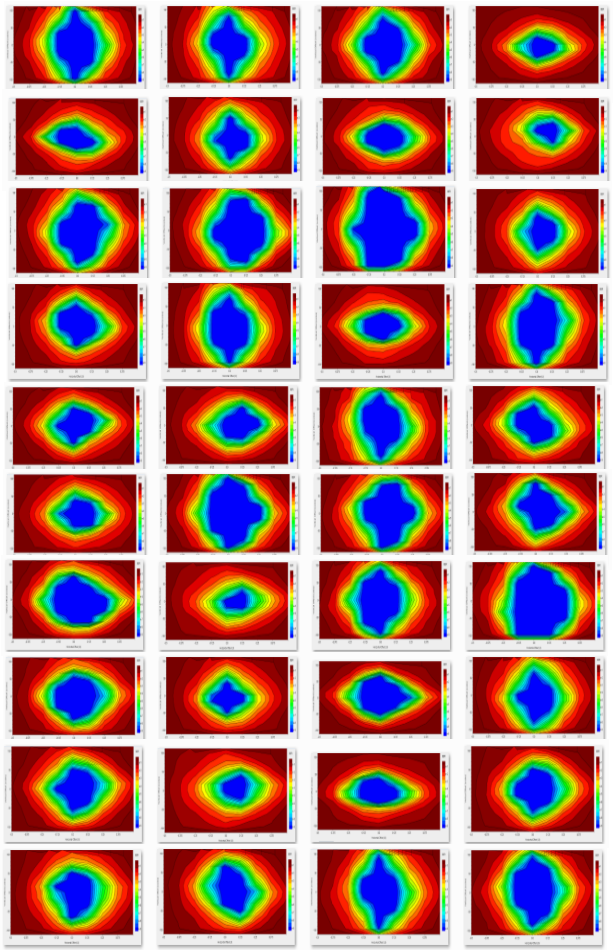
In this test one Pulsar 2B board was installed in slot 1, and another Pulsar 2B board was cycled through the other 13 backplane slots.

Multiple Board Backplane Testing

Shelf A



Shelf C



Five Pulsar 2B boards are installed and tested simultaneously with links running at 10Gbps. A is better than C, but we still see large variations in the eye size in both cases. Tuning is required to get these boards to run error free for several days.

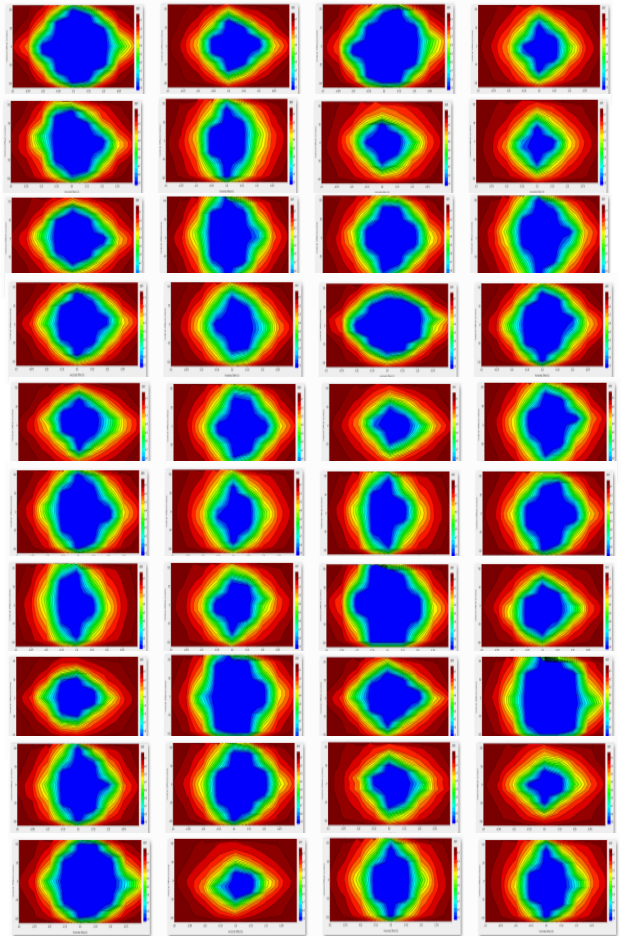
New COMTEL Backplane

- We have been taking part in technical discussions with COMTEL Engineers over the past year regarding the next generation high performance full mesh ATCA backplanes
- As a result we are the first to test their latest backplane design, called Air-/-Plane
- This is one of the very first 100G full mesh backplane designs on the market
  - 1 channel = 4 ports running up to 25Gbps each
  - Split Zone1/Zone2 backplane design for easy upgrades

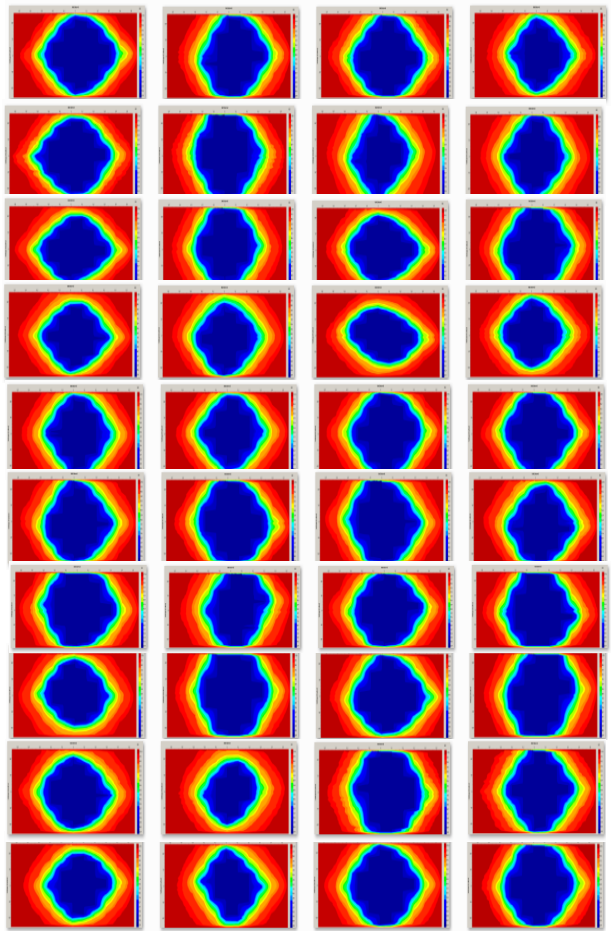
COMTEL ELECTRONICS

New Shelf received December 2014

Shelf A

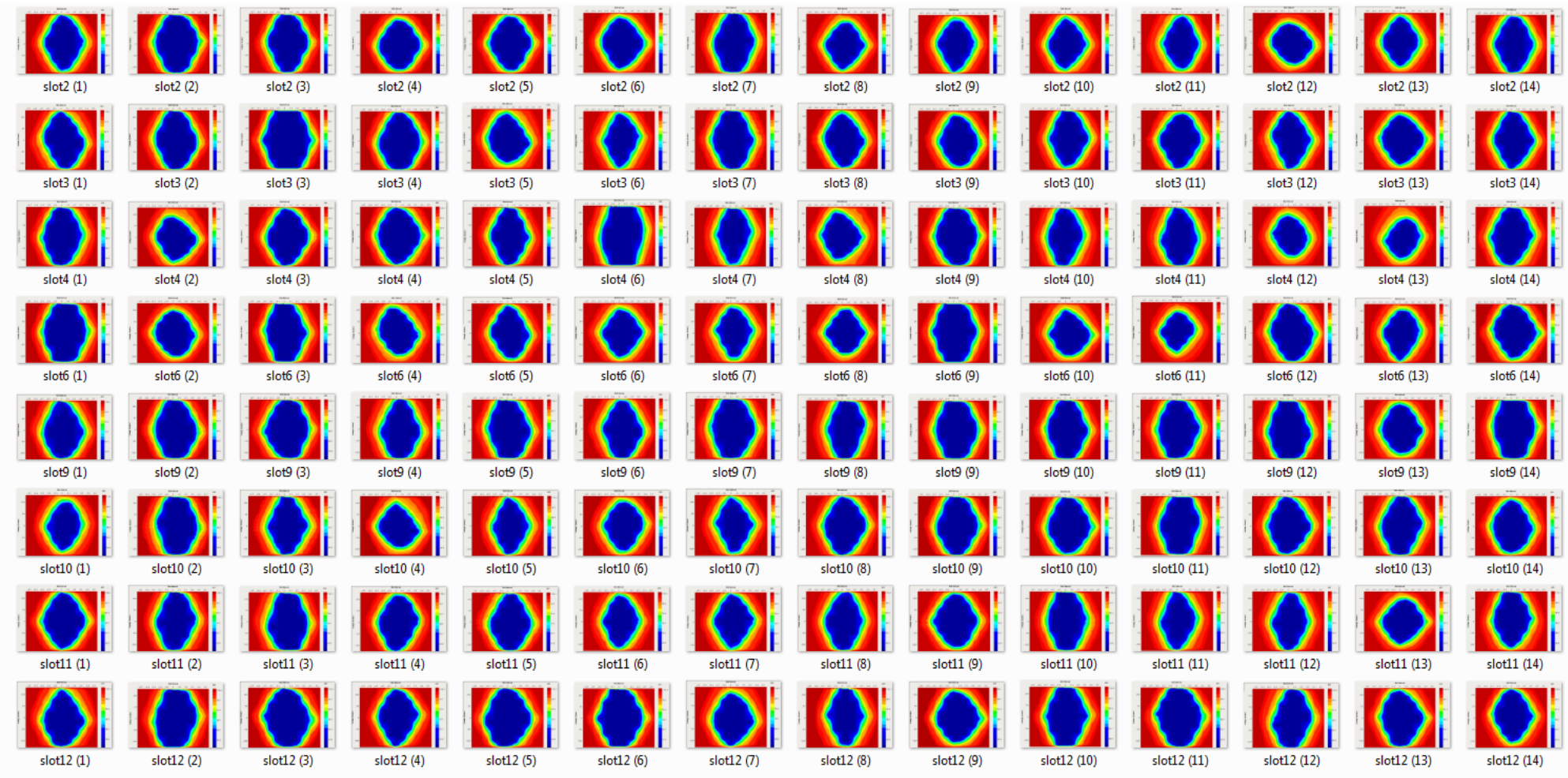


COMTEL Air-/-Plane



Shelf A results are with 7 boards installed, after GTH tuning. The COMTEL results are with 8 boards installed *and no link tuning*. Note the color difference is due to the way Vivado and ISE-Chipscope display the eye. In either case blue = BER of 10^{-9}.

8 Boards Installed in the Air-/-Plane Shelf @ 10Gbps



All 112 links between the eight Pulsar 2B boards are shown here. This test ran for 4 days with **no errors**, achieving a **BER < 3×10^{-16}**. This backplane has the *largest*, and *most consistent* eye diagrams we have ever encountered. And this is without tuning.

Pulsar 2B and backplane testing: conclusion

- Prior to the Air-/-Plane backplane we were testing a combination of the Pulsar 2B characteristics and backplane characteristics.
  - Difficult to determine which parts were effecting backplane link performance
- With the Air-/-Plane backplane we are now getting a clearer picture of the Pulsar 2B board performance
- Pulsar 2B fabric links are fairly consistent at 10Gbps
- Marginal links were caused by backplane, not the Pulsar 2B
- Ongoing discussions with COMTEL Engineers on how to interpret these results and to improve future designs.

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IPMC Mezzanine

- Intelligent Platform Management Controller
  - Required for ATCA boards
- Simplified IPMC module developed at Fermilab for Pulsar 2B testing
  - 244 pin mini-DIMM
  - Cortex M3 micro @ 120MHz
  - Real Time OS (KEIL RTX)
- IPMI Functions
  - I2C interfaces to shelf manager, sensors, power modules, and RTM
  - Monitors front panel switch, controls board power, RTM hot swap
- User Functions
  - 100BASE-T Ethernet Base Interface
  - TCP/IP Stack + various services
  - JTAG master for FPGA programming

Brazil + FNAL

IPMC and Network Communication

As the IPMC network interface matures we go from this:

Bundle of JTAG cables connected to a nearby laptop on the bench. Single user access in a noisy room!

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to this…

Multi-user access; remote access; 10Gb Ethernet over fiber = shelf is electrically isolated from equipment

Xilinx Virtual Cable (XVC)

XVC is an internet-based protocol that acts like a JTAG cable
– Extensible to allow for safe, secure connections
– Debug and programming via Vivado hardware manager

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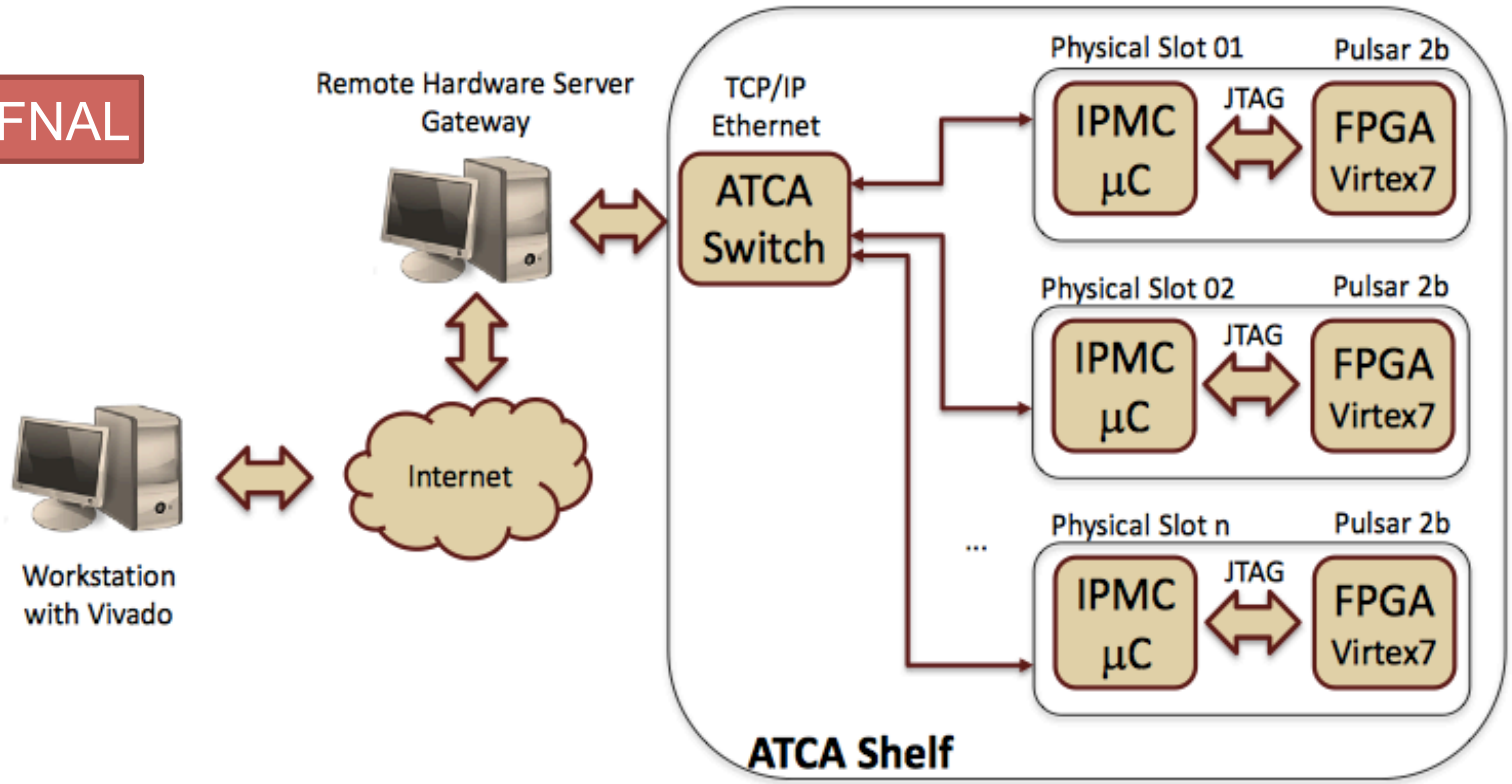

Can be used when the user
– Have an FPGA in an inaccessible location
– Require remote programming and debug of an FPGA
– Do not have direct access to the FPGA pins

XVC Performance

We programmed FPGA of Pulsar 2B from FNAL, CERN and SPRACE
- FPGA image 28MBytes size
- Goal: Performance Check

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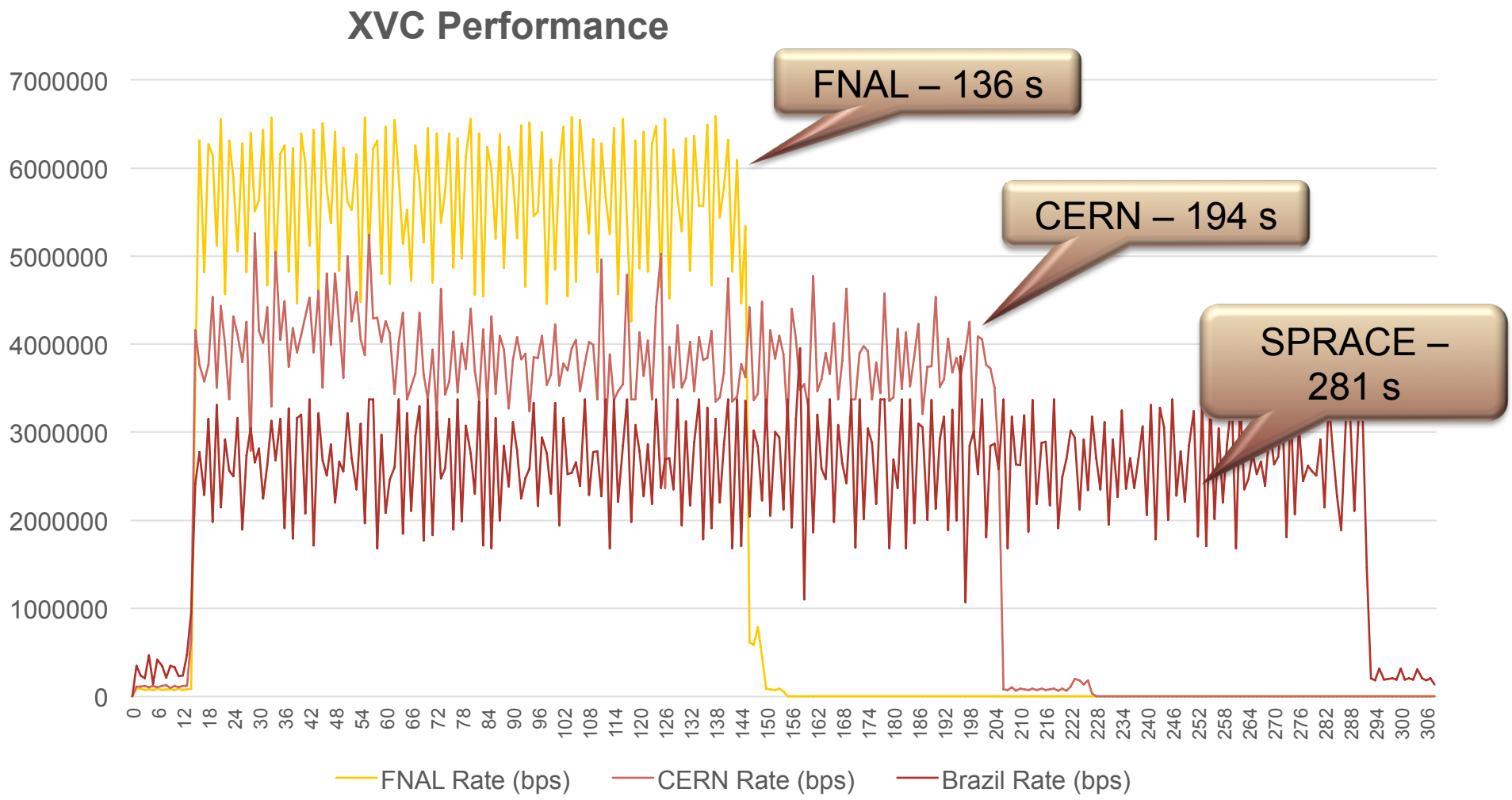

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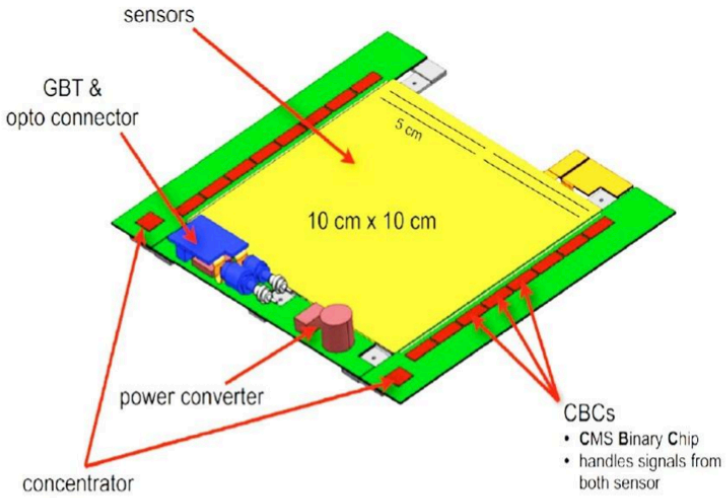
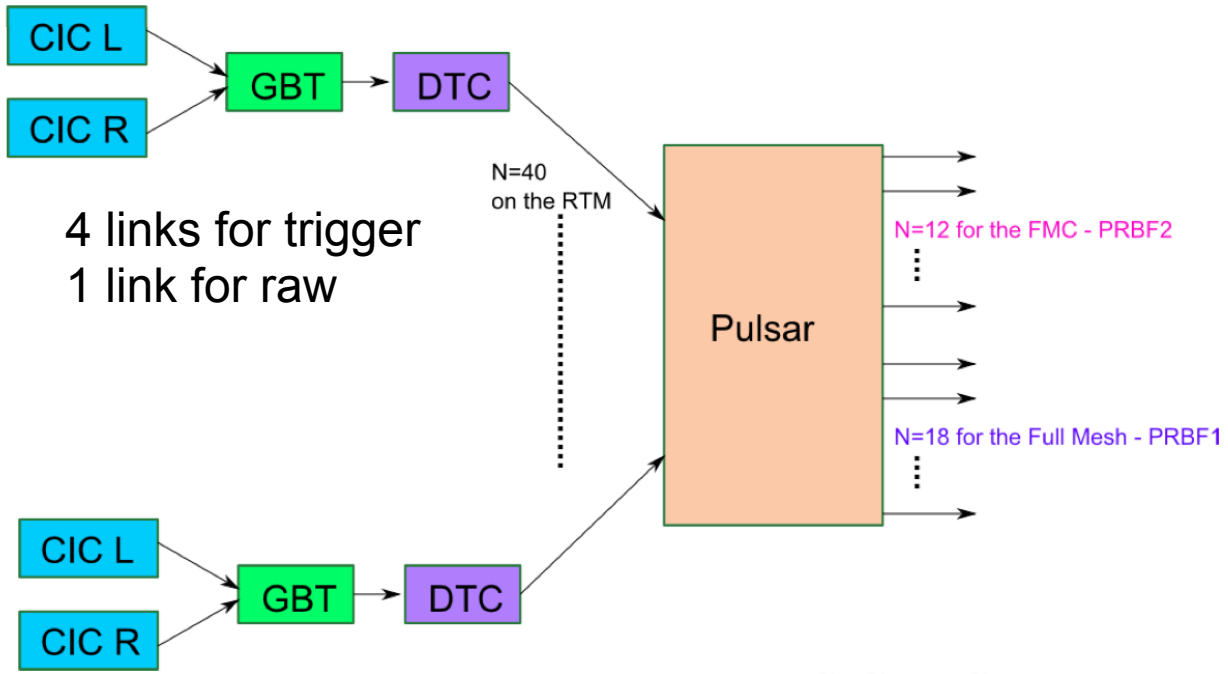
L1 readout performance

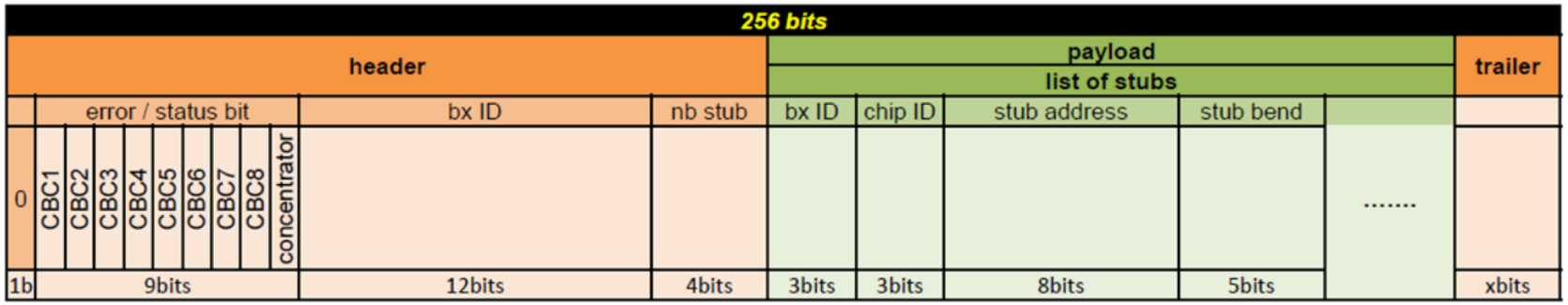
- L1 trigger data rate: 40MHz ~ 25ns
- 8 bunch crossings: 40MHz/8 = 5MHz ~ 200ns
- CIC to GBT readout rate: 320MHz (per link)
  - 320MHz / 5MHz = 64 clock cycles (in 200ns)
- CIC links used for trigger: 4bits(4links) * 64 clk = 256 bits (in 200ns)



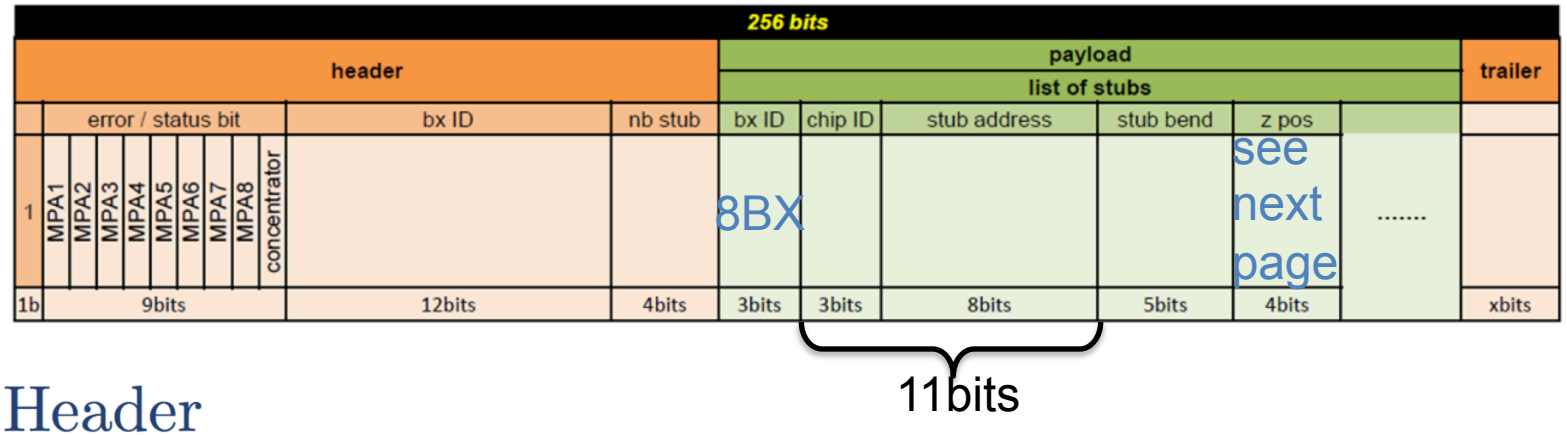


Data format（for LP-GBT）

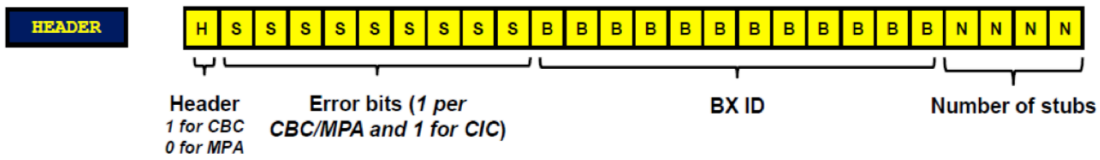
- 2S Module: CBC, 12 stubs x 19 bits + Header and Trailer



- PSModule: MPA, 10 stubs x 23 bits + Header and Trailer



- Header



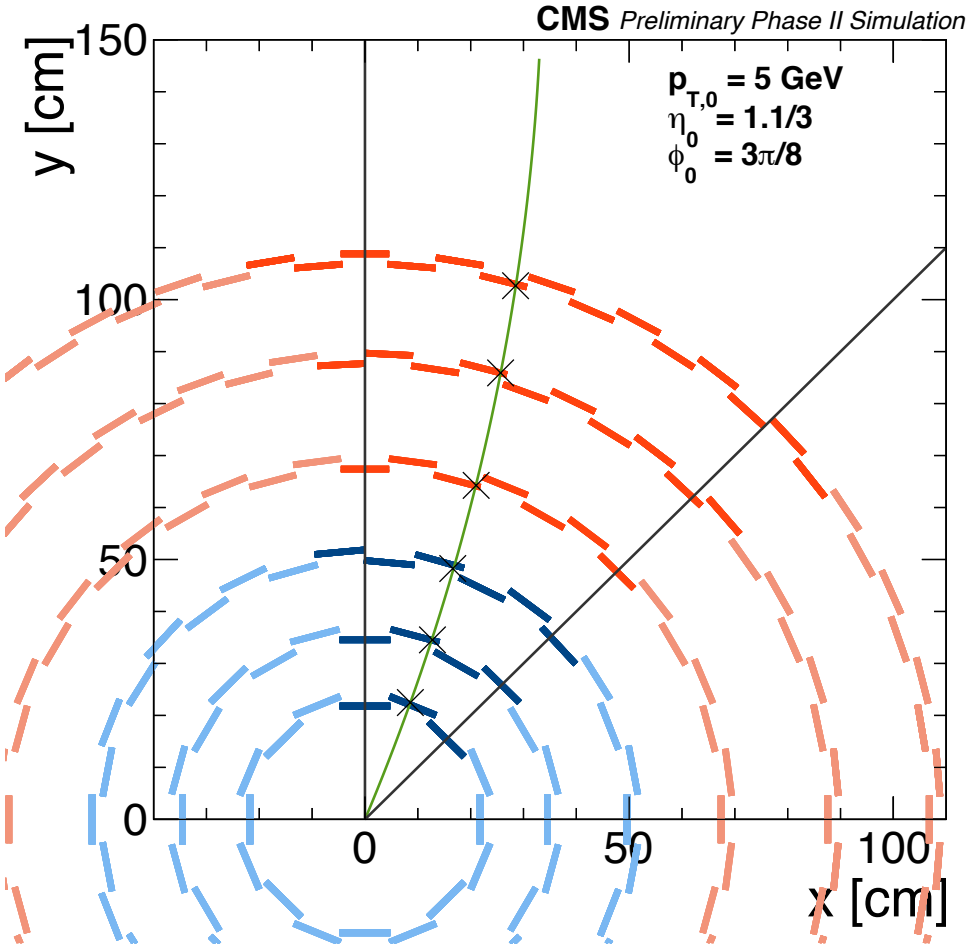
2S Modules: Up to 12*2=24 stubs for a 8BX data train
PS Modules: Up to 10*2=20 stubs for a 8BX data train

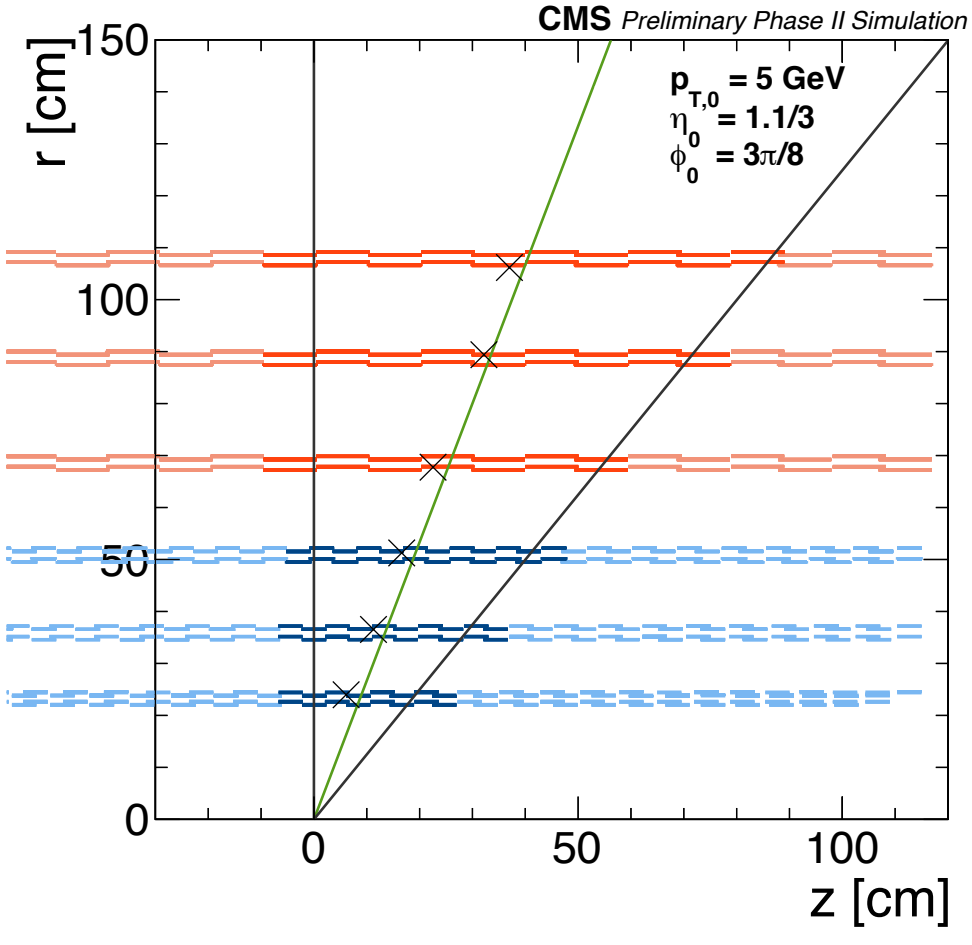
Demonstration data file for 1 board

Preparing Software and Firmware for data sourcing:

- First pass at developing structure for input data to be stored in FPGA
- C++/ROOT based framework interfaced with Python software for Ipbus communication, building upon VIPRAM testing experience

Test with 1 single muon





Data file

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Module_50333 = 0, 0, 0, 1124151322476545, 0, 0, 0, 1
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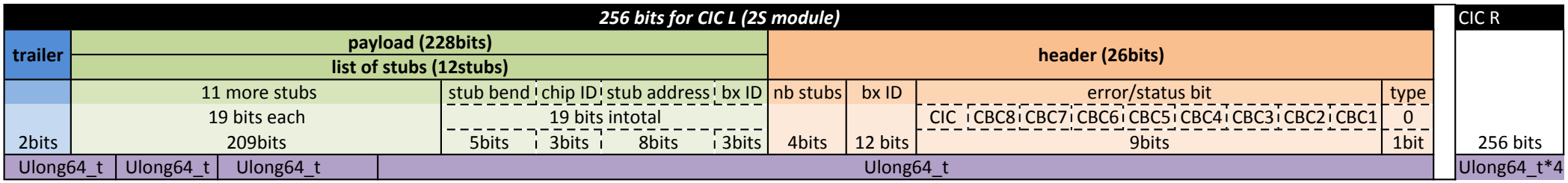
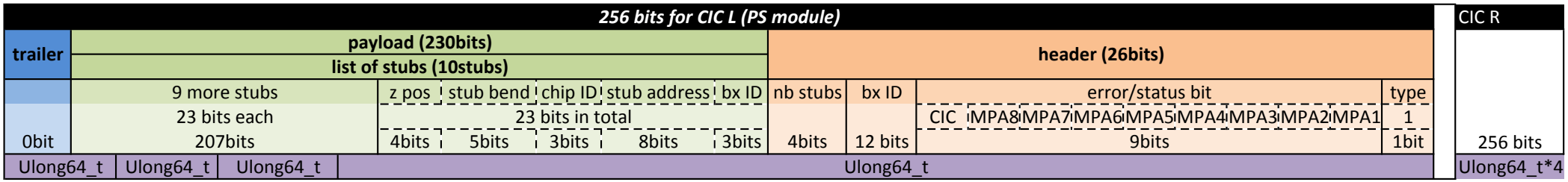
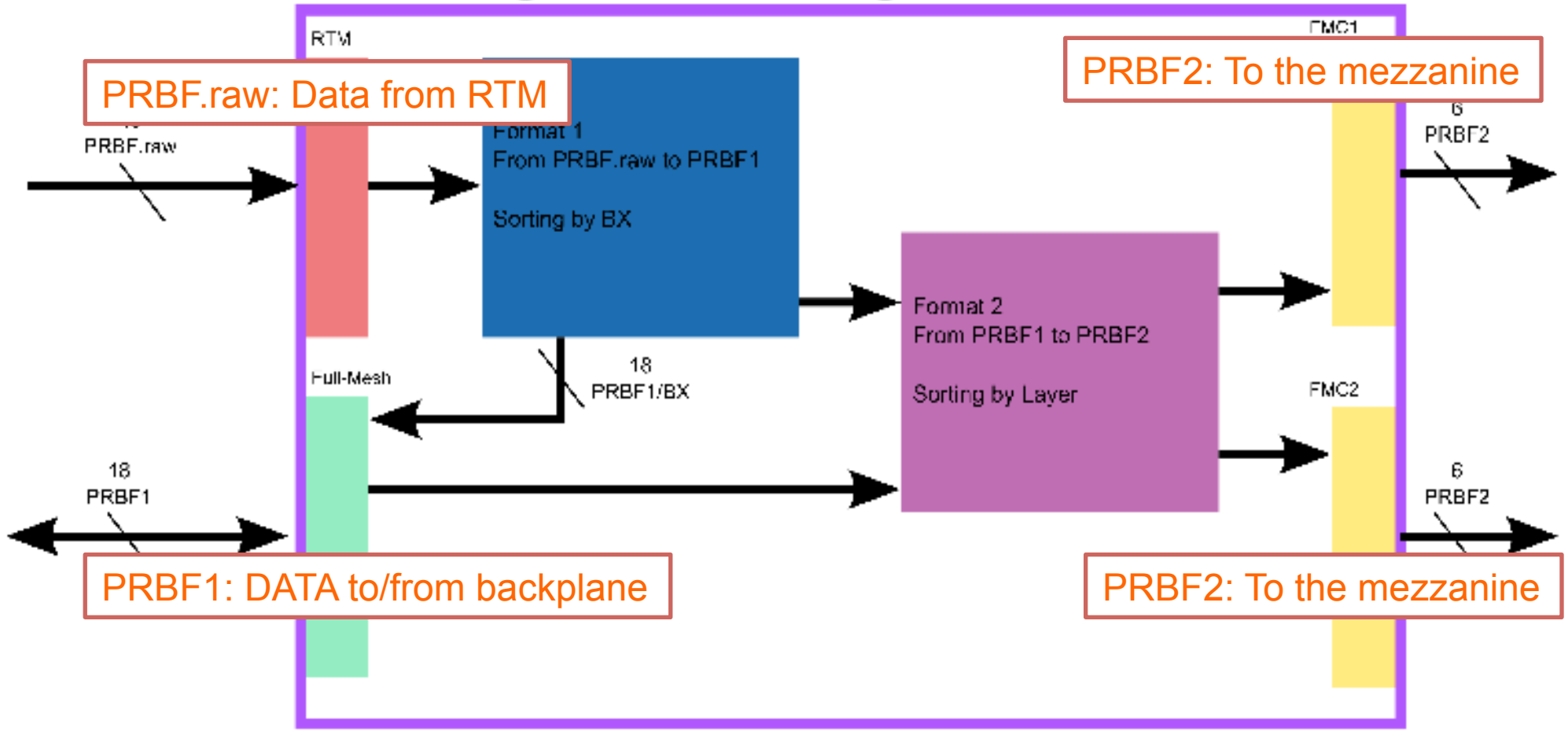




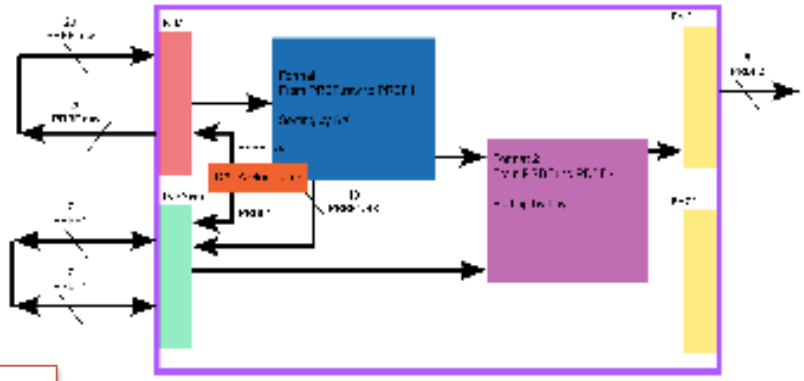
PRB Firmware



Northwestern + CERN

PRB Firmware

- **First test on a single Pulsar:**
  Design will change when **time multiplexing** will be considered.
  - **Data IN:**
    - **20 inputs on the RTM**
    - 8 bits @ 320MHz
    - 12+12 stubs per input (CIC L+ CIC R)
    - 7 IN-OUT on the BackPlane
  - **Data OUT:**
    - 6 output links available on the mezzanine card
    - 32 bits @ 275MHz
    - Line rate=8.8Gbps
    - Aurora64/66b
    - 1 board per BX
    - 1 link per layer per BX on the FMC



CURRENT DESIGN

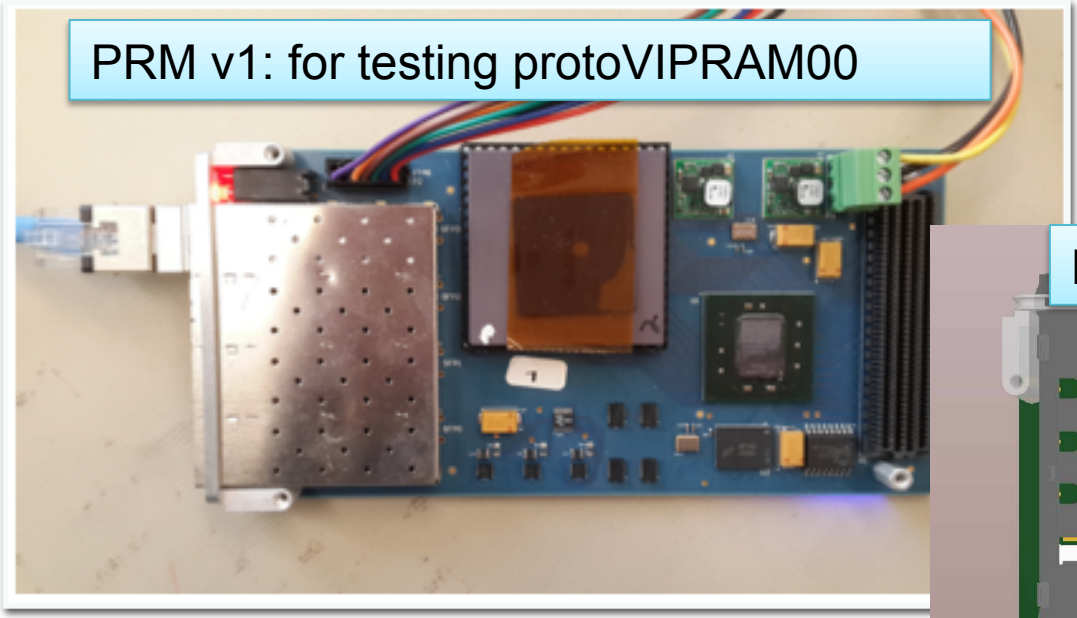
- Latency from PRBF.raw to PRBF1: 800ns
- Latency from PRBF.raw to PRBF2: 1us
  For the final implementation the latency may increase

Northwestern + CERN

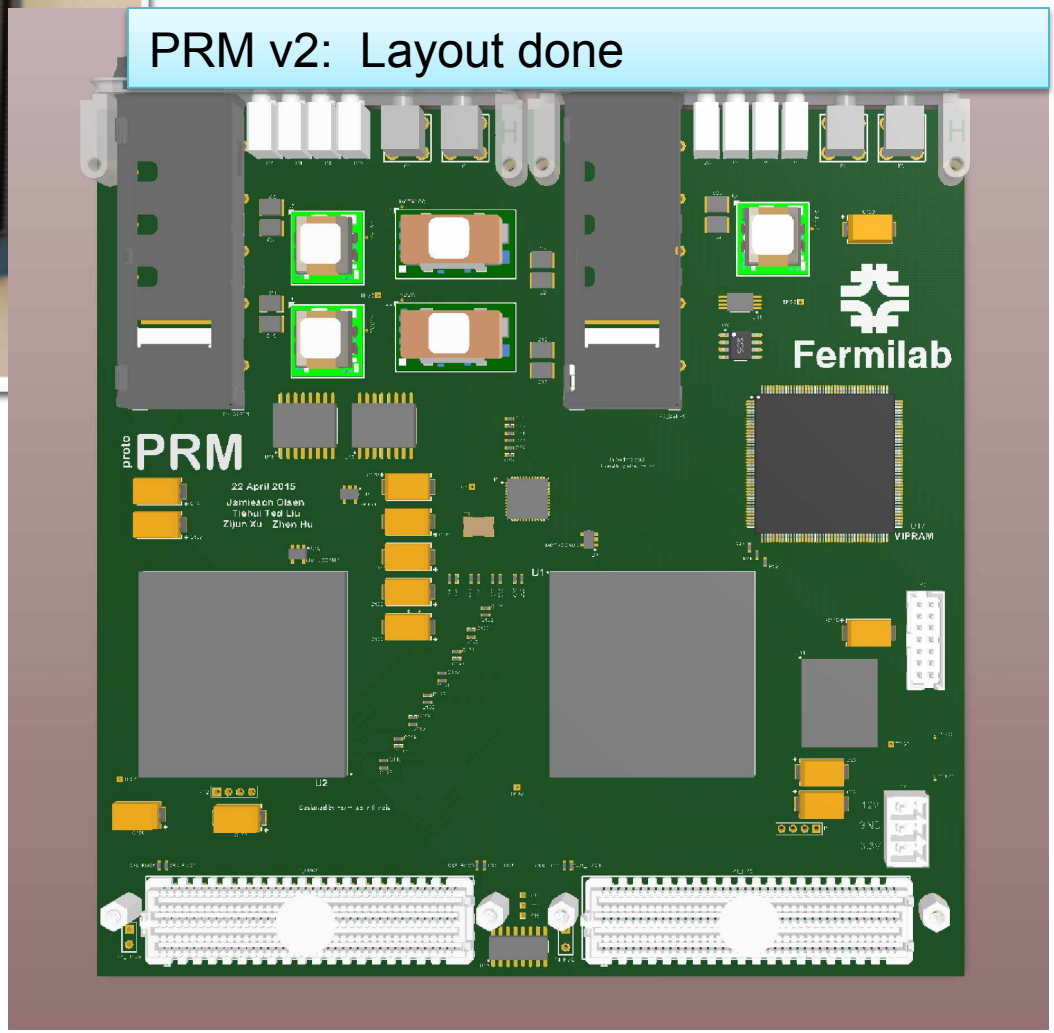
Outline

- Overview of L1 tracking trigger project
- Plans for partial and full-scale demonstration
- Highlight of the recent progress in each of the areas needed for demonstration
  - Pulsar 2B status
  - IPMC/XVC work and remote access
  - Data sourcing and data delivery
  - **Pattern recognition mezzanine card**
- Summary

FNAL Mezzanine Card



Tests with protoVIPRAM00 reported by Nhan on Monday



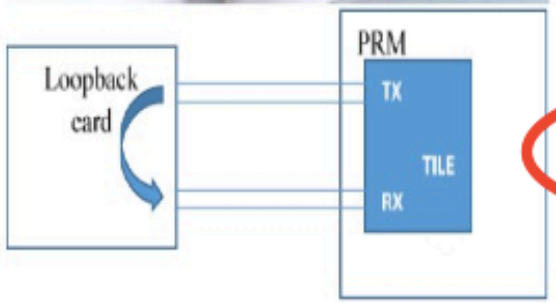
- A more realistic AM platform vs the basic test mezzanine
- New PRM design nearing completion
  - 1 VIPRAMs
  - 2 UltraScale Kintex FPGAs
  - Double FMC
  - High-speed GTH lines to the FMCs

INFN Mezzanine

V1 – to work with AMChip05 (prototype chip, 2k patt)

V2 – for AMChip06 (FTK Chip with 128k patt)

Preliminary tests with 4 AM chips



Setup:

Preliminary test

- Check the FPGA configuration by using JTAG programming header
- Check the system clock distribution and the GTX clock distribution
- Measure the power consumption
- Check the outputs of the power regulators
- High speed interface test by using Xilinx IBERT environment

INFN

Outline

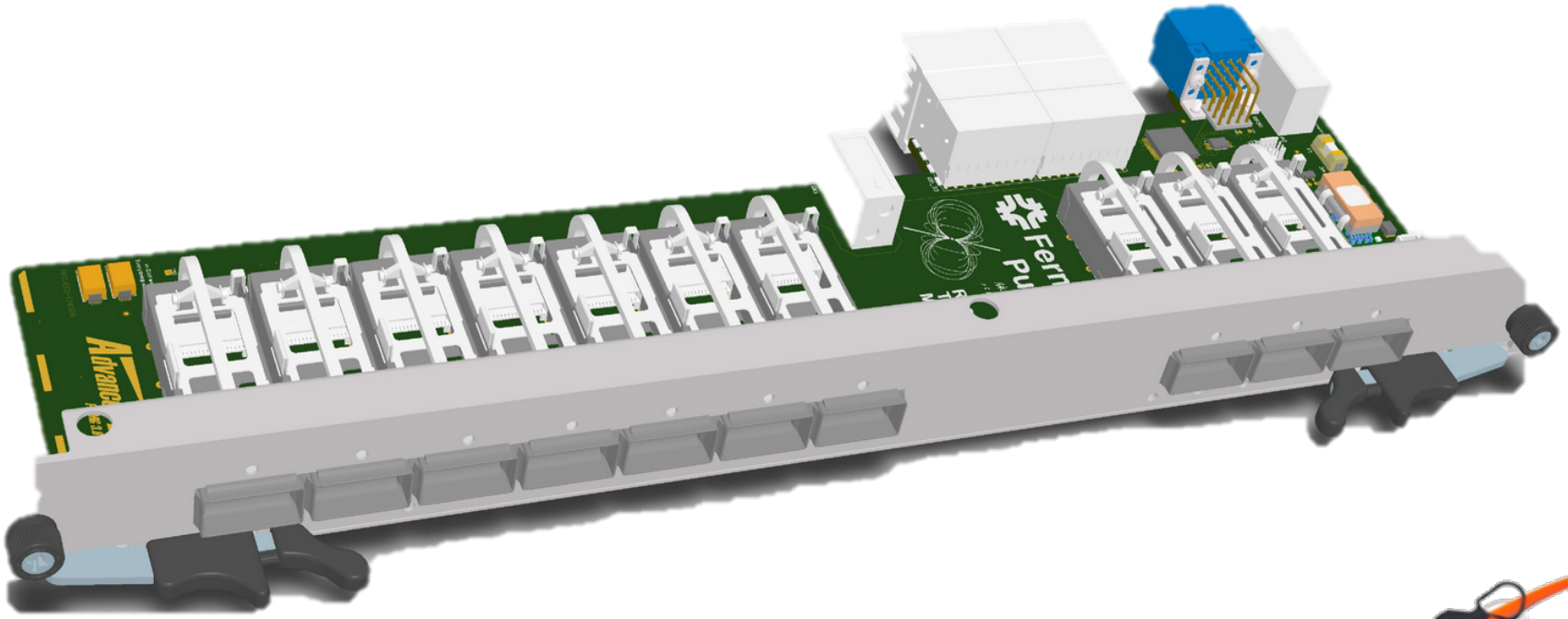
- Overview of L1 tracking trigger project
- Plans for partial and full-scale demonstration
- Highlight of the recent progress in each of the areas needed for demonstration
  - Pulsar 2B status
  - IPMC/XVC work and remote access
  - Data sourcing and data delivery
  - Pattern recognition mezzanine card
- **Summary**

Summary

- We are following staged strategy for demonstrating the AM+FPGA approach
  - at board (2015) and crate (2016) levels
- Steady progress in all areas of the demo implementation
  - expect more detailed presentations during CMS Tracker Week in May
- Broad effort with many engaged institutions
  - on track with the plan towards a demonstrator

Backup

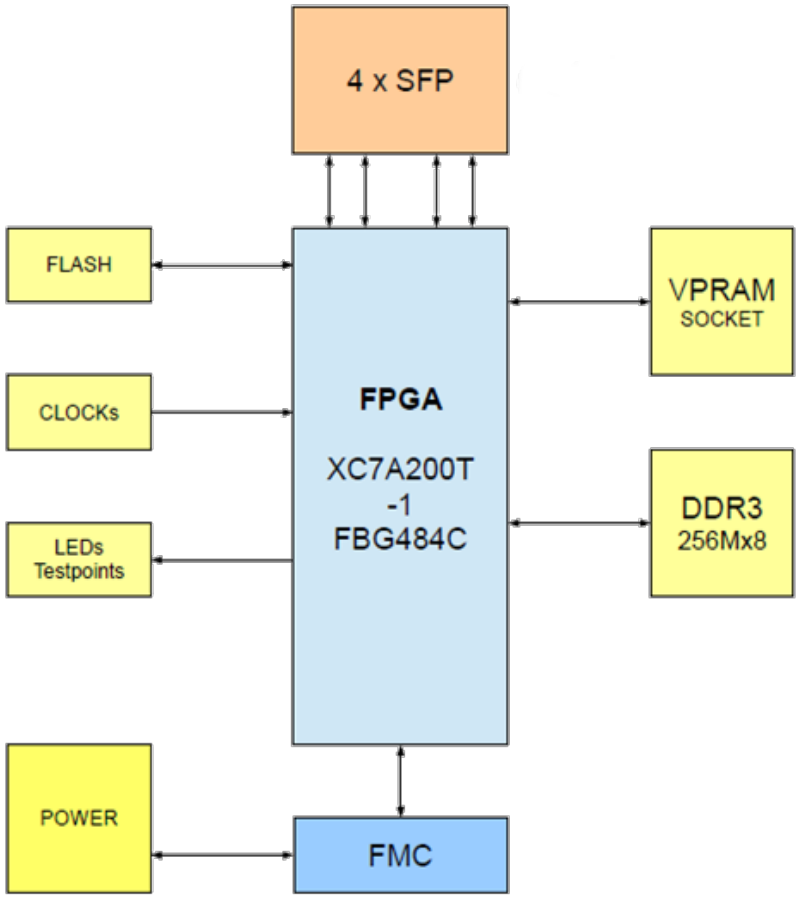
Rear Transition Module (RTM)



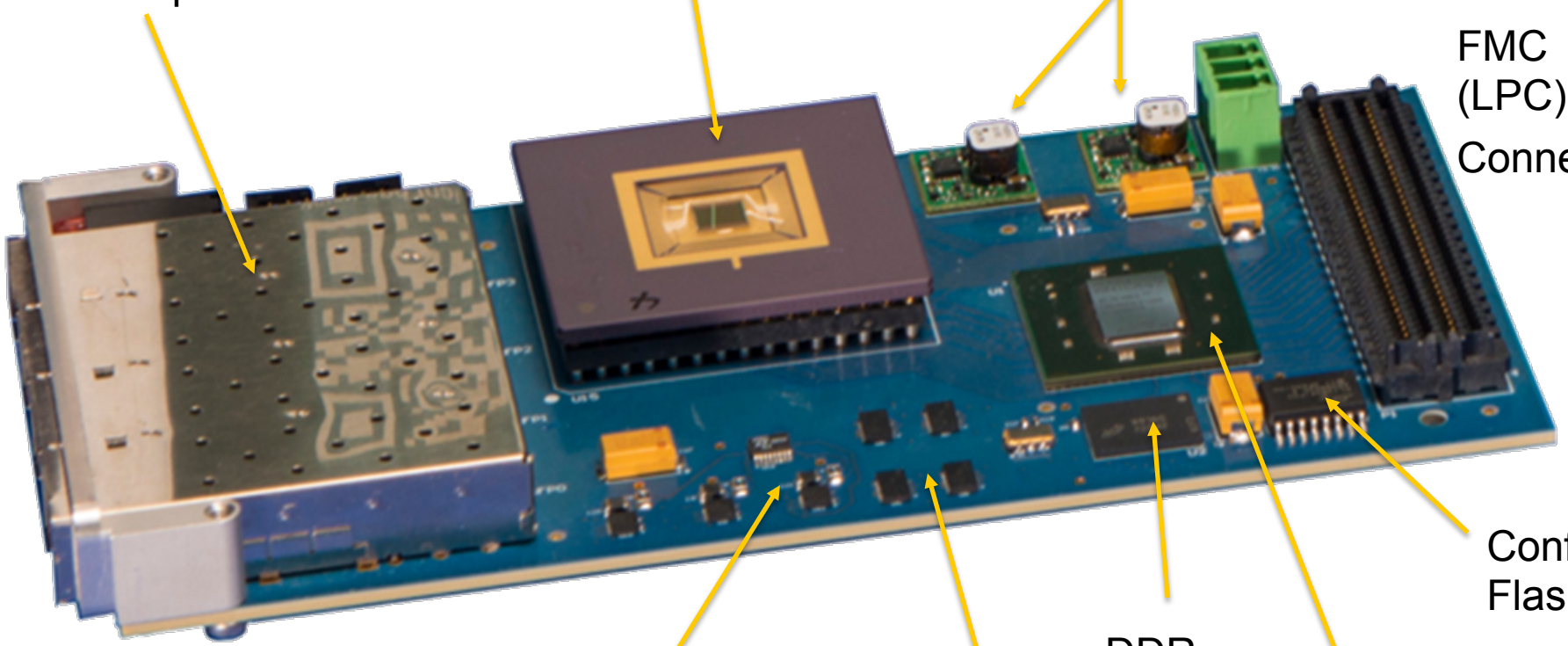
- Supports up to 10 QSFP+ transceivers (400 Gbps)
- Layout v2.0 completed in July 2014
  - Improved diff pair routing and improved power dist.
  - PICMG 3.8 compliant, “intelligent FRU”, hot swap
- Tested using 3M multi-mode QSFP+ Active Optical Cables
  - Single RTM loopback
  - RTM to RTM link tests

Test Mezzanine Card

- Designed in 2013
- Motivation:
  - Test the FMC connector interface with the Pulsar 2B board
  - Standalone test board for our first protoVIPRAM ASIC
- DDR and serial I/O LVDS communication successfully tested with Pulsar 2B boards

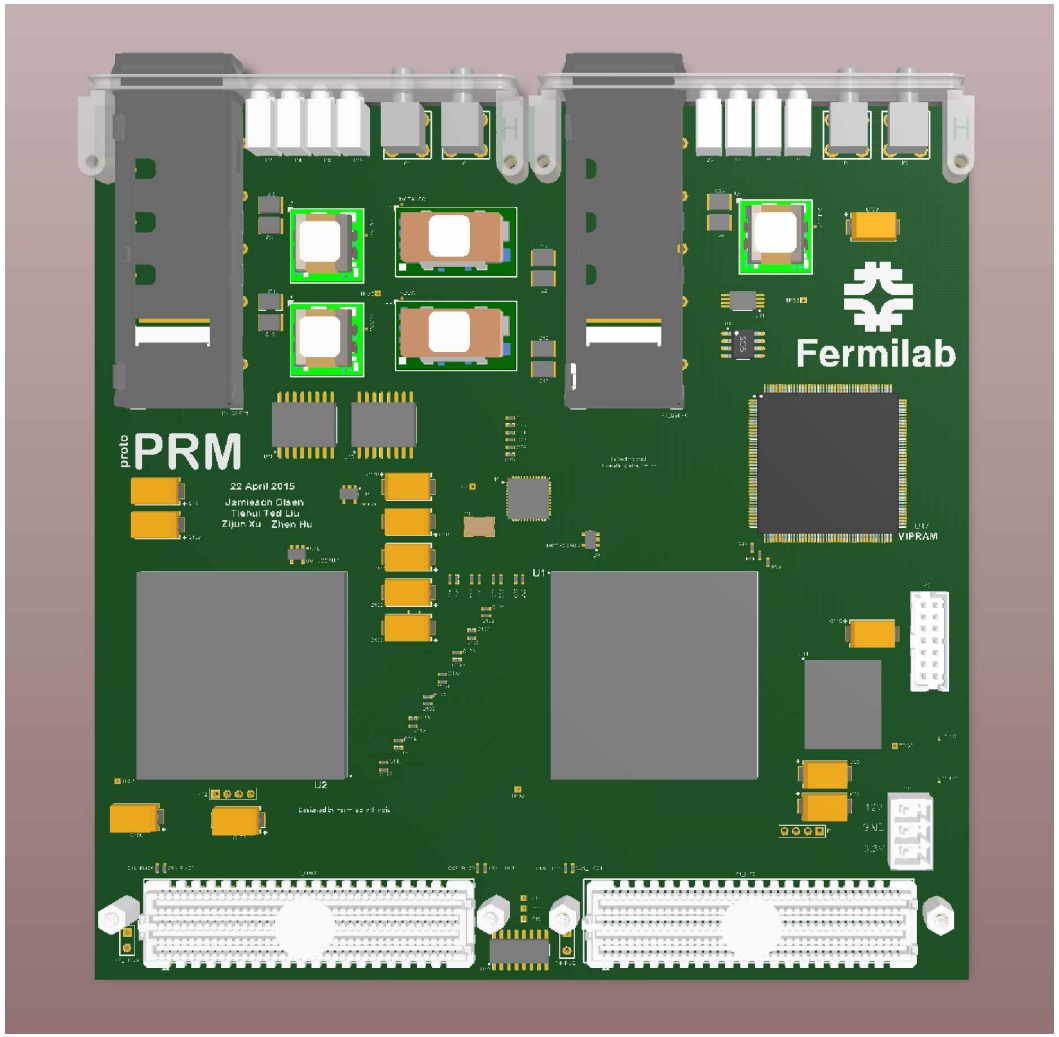


Test Mezzanine Card

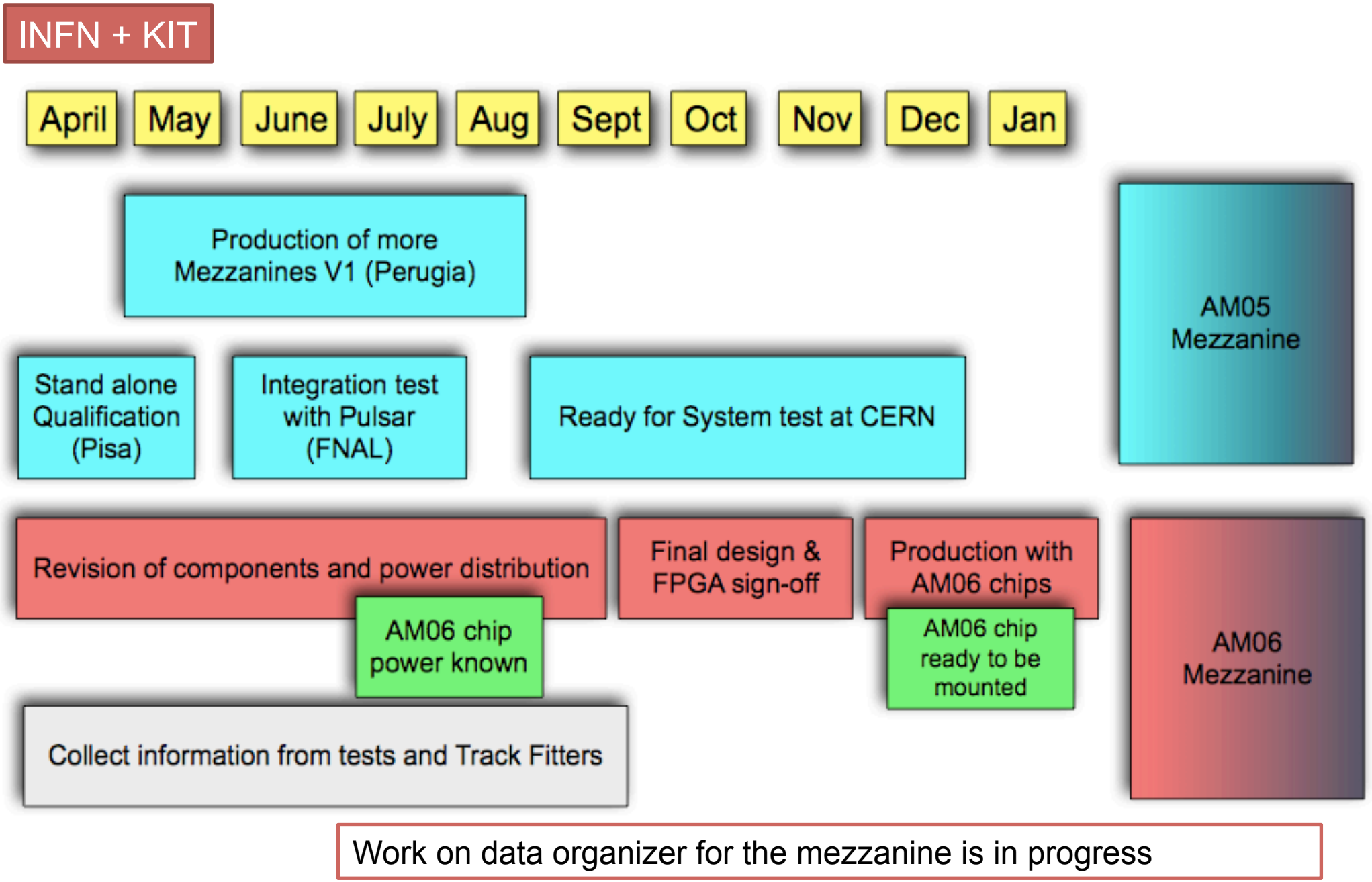


New Mezzanine Card: Motivation

- R&D on an AM based track finder engine
- A flexible test fixture for the next VIPRAM chip
- Compare VIPRAM against FPGA-based VIPRAM implementation
- Gain experience with next generation Xilinx UltraScale FPGAs
- Test high speed GTH links to the Pulsar 2B FPGA

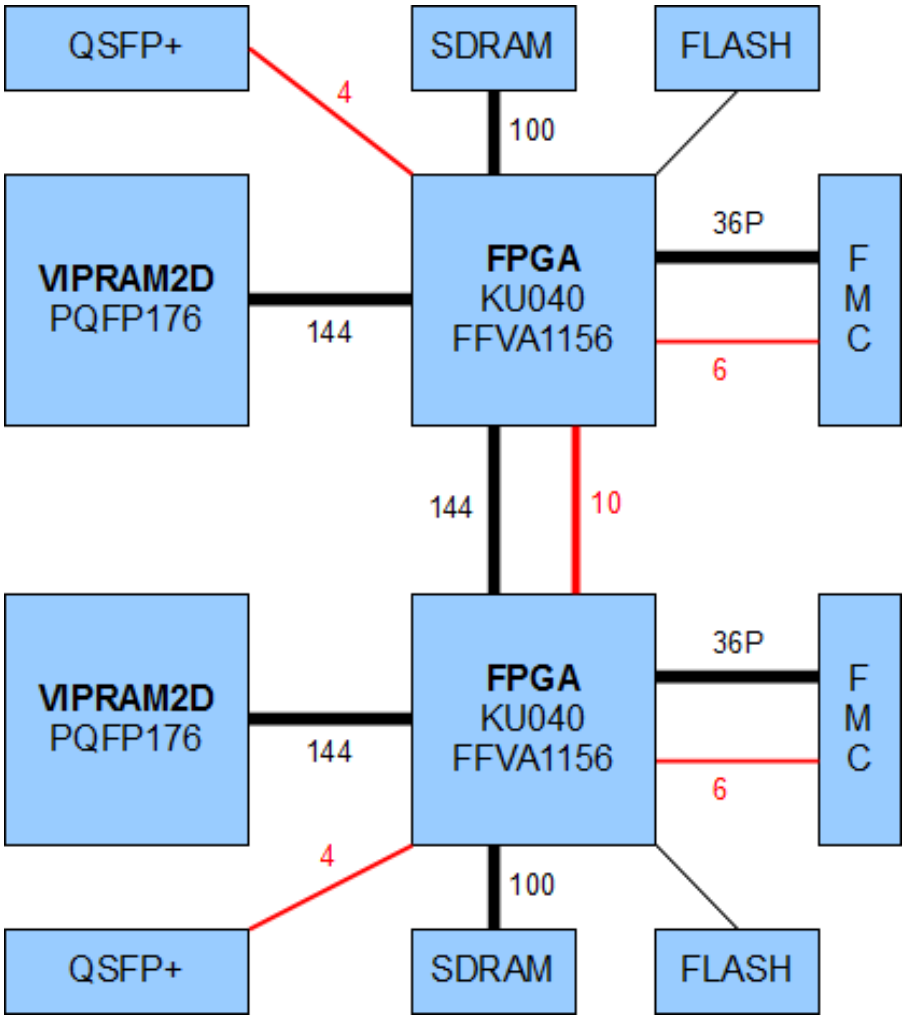


AMChip06 Mezzanine



Work on data organizer for the mezzanine is in progress

New Mezzanine Card: Design

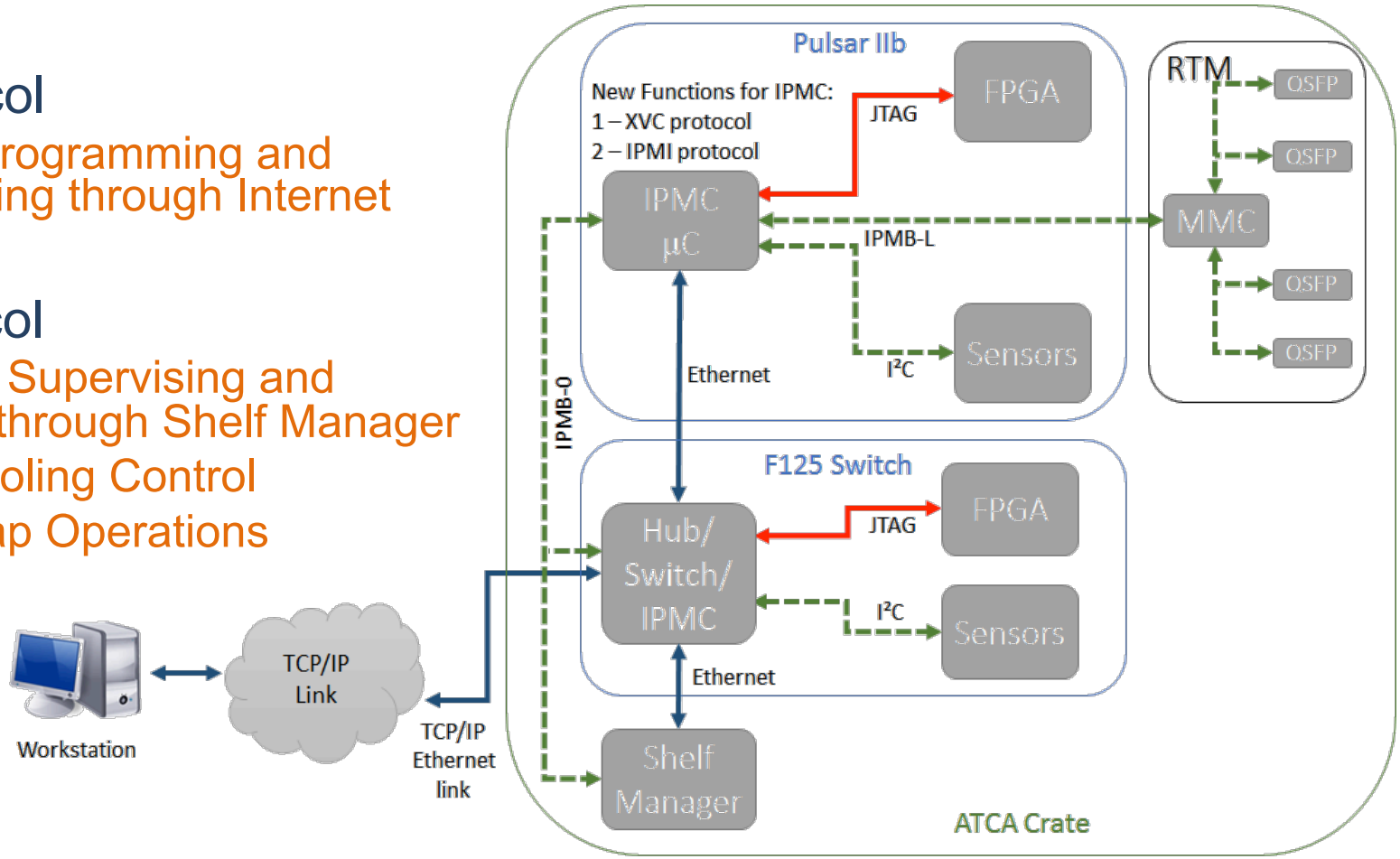


- 2 Kintex UltraScale XC7KU040 FPGAs
  - Dual independent track finder engines, or
  - One FPGA used to model VIPRAM
- Two VIPRAMs
  - Parallel DDR interface
- FMC High Pin Count connectors
  - 12 GTH @ 16Gbps
  - 68 LVDS @ 1Gbps
- Dual QSFP+ transceivers
- Schematics done
- In layout now!

IPMC IPMI Capabilities

Implemented new Functions for Pulsar 2B IPMC:

1. XVC protocol
   - FPGA Programming and Debugging through Internet
2. IPMI protocol
   - Remote Supervising and Control through Shelf Manager
   - Auto Cooling Control
   - Hot Swap Operations

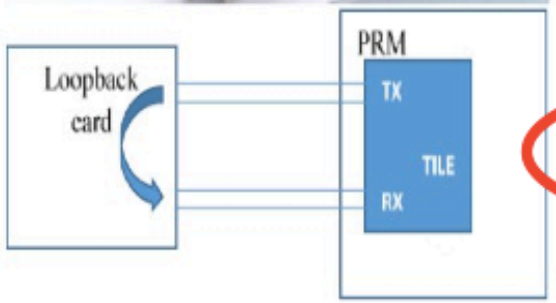


AMChipXX Mezzanine

V1 – to work with AMChip05 (prototype chip, 2k patt)

V2 – for AMChip06 (FTK Chip with 128k patt)

Preliminary tests with 4 AM chips



Setup:

Preliminary test

- Check the FPGA configuration by using JTAG programming header
- Check the system clock distribution and the GTX clock distribution
- Measure the power consumption
- Check the outputs of the power regulators
- High speed interface test by using Xilinx IBERT environment

INFN

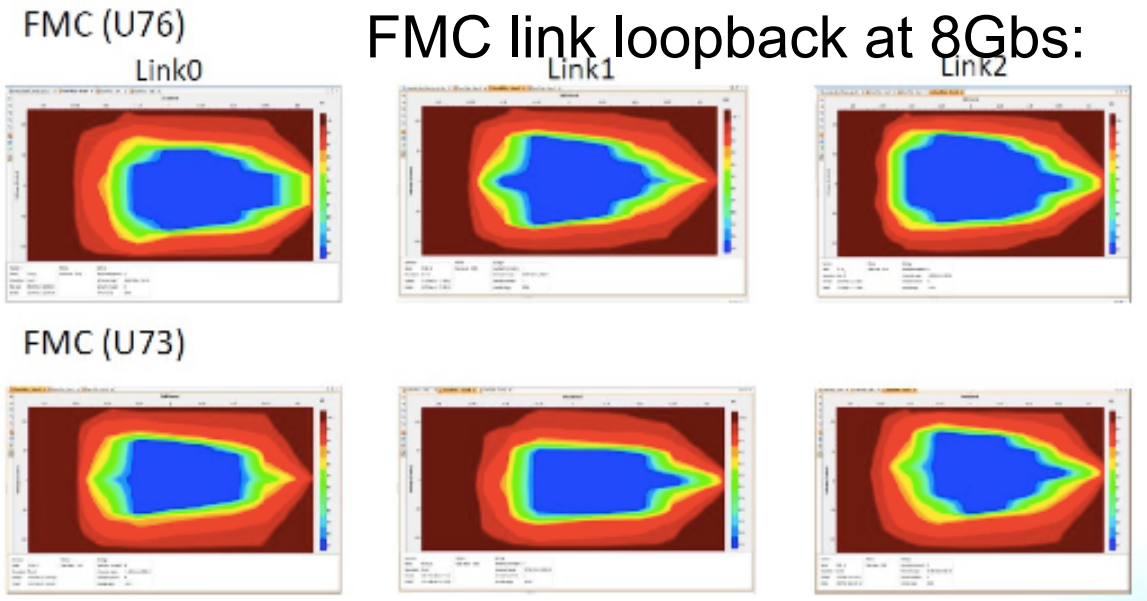
AMChip05 Mezzanine

Power Consumption:

Input voltage		Voltages	# 16 AM05	Fanout	FPGA	TOTAL
Voltage	Watt					
0.425 A @ 12 V	**5.1 W**	1 V	0.82 W	-	4.3 W	5.1 W
9.7 A @ 3.3 V	**32,1 W**	1,2 V	2.56 W	-	9.4 W	20.9 W
		2,5 V	8.9 W	-		
		3,3 V	-	11.2 W		11.2 W

Expected values

FMC link loopback at 8Gbs:



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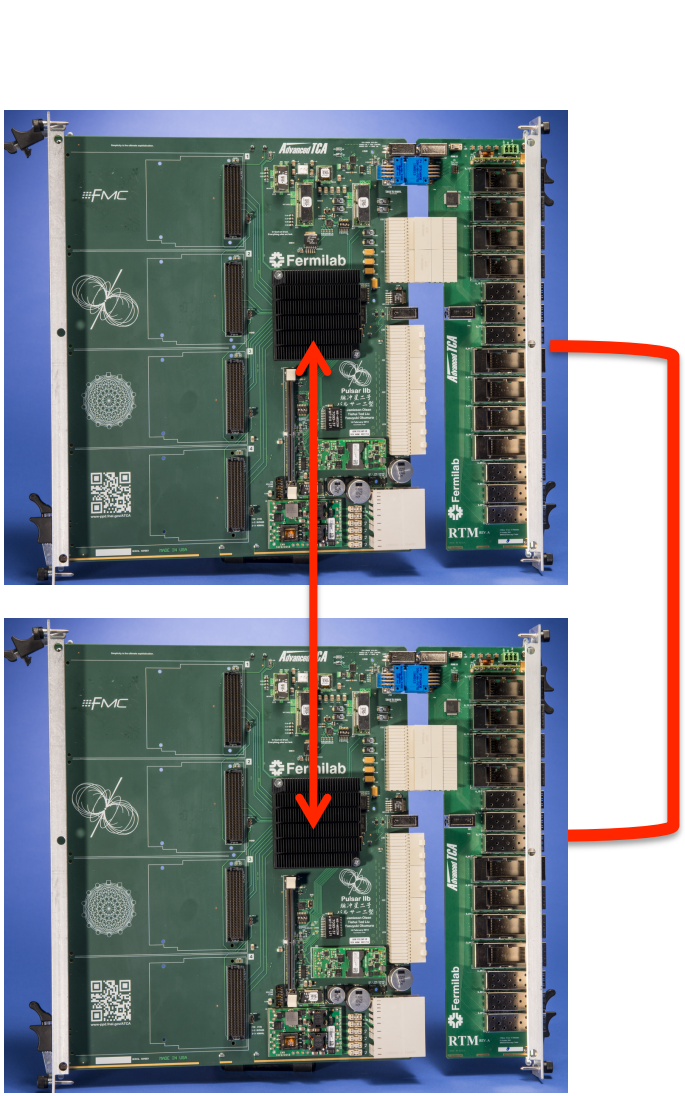
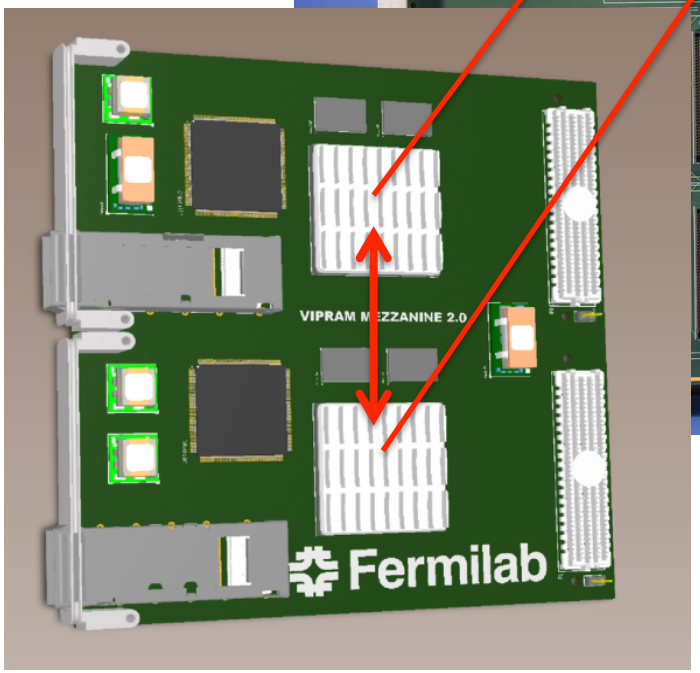
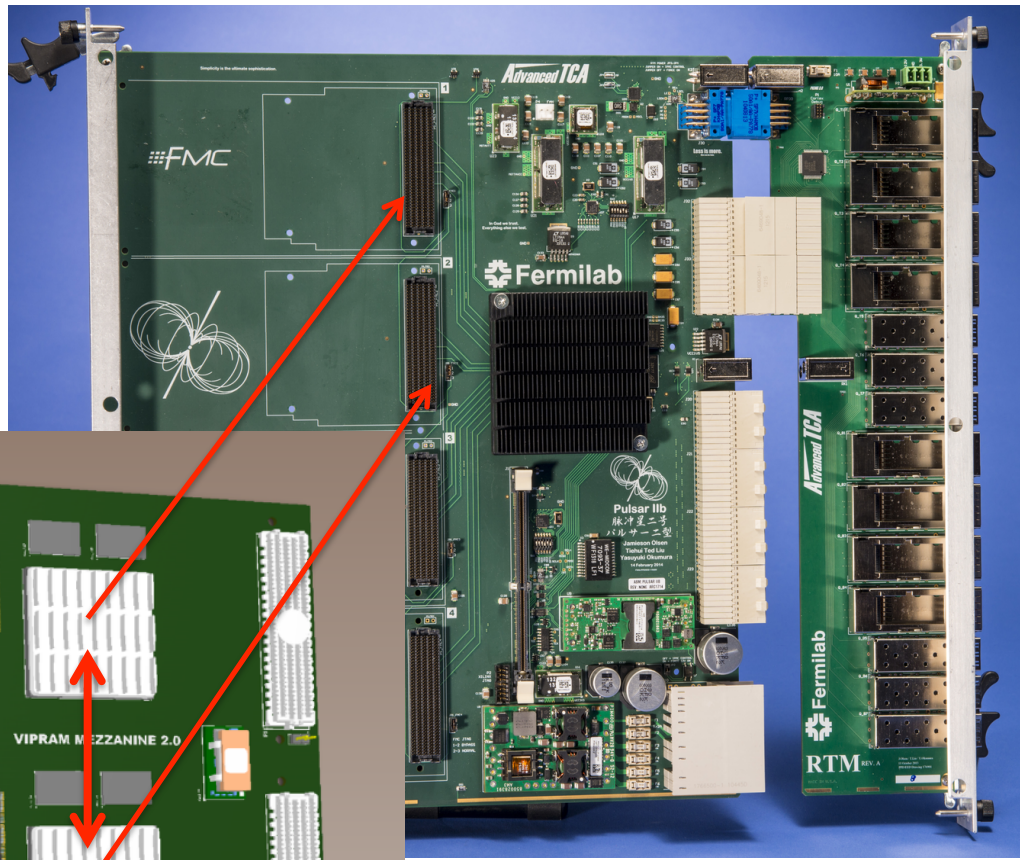
AM in FPGA

- *Many aspects of the system WILL be tested before AM chip arrival*
- *AM functionality now implemented in FPGA (few thousand pattern)*
- Will be first tested using two Pulsar 2B boards, then with new mezzanine

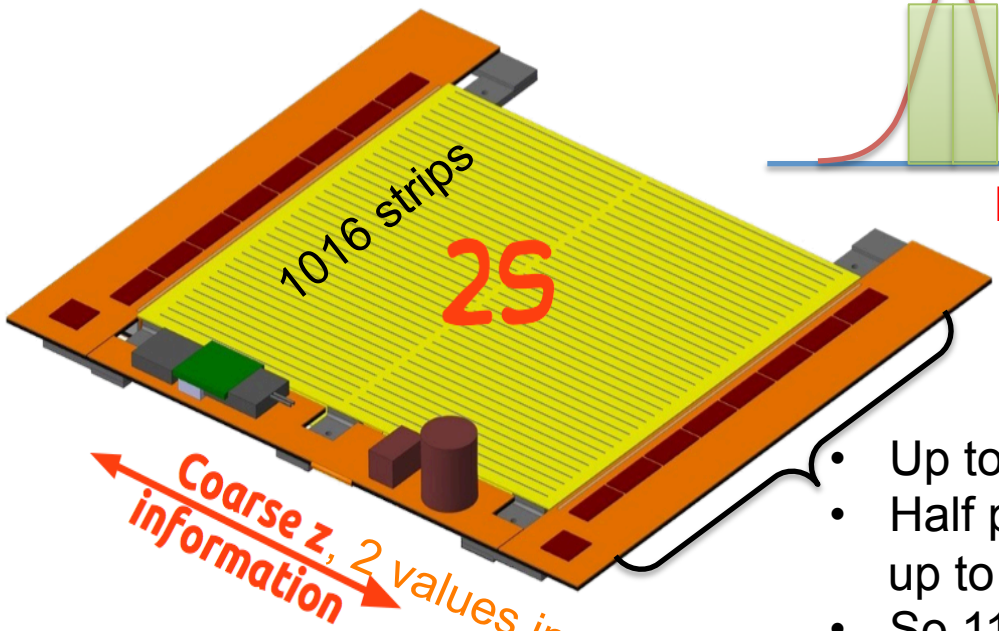


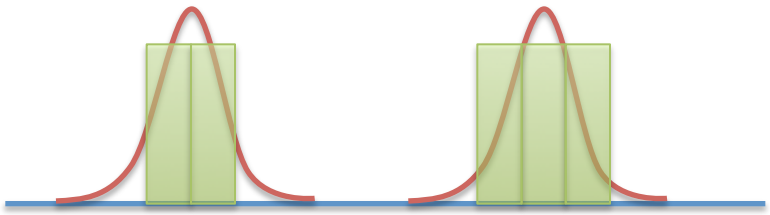




Module design

2 Strip sensors
Strips: 5 cm × 90 μm
Strips: 5 cm × 90 μm
P = 2.7 W
~ 92 cm² active area
For r > 40 cm





- Up to 2^{10} strips
- Half precision measurement: up to 2^{11} values
- So 11 bits needed for the stub address

Pixel + Strip sensors
Strips: 2.5 cm × 100 μm
MacroPixels: 1.5 mm × 100 μm
P = 5.0 W
~ 44 cm² active area
For r > 20 cm

- 2^3=8 chips
- So the first 3 bits of the stub address corresponds to the chip ID

New data format (for LP-SEC)

LP-SEC

320 bits

header											payload: list of stubs					trailer
	error / status bit									bx ID	nb stub	bx ID	chip ID	stub address	stub bend	
0	CBC1	CBC2	CBC3	CBC4	CBC5	CBC6	CBC7	CBC8	concentrator					18 bits per stub....		
1b	9bits									12bits	4bits	3bits	3bits	8bits	4bits	Bits at '0'

- 4 bits are are sufficient for the bend for 2S module
- N_{stub} per CIC: 12 stubs -> 15 stubs

LP-SEC

320 bits

header											payload: list of stubs						trailer
	error / status bit									bx ID	nb stub	bx ID	chip ID	stub address	stub bend	z pos	
1	MPA1	MPA2	MPA3	MPA4	MPA5	MPA6	MPA7	MPA8	concentrator						21 bits	per stub	
1b	9bits									12bits	4bits	3bits	3bits	8bits	3bits	4bits	Bits at '0'

- 3 bits are are sufficient for the bend for PS module
- N_{stub} per CIC: 10 stubs -> 14 stubs

Reference: S.Viret: https://indico.cern.ch/event/354999/contribution/1/material/slides/0.pdf

8BX, 140PU, 2GeV

2GeV

Red: 8BX 140 PU

Blue: 8BX 140 PU + 2ttBar

X-axis range (0,100)

Layer 10

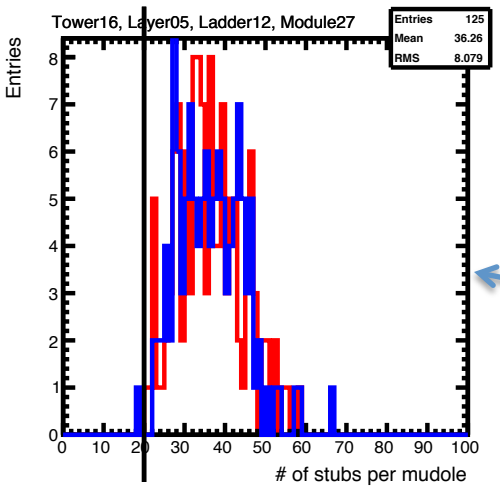
Layer 9

Layer 8

Layer 7

Layer 6

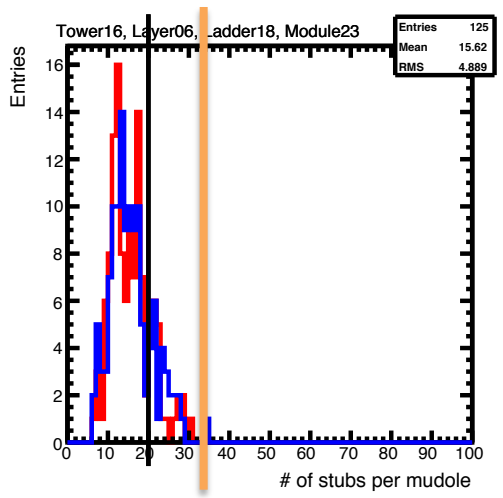
Layer 5



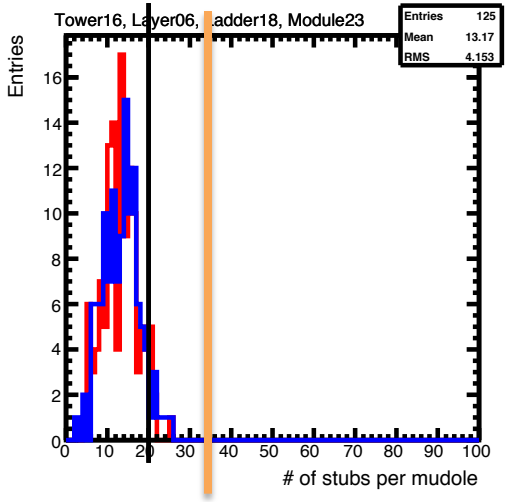
Need more bandwidth for high PU

- Number of stub distributions for 8BX
  - red: 140(or 200)PU; blue: 140(or 200)PU+ttbarttbar

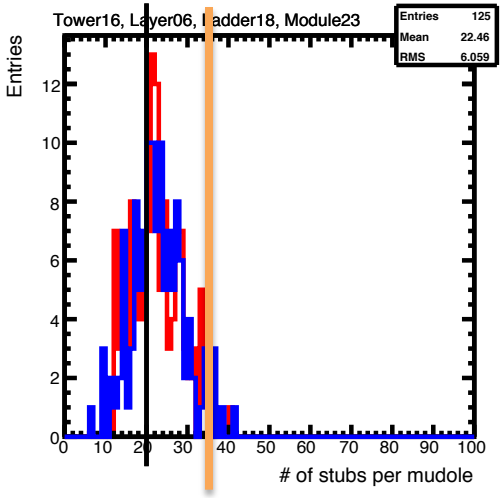
2GeV 140PU



3GeV 200PU

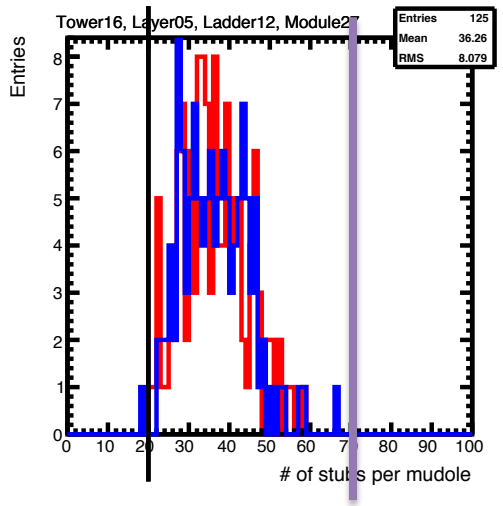


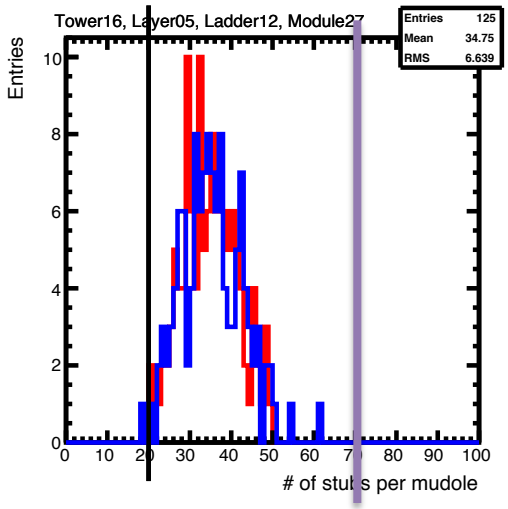
2GeV 200PU

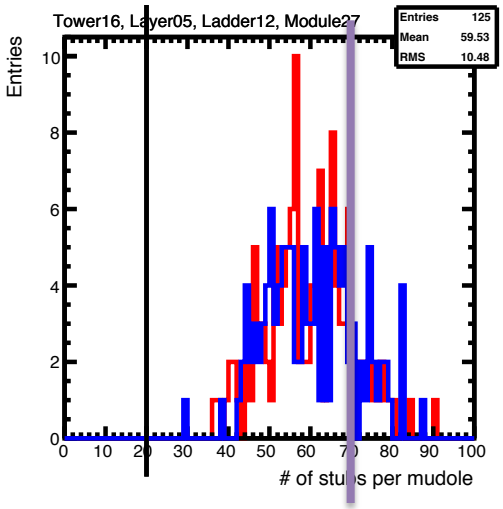


Layer 6

Layer 5







New proposals to increase the bandwidth

- Current repartition for the CIC to GBT data block
  - LP-GBT: 256bits(trigger) / 64bits(raw)
  - 10G-GBT: 512b / 128b
    - Requires 640 MHz output links for the CIC
    - Higher power consumption
    - Potentially 2x more data in the DTC boards

Mode	Bits	N_{stub}/CIC	N_{stub}/module (2 CIC)
LP-GBT	256	10	20
LP-SEC	320	14	28
LP-LEC	384	17	34
10G-SEC	640	29	58
10G-LEC	768	35	70

- Potential increase of the GBT bandwidth using different data correction schemes
  - LP-GBT with strong error correction scheme (LP-SEC): 320b / 64b
  - LP-GBT with light error correction scheme (LP-LEC): 384b / 64b
  - 10G-GBT with strong error correction scheme (10G-SEC): 640b / 128b
  - 10G-GBT with light error correction scheme (10G-LEC): 768b / 128b

Reference:
S.Viret: https://indico.cern.ch/event/354999/contribution/1/material/slides/0.pdf
P.Moreira: https://espace.cern.ch/GBT-Project/Talks/lpGbtProject.2015.02.23.pptx

LYON