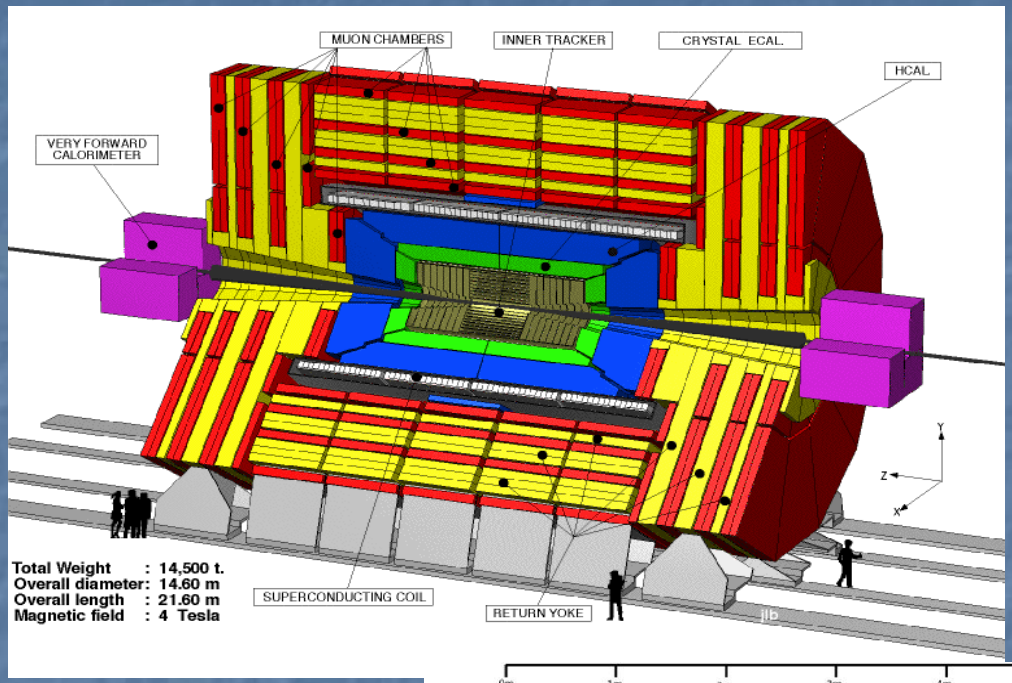
ATLAS/CMS/LCD RD53 collaboration:

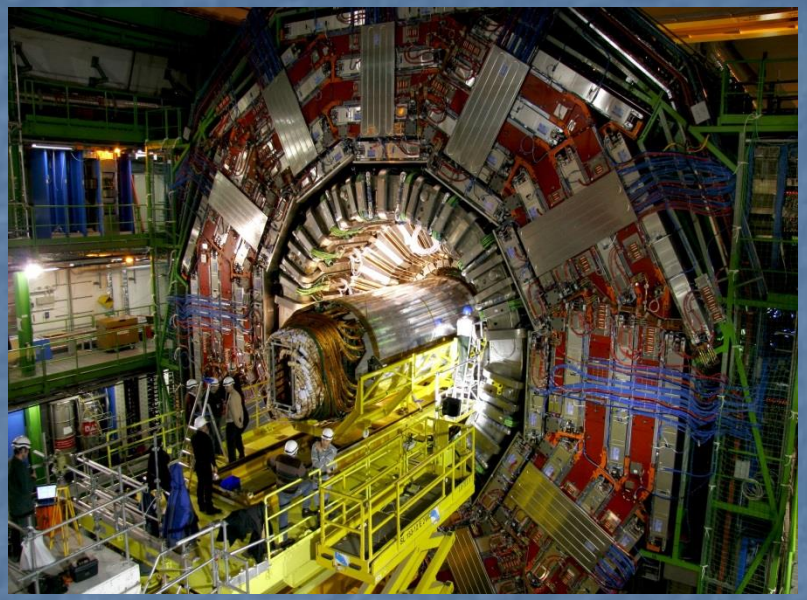
Pixel readout integrated circuits for extreme rate and radiation.

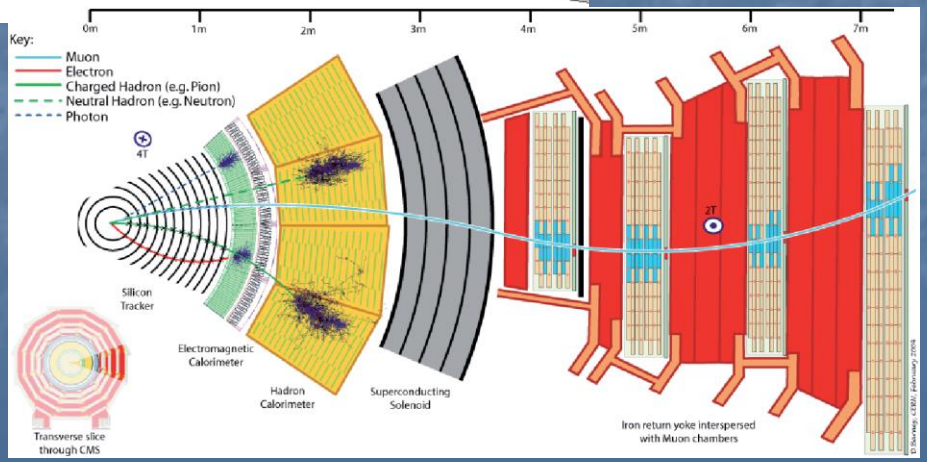
ATLAS and CMS phase 2 pixel upgrades

Jorgen Christiansen on behalf of RD53

CMS experiment

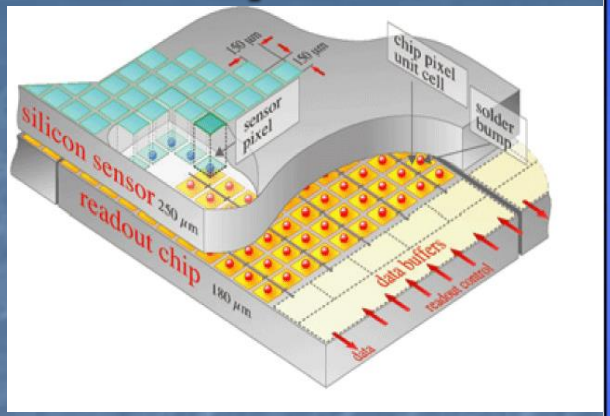


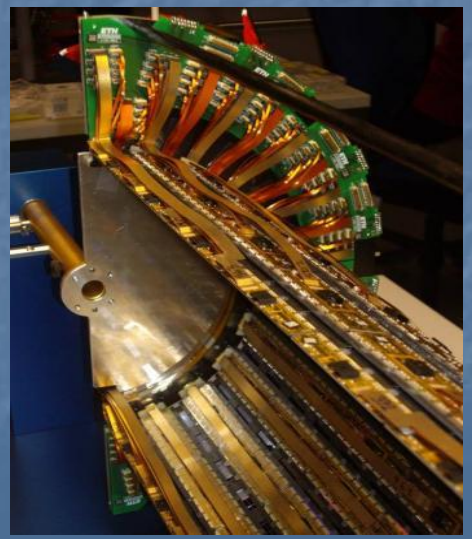


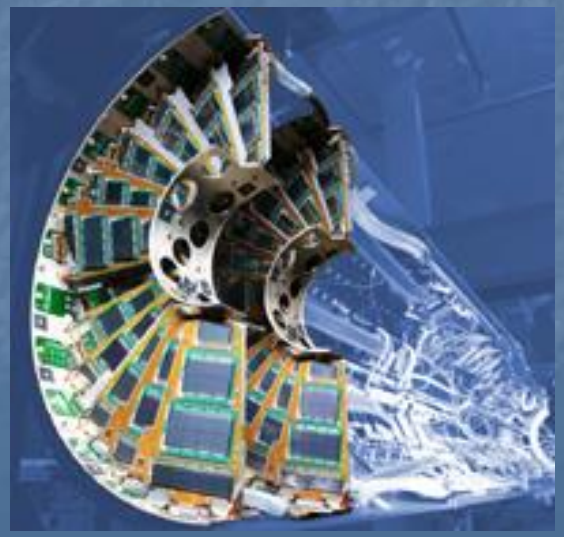


Current CMS pixel

- 100um x 150um hybrid pixels
- 3 barrel layers, 2 disks
- ~1m^2 sensitive surface
- 40MHz clock/sampling
- Hit rate: <100MHz/cm^2
- 100KHz trigger rate
- 250nm pixel ASIC
  - Column drain architecture with data buffering in End Of Column (EOC).
  - Analogue readout (also on optical links)
- Radiation tolerance: ~100Mrad, ~10^{15}neu/cm^2
- ~3KW power

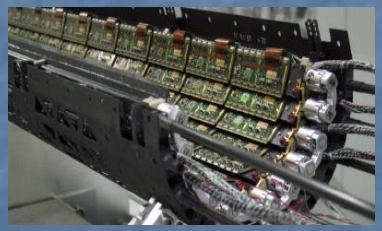


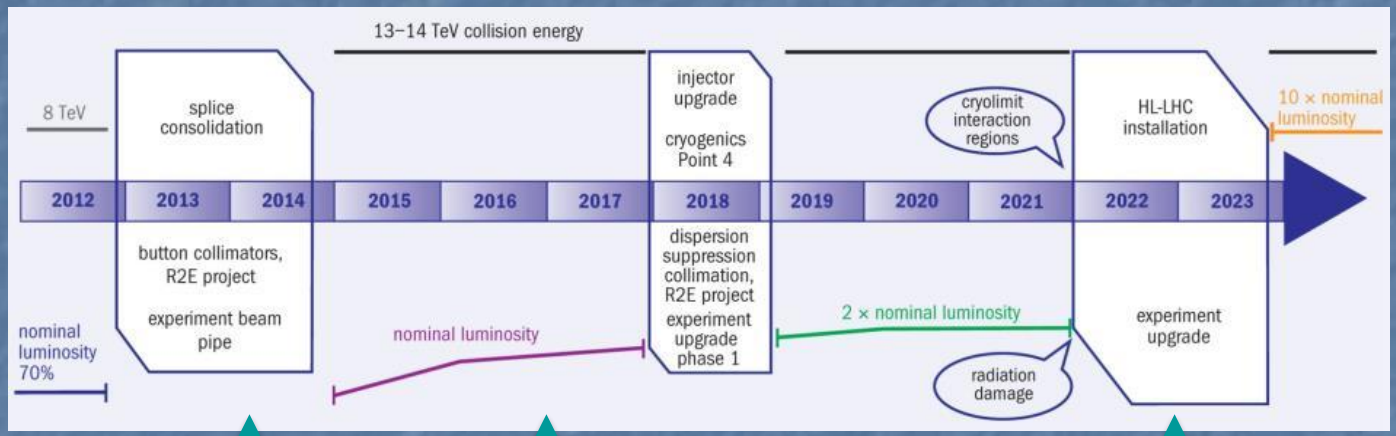




Pixel upgrades

- Current LHC pixel detectors have clearly demonstrated the feasibility and power of pixel detectors for tracking in high rate environments
- Phase0/1 upgrades: Additional pixel layer, ~4 x hit rates
  - ATLAS IBL : Addition of inner B layer with new 130nm pixel ASIC (FEI4).
  - CMS: New pixel detector with modified 250nm pixel ASIC (PSI46DIG).
- **Phase2 upgrades**: 20-30 x hit rates, 2-4 x better resolution, 10 x trigger rates, 16 x radiation tolerance, Increased forward coverage, less material, , ,
  - Installation: ~ 2022
  - Relies fully on significantly improved performance from next generation pixel chips.





ATLAS Pixel IBL

CMS Pixel phase1

CMS & ATLAS phase 2 pixel upgrades

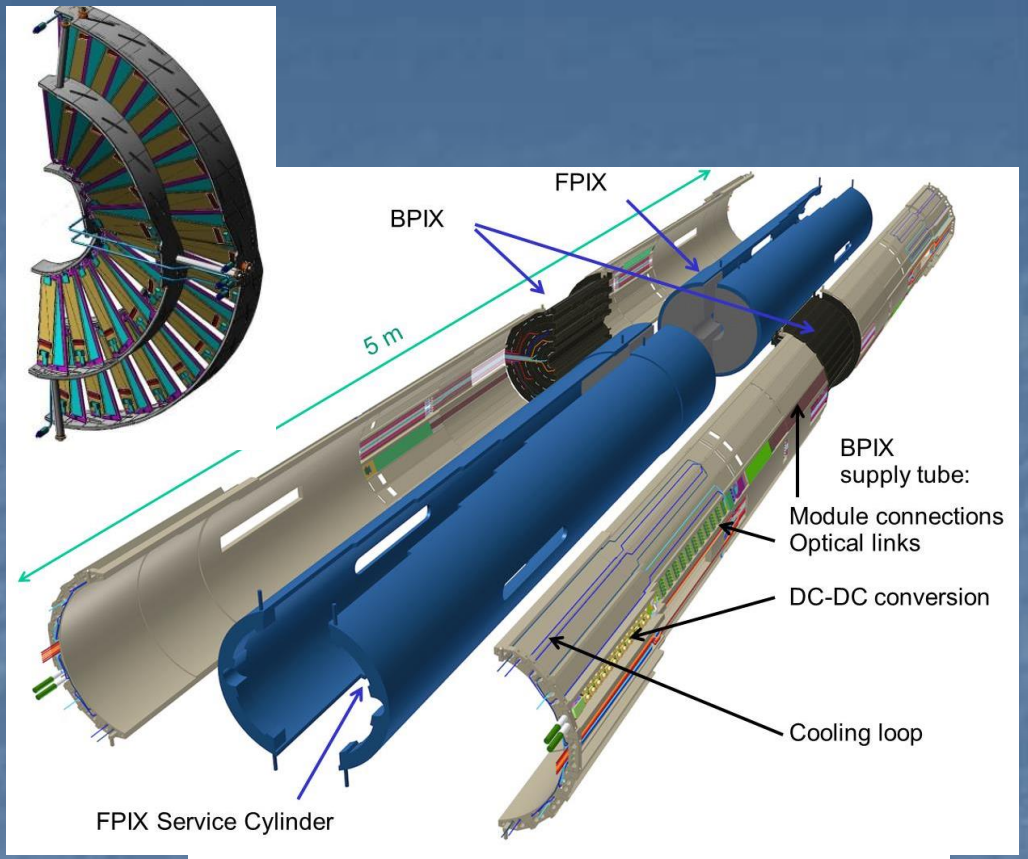
100MHz/cm^2

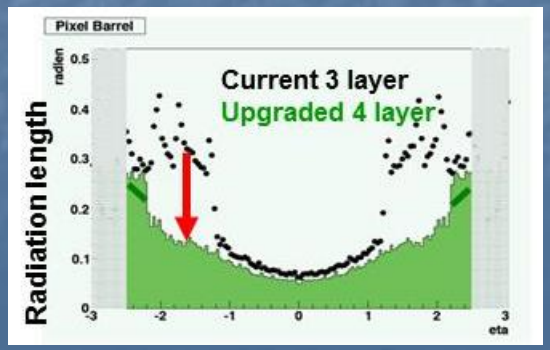
400MHz/cm^2

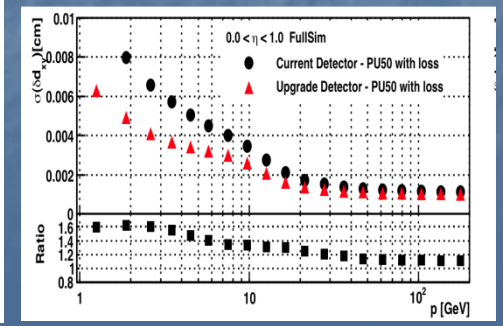
2-3GHz/cm^2

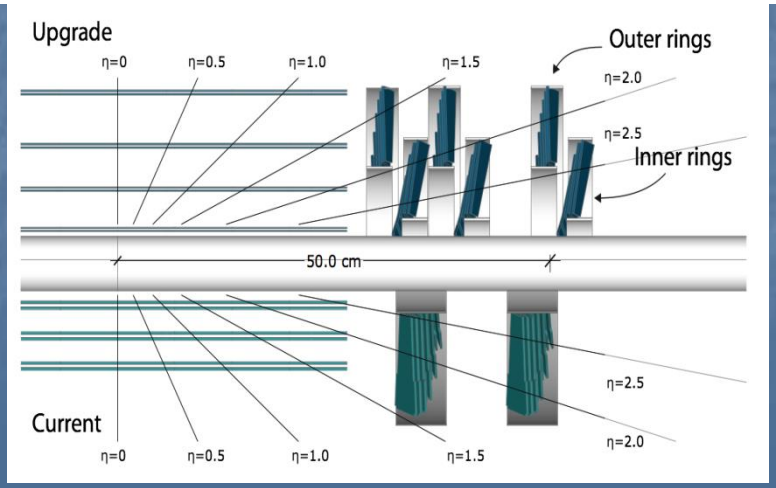
Phase 1 upgrade

- ~4 x hit rates: ~400MHz/cm^2
  - Higher luminosity & Closer to interactions
- Same pixel size: 100x150um^2
- Additional barrel layer: 3 -> 4
  - Closer to interactions
- Additional end-cap disc: 2 ->3
- ~1.5m^2
- Modified 250nm pixel chip
  - Lower detection threshold: 3400e -> ~1800e
  - Increased EOC buffering
  - Digital readout
- Lower material budget (in forward region)
- On detector power conversion: DC/DC
- Installation: 2016/2017
- TDR: http://cds.cern.ch/record/1481838/files/CMS-TDR-011.pdf





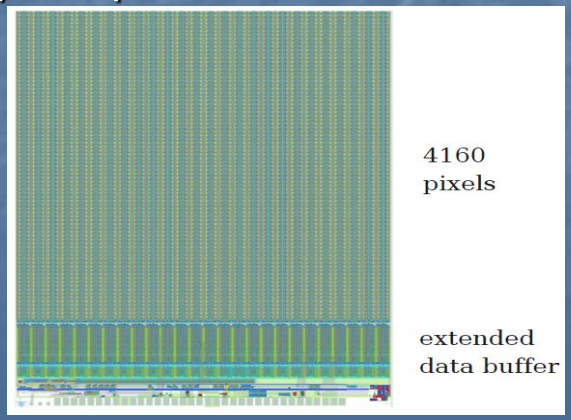


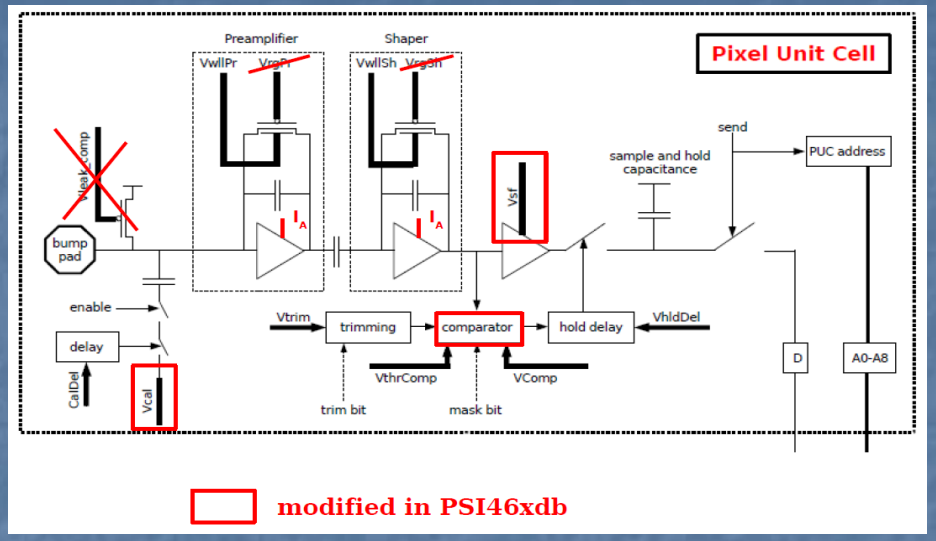


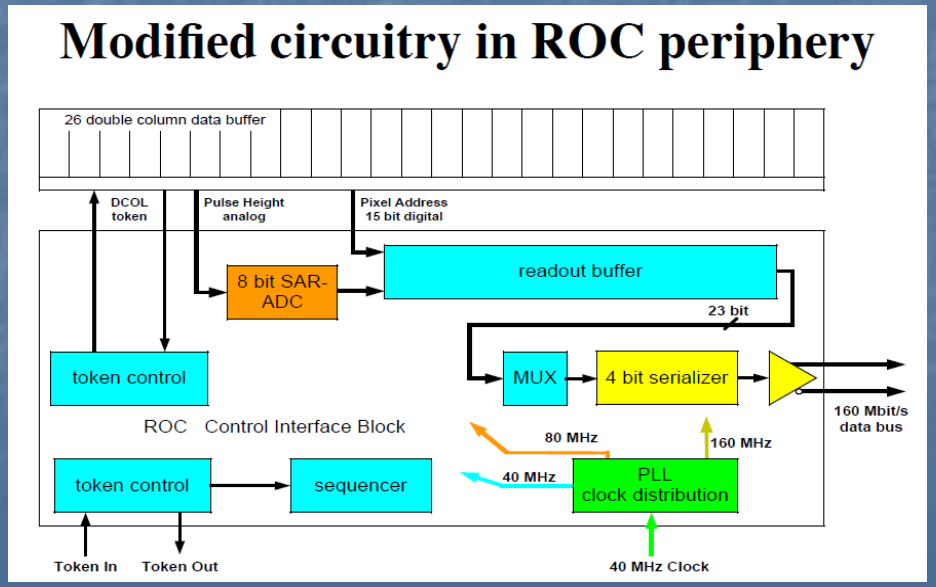
Transverse impact parameter resolution with 50PU

CMS phase1 pixel chip: PSI46dig

- Maintain same architecture
  - Analog charge measurement
  - 1 sample buffer (capacitor) in pixel
  - Column drain architecture
  - Latency storage in EOC
  - No clock to pixel array
- Technology: 250nm
  - Well known and relatively cheap
- Modifications
  - Lower effective threshold
    - Within 25ns: 3400e –> 1800e
  - Increased buffering in EOC
  - On-chip digitization in EOC
  - Faster column transfer for dedicated inner layer chip



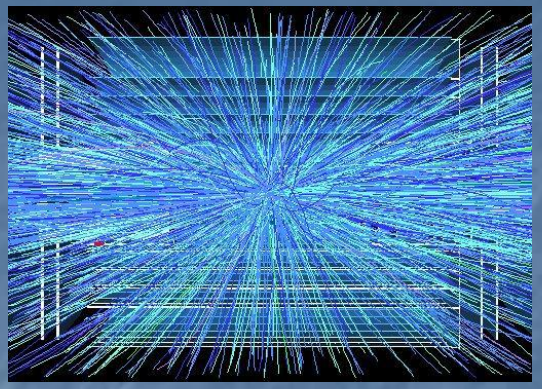


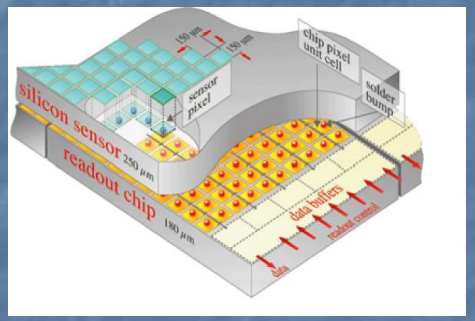


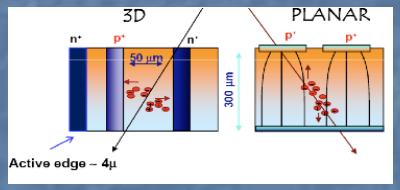
Phase 2 pixel challenges

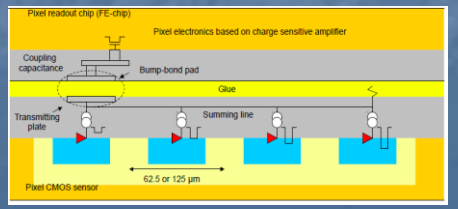
- ATLAS and CMS phase 2 pixel upgrades very challenging
  - Very high particle rates: 500MHz/cm^2
    - Hit rates: 2-3 GHz/cm^2 (factor ~20 higher than current pixel detectors)
  - Smaller pixels: ~¼ (50um x 50um, 25um x 100um)
    - Increased resolution
    - Improved two track separation (jets)
    - 100um x 100um in outer layers for lower power
  - Participation in first/second level trigger ? (no)
    A. 40MHz extracted clusters (outer layers) ?
    B. Region of interest readout for second level trigger ?
  - Increased readout rates: 100kHz -> 1MHz
    - 100x higher data rates: 10x hit rate x 10x trigger rate
  - Low mass -> Low power

  Very similar requirements (and uncertainties) for ATLAS & CMS
- Unprecedented hostile radiation: 1Grad, 10^{16} Neu/cm^2
  - Hybrid pixel detector with separate readout chip and sensor.
  - Phase2 pixel will get in 1 year what we now get in 10 years
  - 10.000 higher than space applications !
- Pixel sensor(s) not yet determined
  - **Planar**, 3D, Diamond, HV CMOS, , ,
  - Possibility of using different sensors in different layers
  - Final sensor decision may come relatively late.
- Complex, high rate and radiation hard pixel readout chips





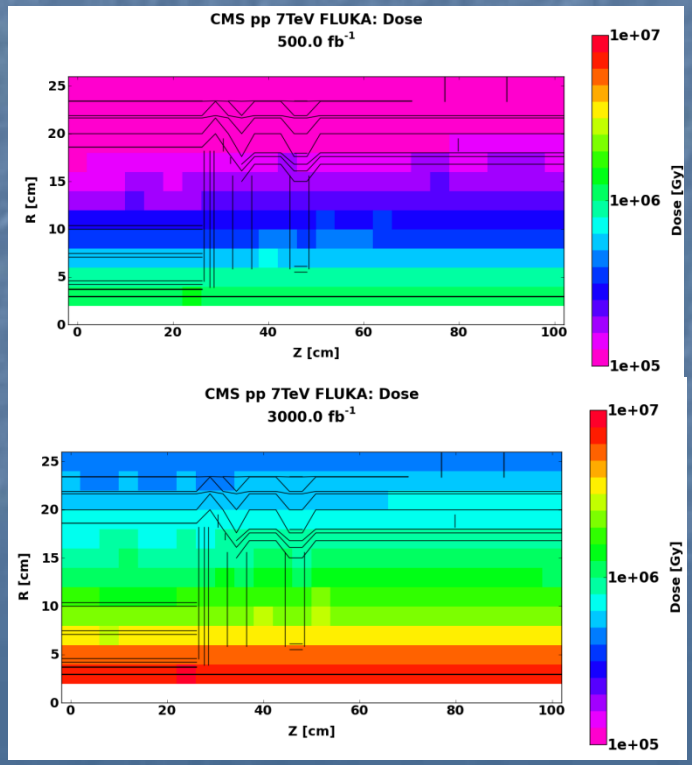




ATLAS HVCMOS program

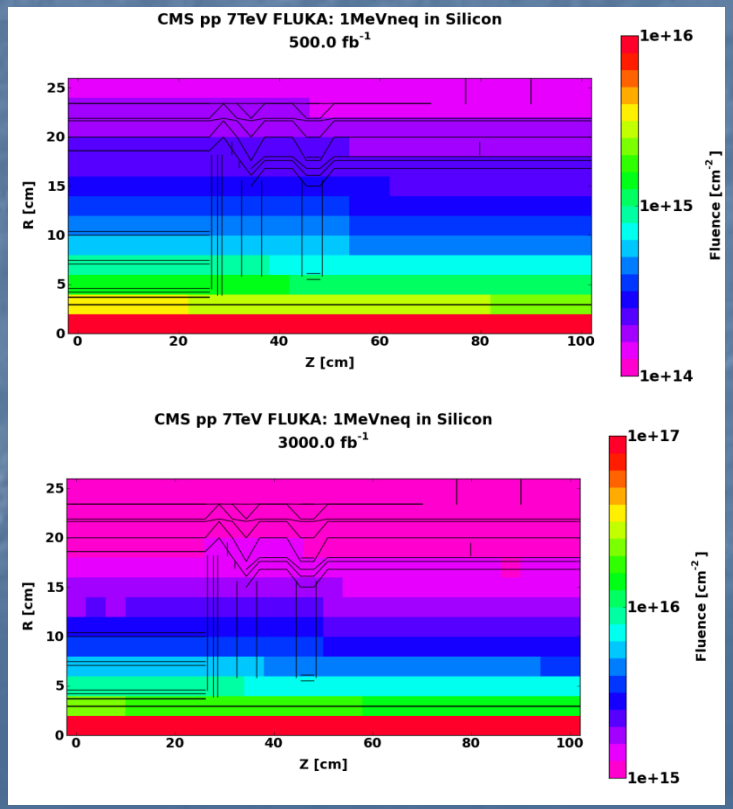
Radiation levels

- TID & Hadrons
- First layer will get ~1Grad, ~2 10^{16} Neu/cm^2 over 10years.
  - Feasible for both sensor and chip ?
  - Need to replace inner layer after few years ? (replaceability and cost)
  - Radiation decreases ~1/2 for each layer: 1, ~½ , ~¼ , ~1/10
  - Annealing scenario critical: -20°C , ~2weeks/year at room temperature
    - To define/understand what the problems are for the chip and the sensor
- Radiation levels do not decrease in forward direction
  - Major challenge for power services and optical link interfaces !



Phase1

Phase2



SEU rate guesstimates

- Basic assumptions:
  - 65nm storage cell (FF, latch, RAM) high energy hadron cross-section: ~10^{-14}
  - HEH rate: 500MHz/cm^2
    (inner layer and very conservative)
- EOC: 1kbit config + 1Kbit state
  - Single Event Functional Interrupt (SEFI): ~100s
  - Requirement: less than one per day per chip

  Full fault tolerance required: TMR, Triple Modular Redundancy
- Pixel cell: 16bit config + 16bit state: ~160k pixels per chip
  - 10 pixel cells per chip affected every second
  - Can possibly also affect function of whole chip (e.g. token passing)

  Full TMR required
- Hit data corruption: 24 bit, 10us storage
  - Hit data corruption probability: ~10^{-9}
  - Requirement: < 10^{-4}

  No SEU protection of hit data required in data buffers

ATLAS – CMS RD collaboration

- Similar/identical requirements, same technology choice and limited availability of rad hard IC design experts in HEP makes this ideal for a close CMS – ATLAS RD collaboration
  - Even if we do not make a common pixel chip
- Workshop between ATLAS and CMS pixel communities confirmed this in 2012.
- Forming a RD collaboration has attracted additional groups and collaborators
  - Synergy with CLIC pixel (and others): Technology, Rad tol, Tools, etc.
- Institutes: 20
  - ATLAS: CERN, Bonn, CPPM, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, RAL, UC Santa Cruz.
  - CMS: Bari, Bergamo-Pavia, CERN, Fermilab, Padova, Perugia, Pisa, PSI, RAL, Seville, Torino.
- Collaborators: ~100
- Collaboration organized with Institute Board (IB) with technical work done in specialized Working Groups (WG)
  - Monthly working group meetings
  - Collaboration meeting 2 times per year
- Work program covers 3(4) years: 2013/14 – 2016/17
  - Full scale demonstrator chip in 2016
  - Will be extended if appropriate:
    A. Common design ?,
    B. Support to experiment specific designs

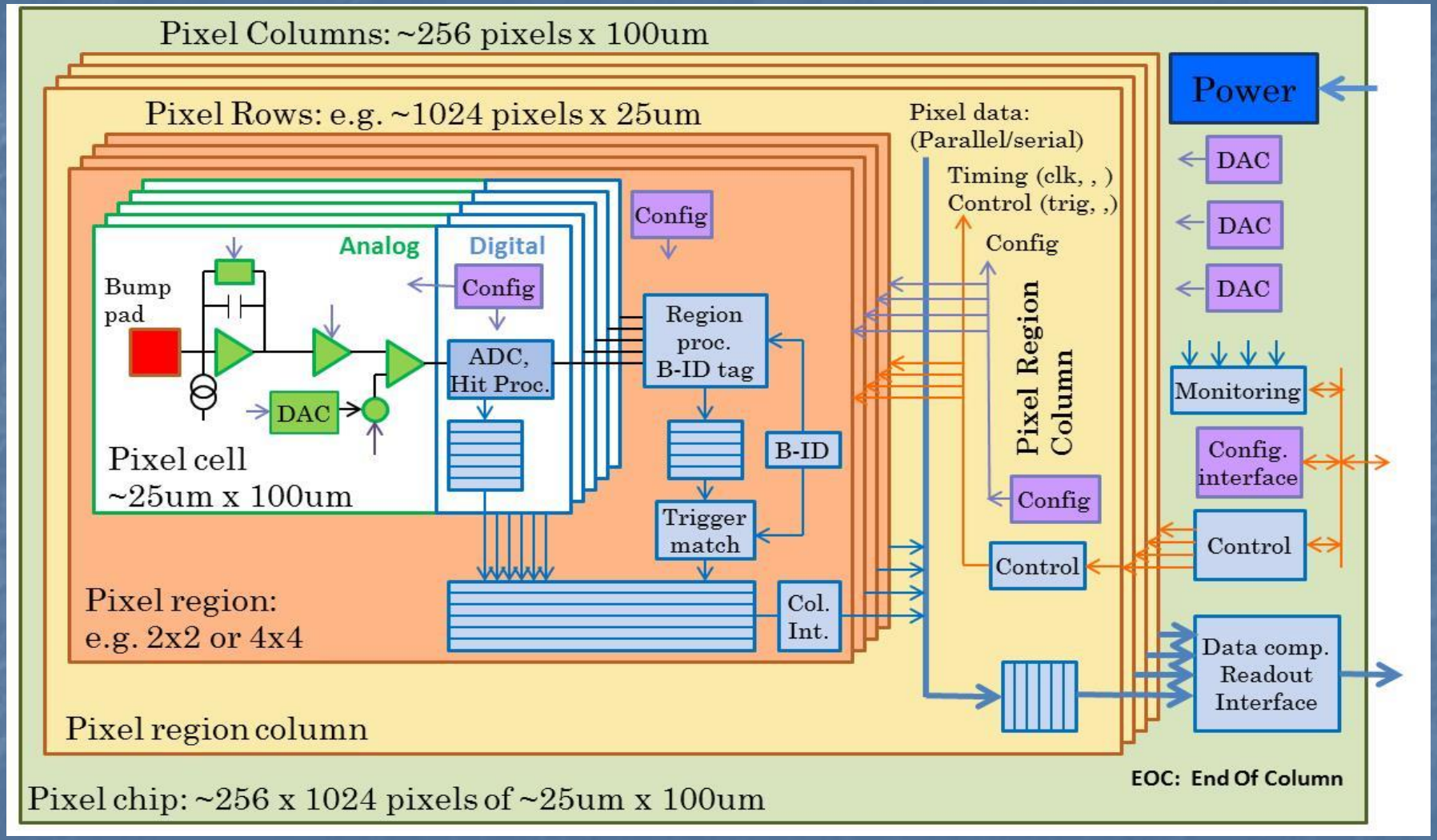
Pixel chip

- Pixel readout chips critical for schedule to be ready for phase 2 upgrades
  - Technology: Radiation qualification
  - Building blocks: Design, prototyping and test
  - Architecture definition/optimization/verification
  - Chip prototyping, iterations, test, qualification and production
  - System integration
    - System integration tests and test-beams
  - Production and final system integration, test and commissioning
- Phase 2 pixel chip very challenging
  - Radiation
  - Reliability: Several storage nodes will have SEUs every second per chip.
  - High rates
  - Mixed signal with very tight integration of analog and digital
  - Complex: ~256k channel DAQ system on a single chip
  - Large chip: ~2cm x 2cm, ½ - 1 Billion transistors.
  - Very low power: Low power design and on chip power conversion
- Both experiments have evolved to have similar pixel chip architectures and plans to use same technology (65nm) for its implementation.
- Experienced chip designers for complex ICs in modern technologies that must work in a extremely harsh radiation environment is a scarce and distributed "resource" in HEP.

Pixel chip generations

Generation	Current FEI3, PSI46	Phase 1 FEI4, PSI46DIG	Phase 2
Pixel size	100x150um^2 (CMS) 50x400um^2 (ATLAS)	100x150um^2 (CMS) 50x250um^2 (ATLAS)	25x100um^2, 50x50um^2, 100x100um^2
Sensor	2D, ~300um	2D+3D (ATLAS) 2D (CMS)	2D, 3D, Diamond, MAPS ?
Chip size	7.5x10.5mm^2 (ATLAS) 8x10mm^2 (CMS)	20x20mm^2 (ATLAS) 8x10mm^2 (CMS)	**> 20 x 20mm^2**
Transistors	1.3M (CMS) 3.5M (ATLAS)	87M (ATLAS)	**~1G**
Hit rate	**100MHz/cm^2**	**400MHz/cm^2**	**2-3 GHz/cm^2**
Hit memory per chip	0.1Mb	1Mb	~16Mb
Trigger rate	100kHz	100KHz	200kHz - **1MHz**
Trigger latency	2.5us (ATLAS) 3.2us (CMS)	2.5us (ATLAS) 3.2us (CMS)	6 - 20us
Readout rate	40Mb/s	320Mb/s	**3-4Gb/s**
Radiation	**100Mrad**	**200Mrad**	**1Grad**
Technology	250nm	130nm (ATLAS) 250 nm (CMS)	**65nm**
Architecture	Digital (ATLAS) Analog (CMS)	Digital (ATLAS) Analog (CMS)	Digital
Buffer location	EOC	Pixel (ATLAS) EOC (CMS)	Pixel
Power	~1/4 W/cm^2	~1/4 W/cm^2	**~1/2 W/cm^2**

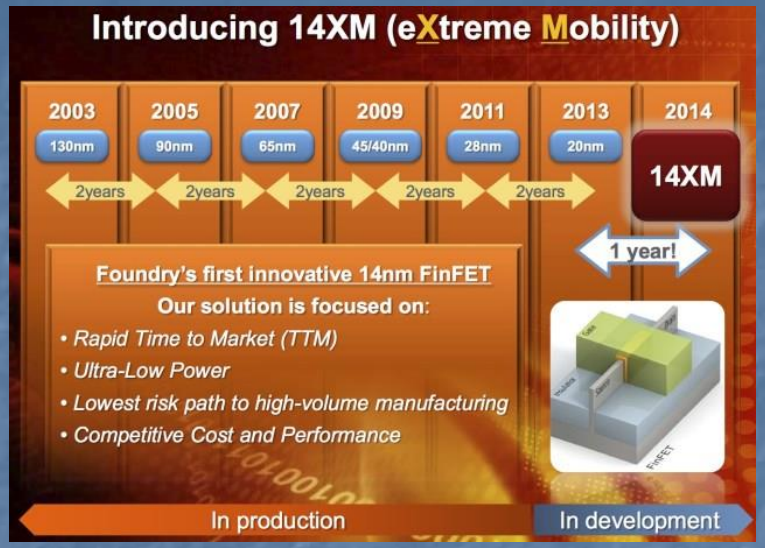
3rd generation pixel architecture

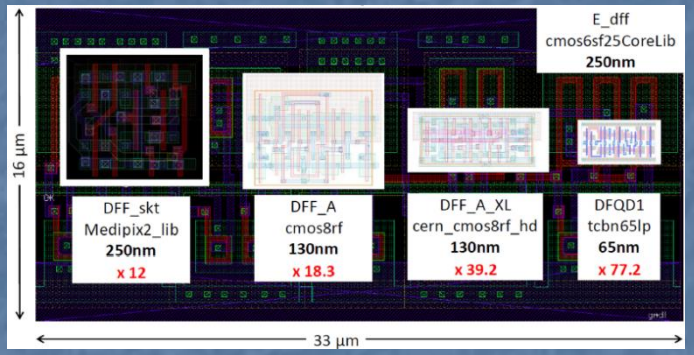


- 95% digital (FEI4 like)
- Charge digitization
- ~200k pixel channels per chip
- Pixel regions with buffering
- Data compression in End Of Column

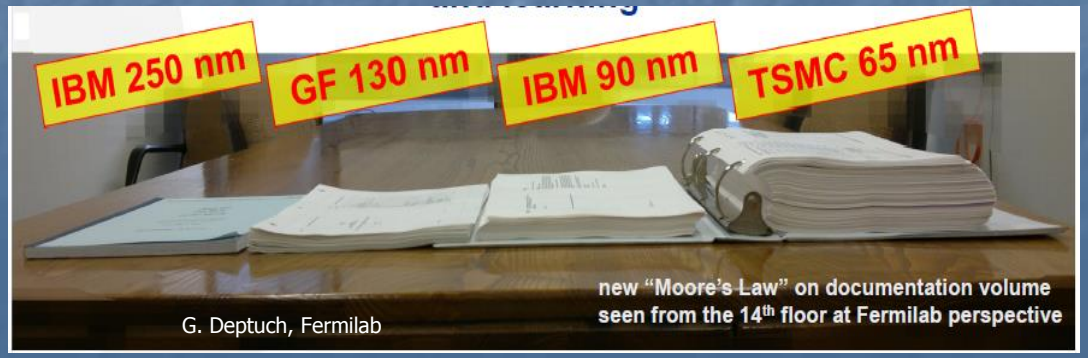
Why 65nm Technology

- Mature technology:
  - Available since ~2007
- High density and low power
- Long term availability
  - Strong technology node used extensively for industrial/automotive
- Access
  - CERN frame-contract with TSMC and IMEC
    - Design tool set
    - Shared MPW runs
    - Libraries
    - Design exchange within HEP community
- Affordable (MPW from foundry and Europractice, ~1M NRE for full final chips)
- Significantly increased density, speed, , , and complexity !





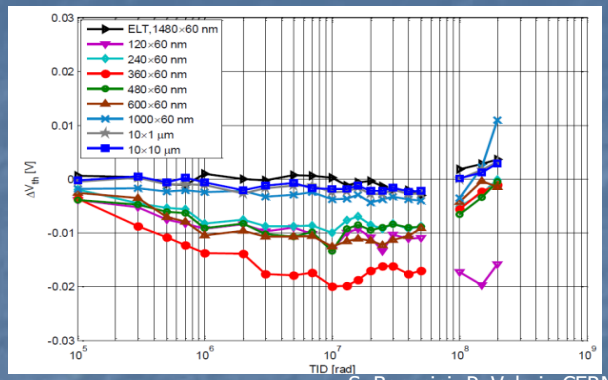
X. Llopart CERN



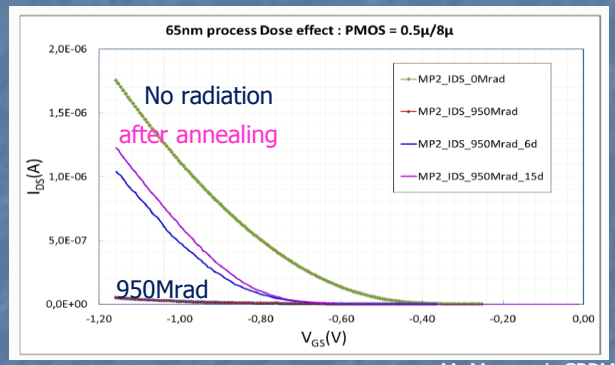
G. Deptuch, Fermilab

65nm Technology

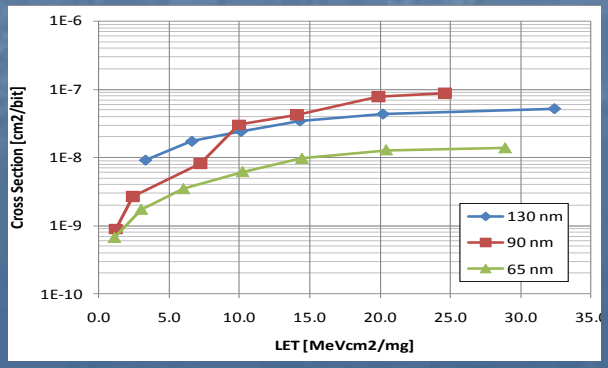
- Radiation hardness
  - Uses thin gate oxide
    - Radiation induced trapped charges removed by tunneling
    - More modern technologies use thick High K gate "oxide".
  - Verified for up to 200Mrad
  - To be confirmed for 1Grad
    - PMOS transistor drive degradation, Annealing ?
    - If significant degradation then other technologies must be evaluated and/or a replacement strategy must be used for inner pixel layers
  - CMOS normally not affect by NIEL
    - To be confirmed for 10^{16} Neu/cm^2
    - Certain circuits using "parasitic" bipolars to be redesigned ? (bandgaps)
  - SEU tolerance to be build in (as in 130 and 250nm)
    - SEU cross-section reduced with size of storage element, but we will put a lot more per chip
  - All circuits must be designed for radiation environment (e.g. Modified RAM)



S. Bonacini, P. Valerio CERN



M. Menouni, CPPM



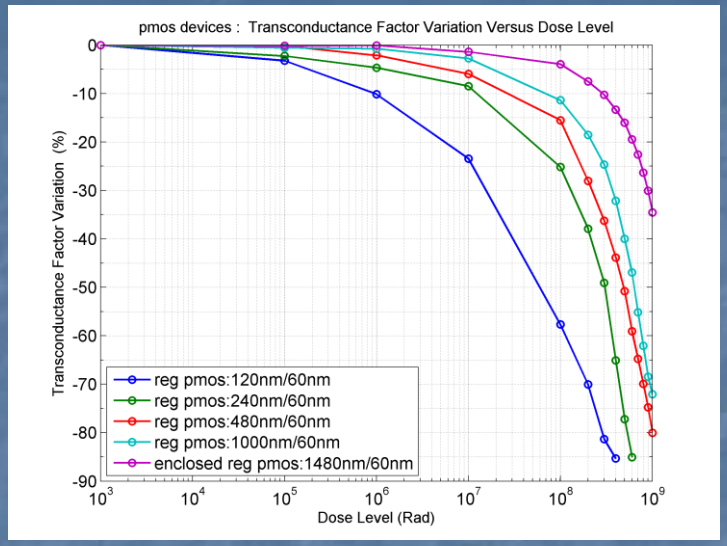
Working groups

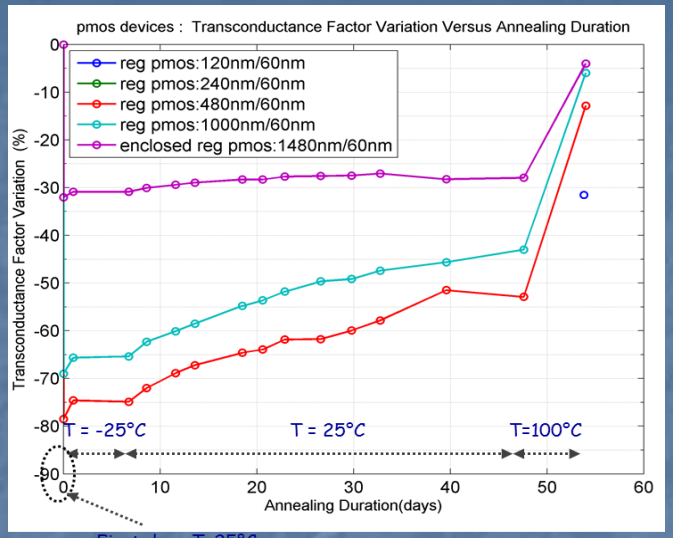
WG	Domain
WG1	Radiation test/qualification
Coordinate test and qualification of 65nm for 1Grad TID and10^{16} neu/cm^2 Radiation tests and reports. Transistor simulation models after radiation degradation Expertise on radiation effects in 65nm	
WG2	Top level
Design Methodology/tools for large complex pixel chip Integration of analog in large digital design Design and verification methodology for very large chips. Design methodology for low power design/synthesis. Clock distribution and optimization.	
WG3	Simulation/verification framework
System Verilog simulation and Verification framework Optimization of global architecture/pixel regions/pixel cells	
WG4	I/O
Development of rad hard IO cells (and standard cells if required) Standardized interfaces: Control, Readout, etc.	
WG5	Analog design / analog front-end
Define detailed requirements to analog front-end and digitization Evaluate different analog design approaches for very high radiation environment. Develop analog front-ends	
WG6	IP blocks
Definition of required building blocks: RAM, PLL, references , ADC, DAC, power conversion, LDO, , Distribute design work among institutes Implementation, test, verification, documentation	

Radiation WG

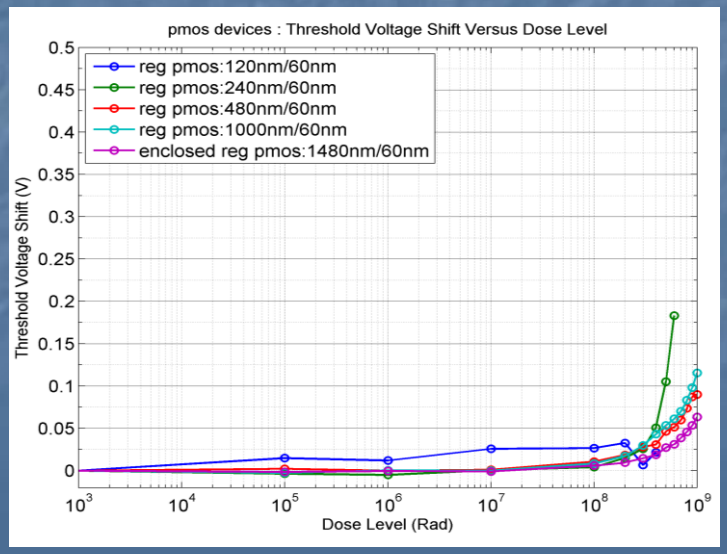
- Radiation test and qualification of baseline 65nm technology for radiation levels of 1Grad and 10^{16} neu/cm^2
- WG convener: Marlon Barbero, CPPM
- Activities and Status:
  - Defining radiation testing procedure
  - Test of 65nm transistors to 1Grad
    - NMOS: Acceptable degradation (20-30%)
    - PMOS: Severe radiation damage above 300Mrad (next slide)
      - Not yet full understanding of effects seen at these unprecedented radiation levels
      - Much less radiation degradation when radiated cold (-25^{o}C). Unexpected. Annealing effects to be verified.
      - Annealing depends on biasing during annealing: NEW
    - Systematic radiation/annealing studies required to be verified with pixel detector operation (cold -20^{o}C)
  - Test of circuits to 1Grad
    - Ring oscillators, Pixel chips (CERN, LBNL)
    - Some digital circuits remains operational up to 1Grad, depending on digital library used. (better than indicated by tests of individual transistors)
- Plans
  - Systematic radiation and annealing studies of 65nm basic devices and circuits including cold radiation
  - Hadron/neutron radiation tests for NIEL effects
  - Radiation test of basic transistors/structures in alternative technologies (for comparison/understanding)
  - Simulation models of radiation degraded transistors (if possible)
- CERN, CPPM, Fermilab, LBNL, New mexico, Padova

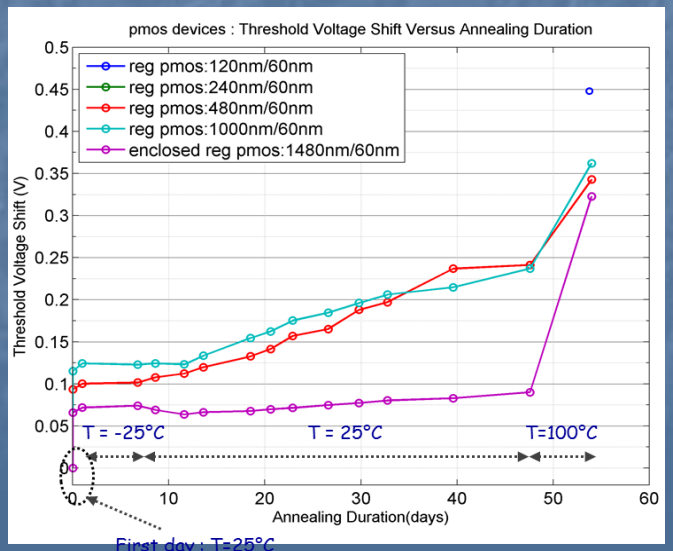
PMOS Radiation effects 65nm





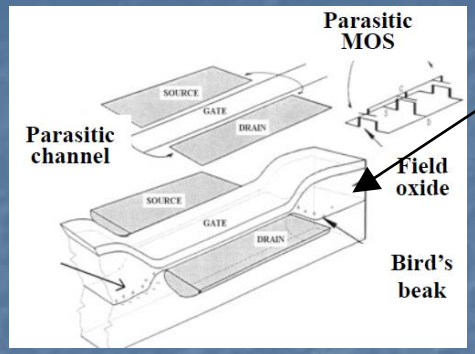
Transconductance





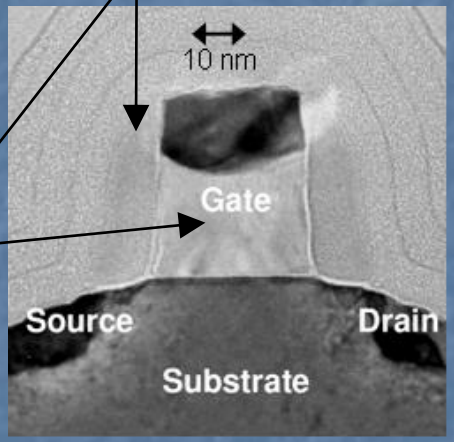
Vt shift

Radiation effects



Birds beak parasitic device

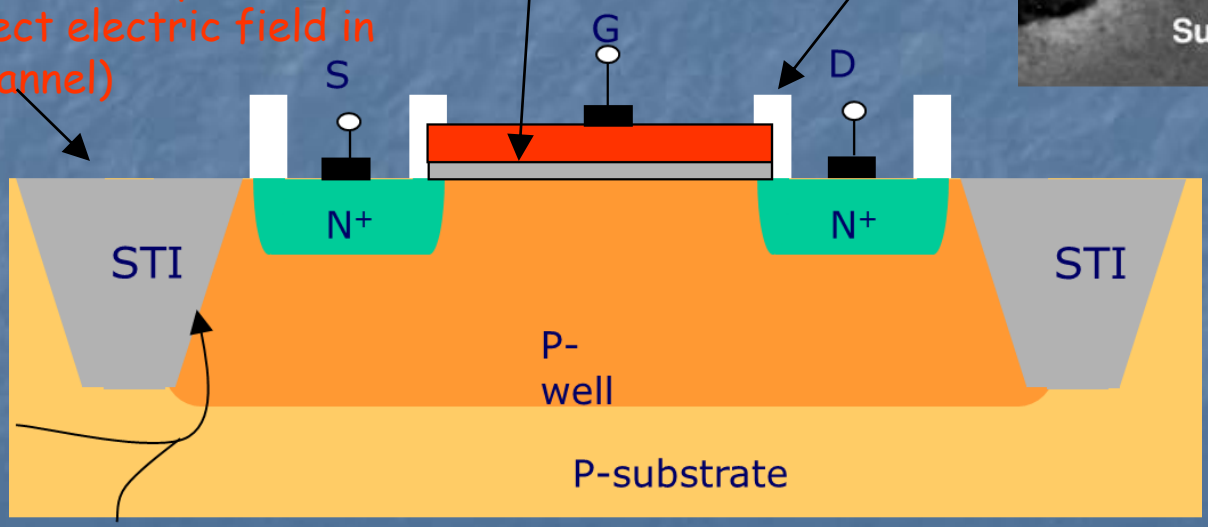
Spacer dielectrics may be radiation-sensitive



Charge buildup in gate oxide and interface states affects Vt

Thick Shallow Trench Isolation Oxide (~ 300 nm); radiation-induced charge-buildup may turn on lateral parasitic transistors and affect electric field in the channel)

Doping profile along STI sidewall is critical; doping increases with CMOS scaling, decreases in I/O devices

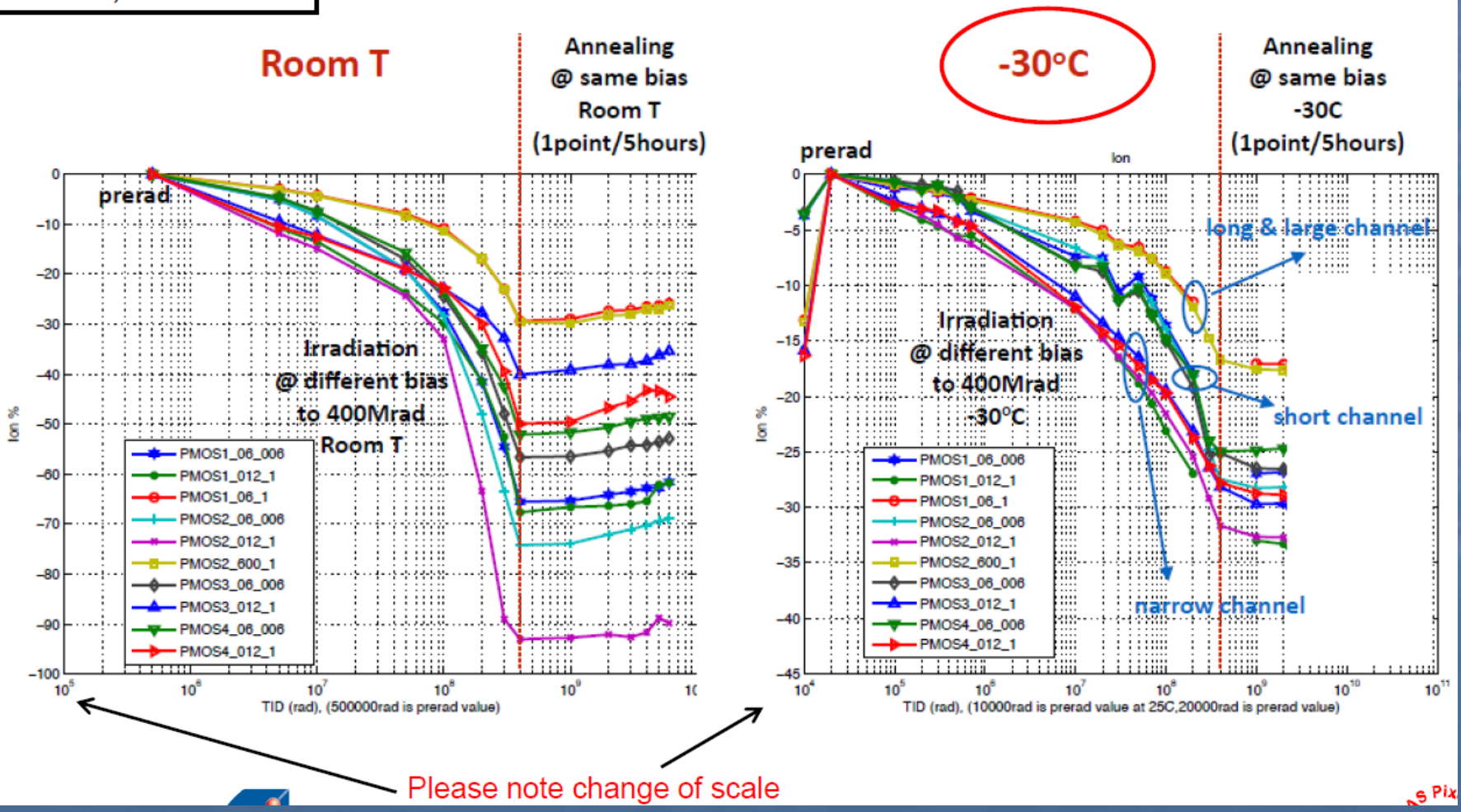


Increasing sidewall doping makes a device less sensitive to radiation (more difficult to form parasitic leakage paths)

Latest PMOS results

Low temperature

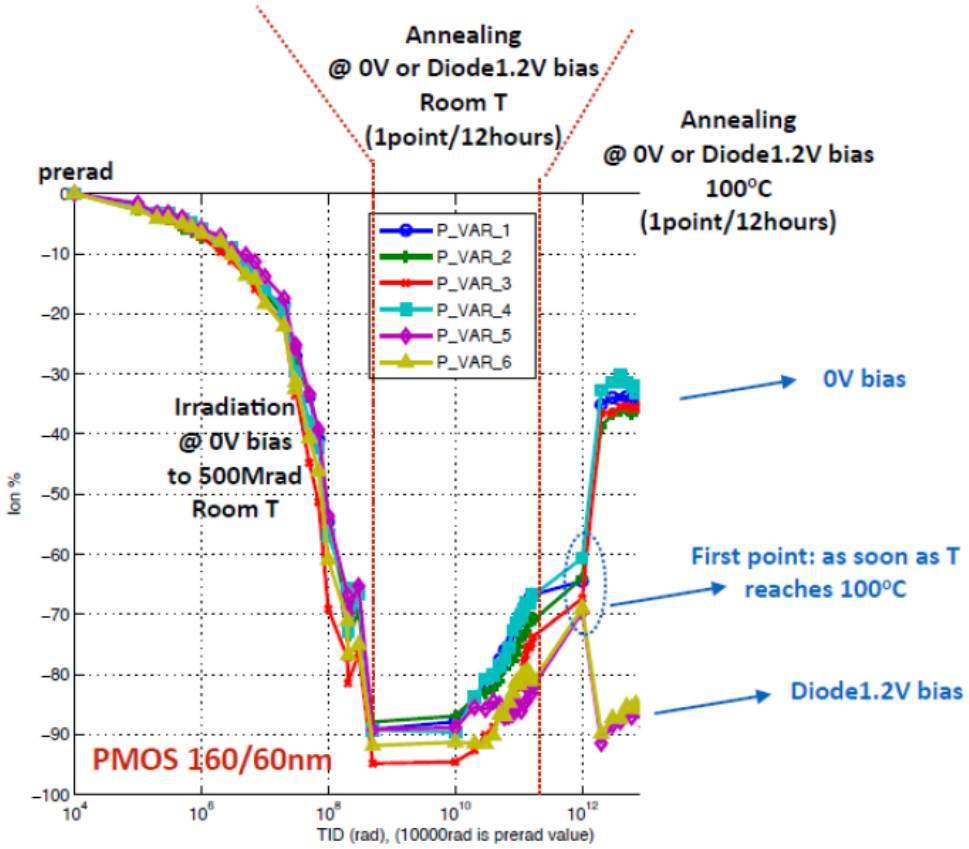
CERN, Jan. 2015



Evolution at high temperature

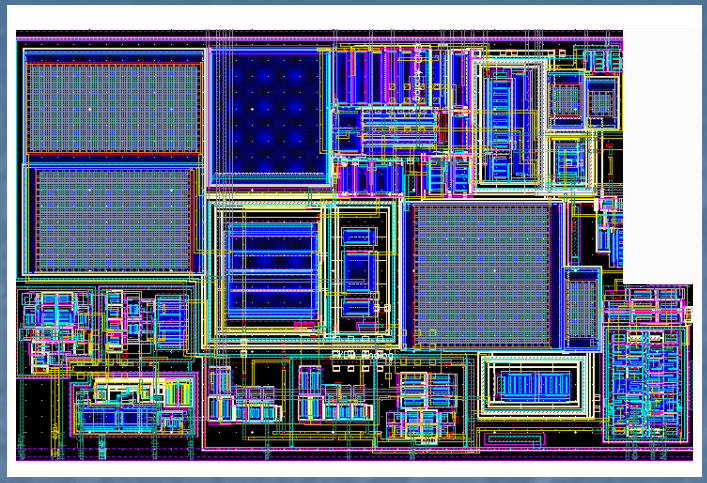
The evolution of the electrical characteristics of the transistors at high temperature (100°C) depends on the applied bias

CERN, Jan. 2015

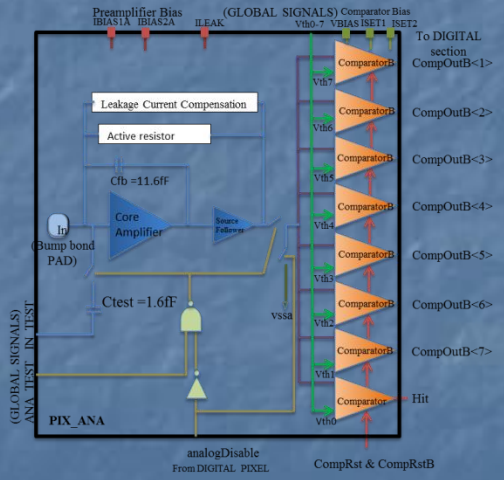


Analog WG

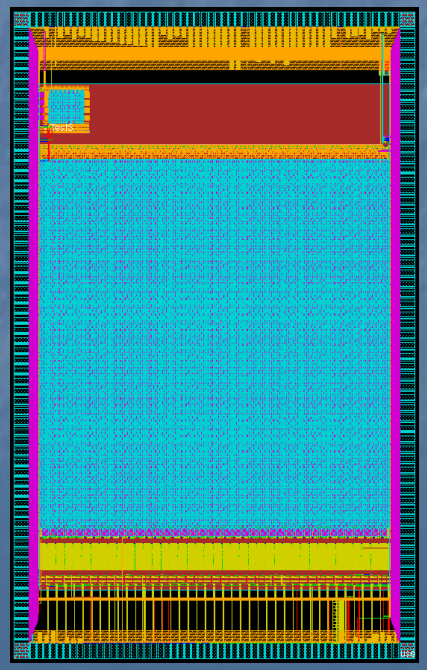
- Front-end requirements document
  - https://cds.cern.ch/record/1952563
  - Low threshold (100e), low power, ,
- 5 Groups designing and evaluating different front-end architectures
  - Designs prototyped and testing starting
- Convener: Valerio Re, Bergamo

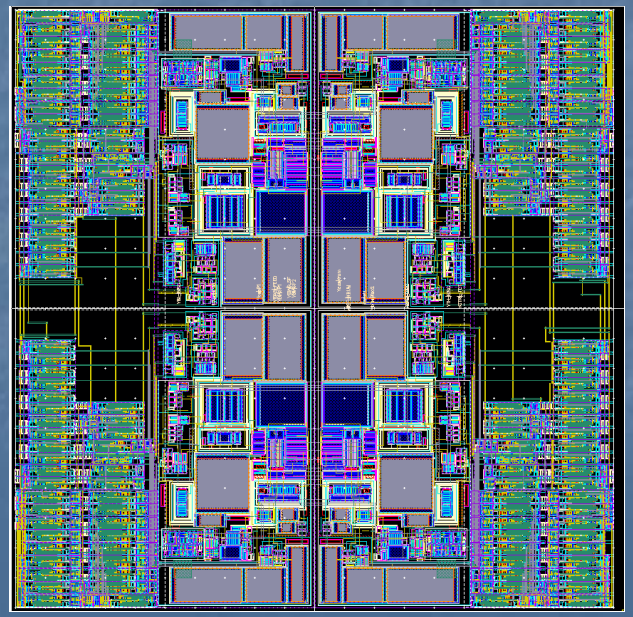


Example: Torino front-end and pixel array (INFN CHIPIX65)



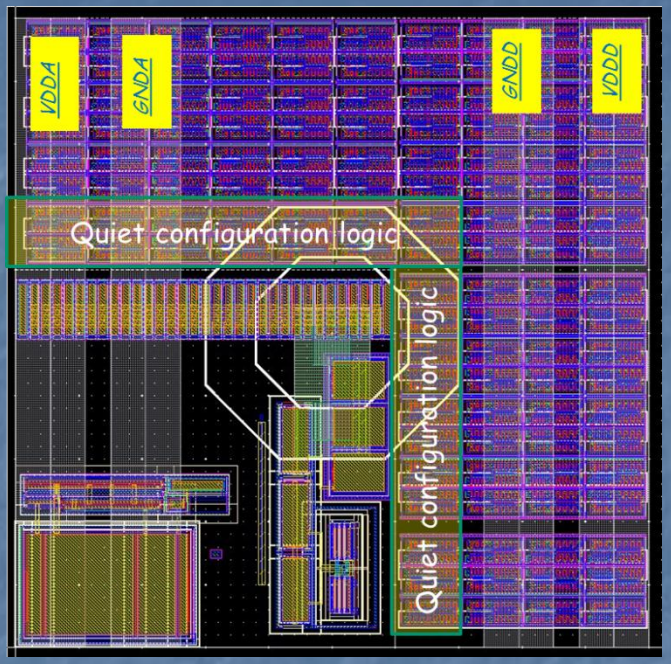
Fermilab (130nm)

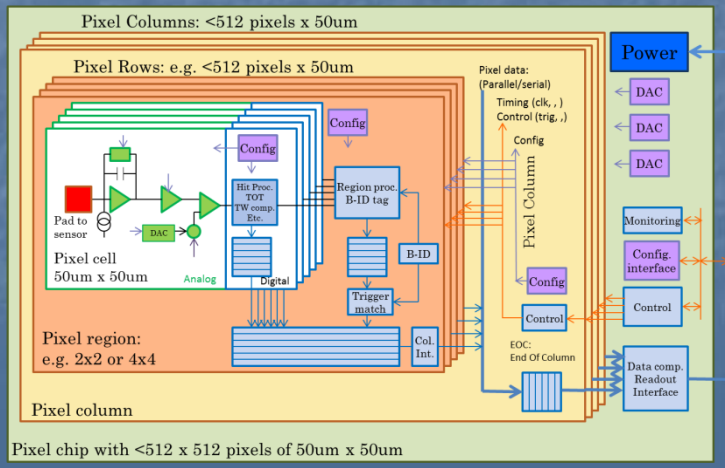




Top level WG

- Global architecture and floor-plan issues for large mixed signal pixel chip
- Convener: Maurice Garcia-Sciveres, LBNL
- Activities and status
  - Global floorplan issues for pixel matrix
    - 50x50um^2 – 25x100um^2 pixels with same pixel chip
      - ATLAS – CMS has agreed to aim for this
    - Compatibility with bigger pixels for outer layers
    - Global floor-plan with analog and digital regions
      - Analog islands in digital sea
  - Appropriate design flow
  - Column data bus versus serial links
  - Matrix structure for first pixel array test chip
- Plans
  - Submission of simplified pixel matrix test chip: 2015
  - Evaluation of different pixel chip (digital) architectures
    - Using simulation frameworks from simulation WG.
  - Full pixel chip demonstrator: 2016
- Bonn, LBNL, , , ,

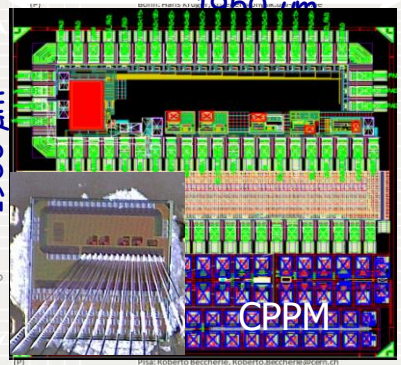




IP blocks

- ~ 20 IP blocks needed for pixel chip
  - ADC, DAC, Bandgaps, drivers, PLLs, serializers, IO driver/receivers, RAMs, Shut-LDO, Clock circuits, ,
  - Must all be rad hard: 1Grad
- Basic specs and data sheets of IP blocks defined
- Recommendations on how to make IPs
  - Lacked clear guidelines on how to make them sufficient radiation hard
- Many groups involved
- Most IPs prototyped and testing on-going
- Other projects show interest to use IPs
  - For non RD53 use: IPs belong to institutes.
- Convener: Jorgen Christiansen, CERN

Country	DE		FR	NL	IT - INFN				US	FR	UK	US	CZ	Comments	Contacts
Group	Bonn	CERN	CPPM	NIKHEF	Bari Pavia Berg	Milano	Padova	Pisa	Torino	LBNL	LPNHE	RAL Swin	Oxford	Prague	
ANALOG: Coordination with analog WG															
Temperature sensor.		O			(P)			(P)					(P)		CPPM: Mohsine Menouni, menouni@cppm.in2p3.fr
Radiation sensor		O			(P)			(P)					(P)		CPPM: Mohsine Menouni, menouni@cppm.in2p3.fr
HV leakage current sensor.		O						(P)					(P)		CPPM: Mohsine Menouni, menouni@cppm.in2p3.fr
															Pavia/Bergamo: Gianluca Traversi, gianluca.traversi@unibg.it
Band gap reference															CPPM: Mohsine Menouni, menouni@cppm.in2p3.fr
															CERN: Stefano Michelis, Stefano.Michelis@cern.ch
		O	O	(P)	O						(P)			3 Groups	NIKHEF: Vladimir Gromov , vgromov@nikhef.nl
Self-biased Rail to Rail analog buffer	(P)		(P)	(P)											RAL: Steve Thomas, stephen.thomas@stfc.ac.uk
MIXED											O		(P)		NIKHEF: Vladimir Gromov , vgromov@nikhef.nl
8 – 12 bit biasing DAC			(P)		O								O	2 groups	Bari: Flavio Loddo, flavio.loddo@ba.infn.it Prague: Gordon Neue, Gordon.Neue@fjfi.cvut.cz
10 - 12 bit slow ADC for monitoring															Bari: Cristoforo Marzocca, marzocca@poliba.it CPPM: Mohsine Menouni, menouni@cppm.in2p3.fr;
		O	O		O									3 Groups	CERN: Sandro Bonacini, sandro.bonacini@cern.ch
PLL for clock multiplication	O	(P)		(P)			(P)	(P)	(P)		(P)	(P)			Bonn: Hans Kruger, krueger@physik.uni-bonn.de
High speed serializer (~Gbit/s)	O	(P)		(P)				(P)			(P)	(P)		Together	(NIKHEF: Vladimir Gromov , vgromov@nikhef.nl) Bonn: Hans Kruger, krueger@physik.uni-bonn.de
															(NIKHEF: Vladimir Gromov , vgromov@nikhef.nl)
(Voltage controlled Oscillator)				(P)		O	(P)	(P)						Needed ?	Padova: Daniele Vogrig, vogrig@dei.unipd.it (Pisa: Guido Magazzu, Guido.Magazzu@cern.ch)
Clock recovery and jitter filter	O	(P)					(P)				(P)				(NIKHEF: Vladimir Gromov , vgromov@nikhef.nl)
Programmable delay	O	(P)					(P)								Bonn: Hans Kruger, krueger@physik.uni-bonn.de
DIGITAL															
SRAM for pixel region	(P)	(P)				O									
SRAM/FIFO for EOC.	(P)	(P)				(P)		(P)							
EPROM/EFUSE	(P)	O	(P)												
OICE storage cell / config reg	(P)		O			(P)		(P)							
LP Clock driver/receiver	(P)				O										
(Dedicated rad hard digital library)	(P)	(P)	(P)					O							
(compact mini digital library for pixels)	(P)	(P)	(P)					O							
IO: Coordination with IO WG															
Basic IO cells for radiation	(P)	O													
Low speed SLVS driver (<100MHz)	(P)	(P)				O			(P)	(P)					
High speed SLVS driver (~1Gbits/s)	(P)	(P)				O			(P)						
SLVS receiver	(P)	(P)				O			(P)						
1Gbits/s drv/rec cable equalizer															
C4 and wire bond pads	(P)	O													
(IO pad for TSV)	O		(P)												
Analog Rail to Rail output buffer	O		(P)												
Analog input pad	O														
POWER															
LDO(s)	O	(P)	(P)	(P)					(P)	(P)					
Switched capacitor DC/DC		(P)													
Shunt regulator for serial powering	O			(P)											
Power-on reset															
Power pads with appropriate ESD	(P)	O													
SOFT IP: Coordination with IO WG															
Control and command interface		(P)		(P)				O							
Readout interface (E-link ?)		(P)		(P)				O							

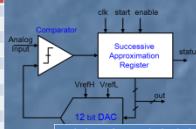


12 bit Monitoring ADC

Parameter	Value
Supply voltage	1.2 V (±10%)
Temperature range	-40 °C to +60 °C
Architecture	SAR
Conversion clock Clkc	312 kHz (40 MHz CLK/128) or lower ?
Resolution	12 bit
Input range	0 to 1 V (LSB = 244 μV)
Integral Non Linearity (INL)	± 1 LSB
Differential Non Linearity (DNL)	± 0.5 LSB
Conversion time	14 clock cycle
Capacitor	MIMCAP
Power	< 1mW (depends on frequency)
Trimming	Yes
Status (end of june)	First prototype submitted
Designer (Email)	menouni@cppm.in2p3.fr; awang@cppm.in2p3.fr; renaud.gaglione@lapp.in2p3.fr;

I/O signals	Function
Input signals (Vref, Vin, Ibias, clk, reset, enable)	
Output signals (out<11:0>, data_valid)	
VDDA	Analog supply
VDDD	Digital supply
GND	Ground

Block Diagram

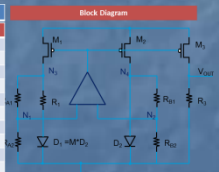


IP Block: Bandgap V1 Bipolar device

Parameter	Value
Supply voltage	Typ 1.2 V (±10%)
Temperature range	-40 °C to +60 °C
Active element	BJT_PNP10
Bandgap voltage output	400 mV – 600 mV – 800 mV
Temperature coefficient	400 ppm/°C max
Noise	20 μV RMS max
Max variation (PVT, mismatch)	< 4 mV
Power supply rejection	TBD
Consumption	500 μW (main stage)
Startup circuit	Yes
Trimming	Yes
Max variation (1Grad, 10^{15} n/cm²)	?
Status (end of june)	First prototype submitted
Designer (Email)	menouni@cppm.in2p3.fr; awang@cppm.in2p3.fr;

I/O signals	Function
Input signals (Signal name)	
Output signals (Signal name)	
BGP	Bandgap output
VDD	Supply voltage
GND	Ground

Block Diagram



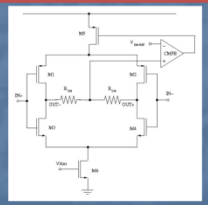
Schedule

Status	Date
Prototype 0 submitted	Q2 2014
	Q3 2014
First Tests and Irradiation	Q4 2014
Re-design, Improvement	Q4 2014
Prototype 1 submission	Q4 2014
Prototype characterized	Q1 2015
Prototype 2 submission	Q3 2015
Prototype 2 characterized	Q3 2015
Full IP available	Q4 2015

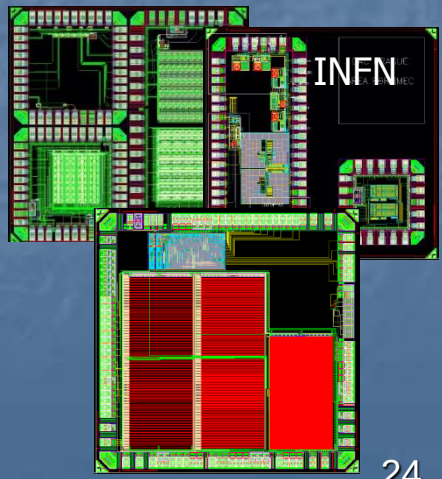
IP Block: BG-PV (low-medium speed) Scalable LVDS driver

Parameter	Value
Size	155μm X 165μm
Supply voltage	1.08-1.32V
Power	2.1 mW
Temperature range	-25°C +75°C
Frequency of operation	320 Mbps
Metal layers	M1-M2-M3
Special options	None
Capacitor	NMOS
Active element used	NMOS, PMOS, LVT_NMOS, LVT_PMOS, rpolywo, rnolywo
Status (date)	First prototype fabricated and ready to be characterized
Designer (Email)	gianluca.traversi@cern.ch francesco.de.canio@cern.ch

Block Diagram



I/O signals	Function
Input signals (Signal name)	IN
Output signals (Signal name)	OUT+, OUT-
VDD, GND	Supply voltage, ground

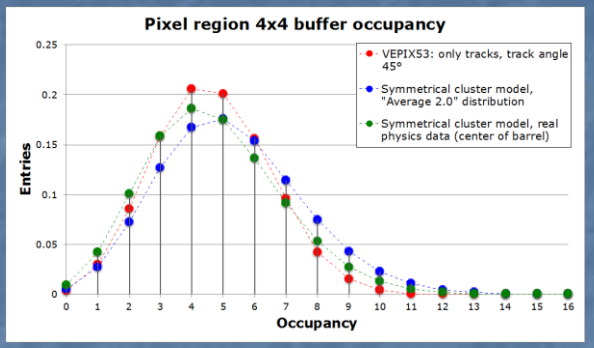


IP Schedule

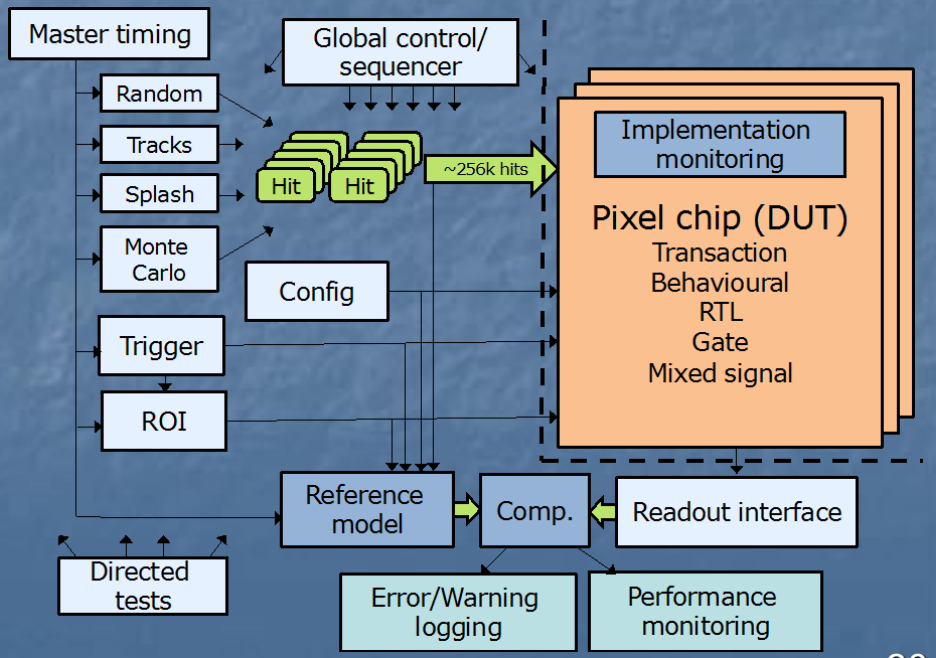
- ~2 years to make IPs.
  To have full pixel array ROC at end of 3 year RD53 program
  - Who makes what and how: Done
  - Specs of each IP: Done
  - Initial schematic/layout: Q4 2014 (90% done)
  - First Prototype: Q1 2015 (~50%)
  - Behavioural model Q2 2015 (to allow progress on global pixel)
  - Tested Prototype: Q3 2015
  - Radiation qualification: Q4 2015
  - (2nd. Prototype) Q4 2015 (shared MPW submission)
  - Final IP: Q1 2016
    - Long list of things to deliver for each IP

Simulation/verification WG

- Simulation and verification framework for complex pixel chips
- Convener: Tomasz Hemperek, Bonn
- Activities and status
  - Simulation framework based on system Verilog and UVM (industry standard for ASIC design and verification)
    - High abstraction level down to detailed gate/transistor level
    - Benchmarked using FEI4 design
  - Framework available on common repository
    - Internal generation of appropriate hit patterns
  - Study of buffering architectures in pixel array
  - Integration with ROOT to import hits from detector simulations and for monitoring and analysing results.
- Plans
  - Refine/finalize framework with detailed reference model of pixel chip
  - Import pixel hit patterns from detector Monte-Carlo simulation
  - Modelling of different pixel chip architectures and optimization
  - Verification of final pixel chip
- Bonn, CERN, Perugia



Buffer occupancy comparison between simulation and analytical statistical model



IO WG

- Defining and implementing readout and control interfaces
  - Common test interfaces and test hardware
- Convener: Roberto Beccherle, Pisa (recently started)
- Plans
  - Defining readout and control protocols
  - Implement/verify IO blocks for pixel chip
  - Standardized pixel test systems
- Pisa, Bonn , , ,

RD53 planning

- 2014:
  - Release of CERN 65nm design kit. (lots of delays encountered with legal NDA issues)
  - Detailed understanding of radiation effects in 65nm
    - Cold operation
    - Radiation test of few alternative technologies.
    - Spice models of transistors after radiation/annealing
  - IP/FE block responsibilities defined and first FE and IP designs/prototypes
  - Simulation framework with realistic hit generation and auto-verification.
- 2015:
  - Final versions of IP blocks and FEs: Tested prototypes, documentation, simulation, etc.
  - IO interface of pixel chip defined in detail
  - Global architecture defined and extensively simulated with MC hits
  - Initial small scale pixel array prototype
- 2016:
  - **Full sized pixel array demonstrator chip**.
  - Pixel chip tests, radiation tests, beam tests , ,
- 2017:
  - Separate or common ATLAS – CMS final pixel chip submissions.

Access to RD53 information

- Access to RD53 meetings and documents by default limited to RD53 members.
- Special "RD53 guests" category that can get full access to meetings and documents:
  - Members of ATLAS/CMS pixel upgrade projects
  - Institutes requesting to become active RD53 members.
  - CERN 65nm technology support
  - Others when well justified.

RD53 Summary

- RD53 has gotten a good start
  - Organization structure put in place
  - Technical work in WGs have started
  - Institutes has gotten some R&D funding because it is a common effort

  The development of such challenging pixel chips across a large community requires a significant organisation effort.
- Radiation tolerance of 65nm remains critical
  - Annealing effects/scenario to be better understood
  - Backup (baseline): Inner layer replacement versus alternative technology

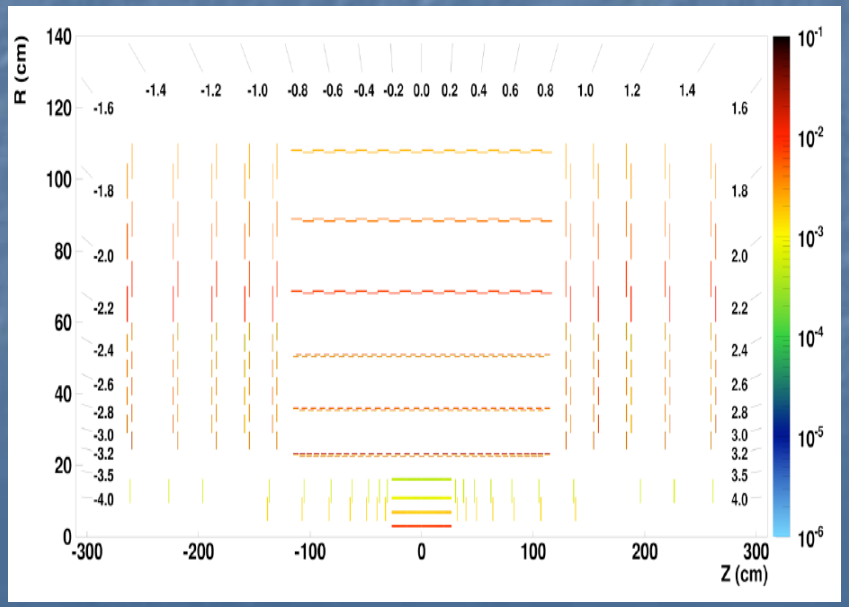
  1Grad radiation was completely unexplored territory and new effects have been seen.
- Prototypes of FEs and IPs made and under test
- Simulation framework available and being used for simulations with MC hits and optimization of final architecture
- Small scale pixel array prototype to be submitted before summer
- Full scale pixel chip demonstrator in 2016

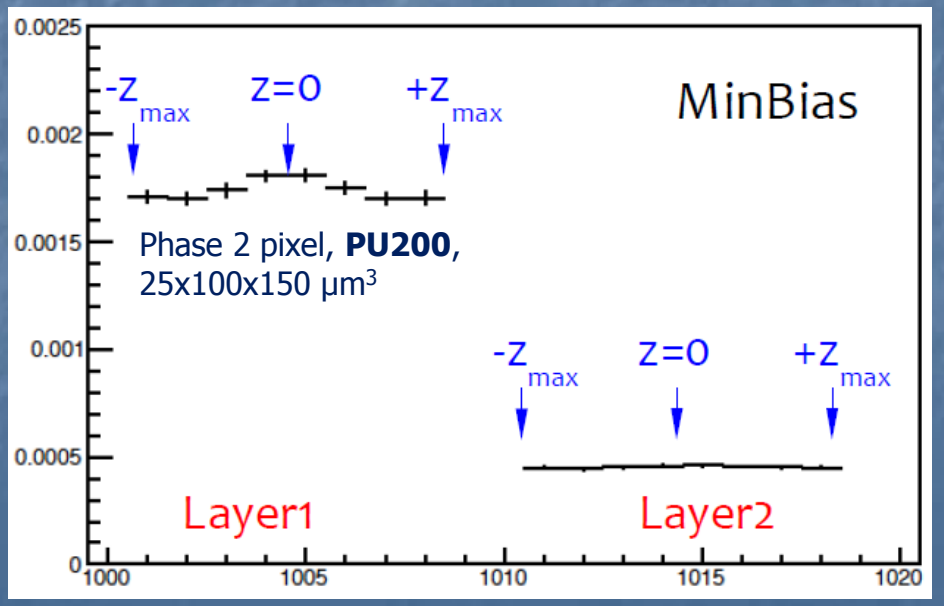
CMS and ATLAS relies on RD53 for their pixel upgrades

CMS PHASE 2 CASE

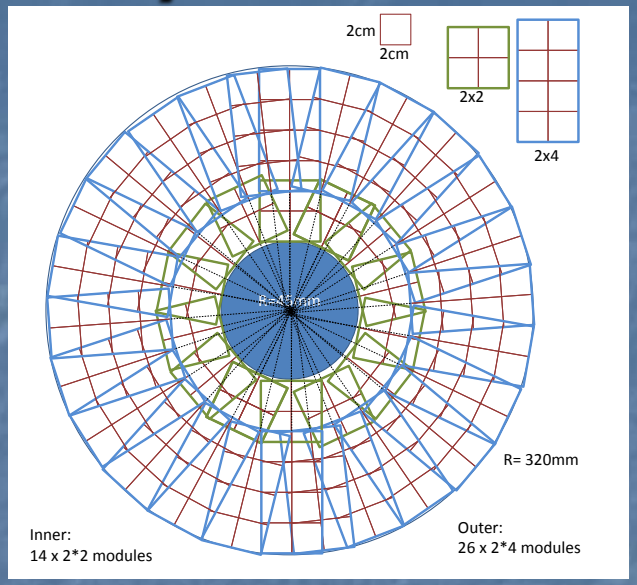
Rate estimates

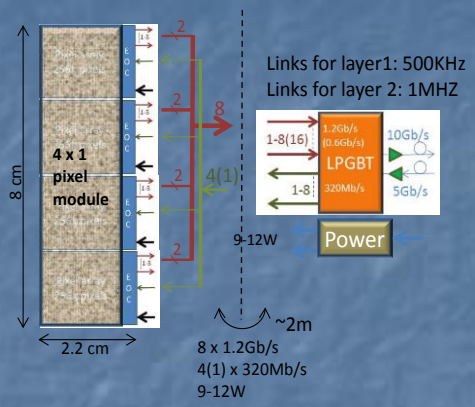
- Phase 2 MC with 25x100x150um^3 pixels
  - Hit rates inner layer: 2GHz/cm^2 (PU140) – 3GHz/cm^2 (PU200)
  - Rates relatively constant across barrel layer:
    - Middle: high track rate, small clusters
    - End barrel: lower track rate but much larger/longer clusters
  - Rate decreases factor ~2 for each barrel layer.

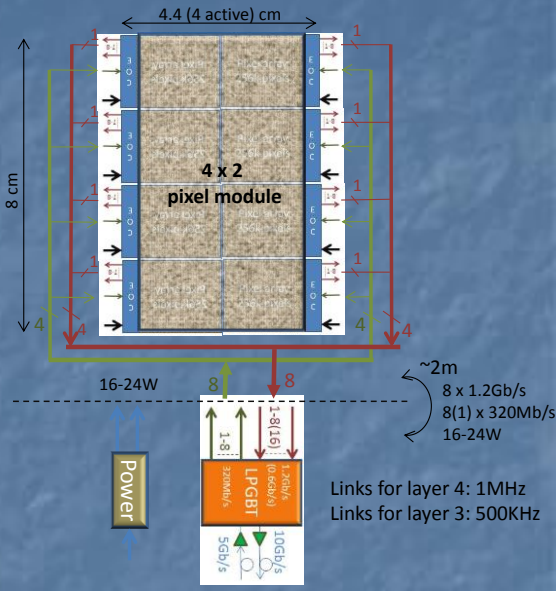


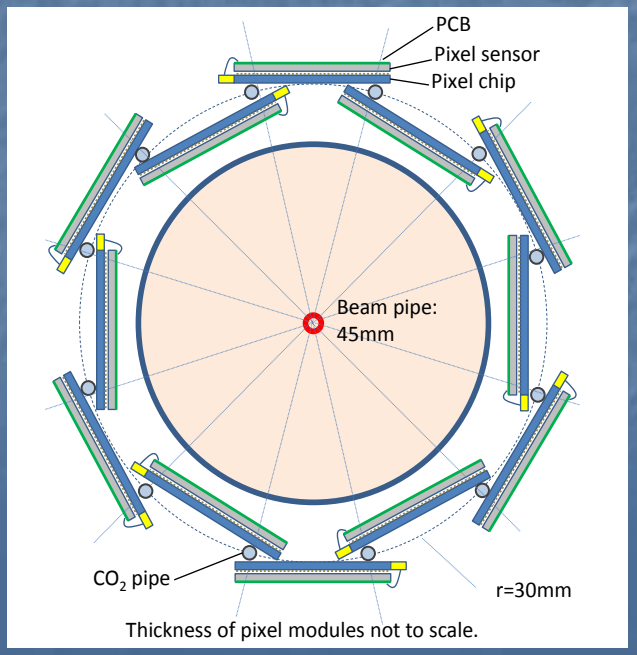


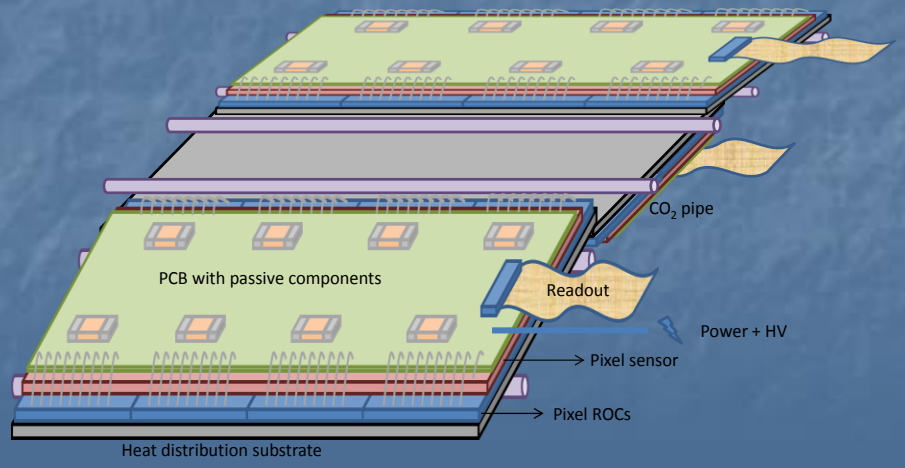
Layout sketches and modularity





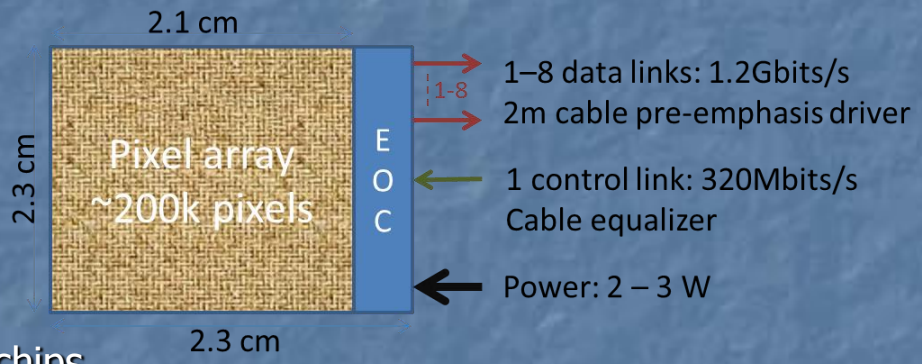


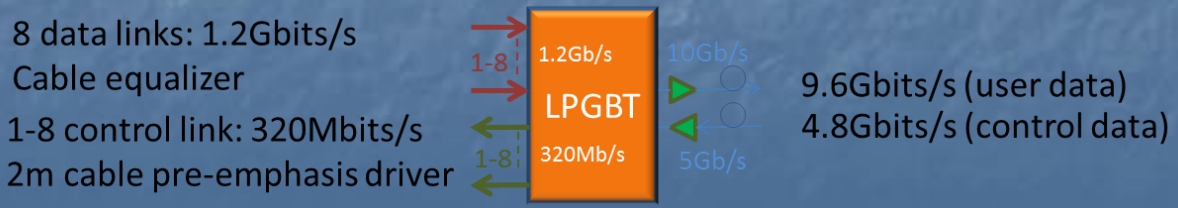




Pixel detector building blocks

- 1x4 pixel chip modules for Layer 1 & 2
- 2x4 pixel chip modules for Layer 3 & 4 and forward disks
- Electrical links: 1.2Gbits/s on capton flex, micro coax, twinax, **twisted pair**
  - Only point to point connections
  - Pre-emphasis drivers
  - Equalizer(filter) receivers
- Pixel chip:
  - 1-8 **1.2**Gbits/s data links
  - 1 320Mbits/s control/timing link
  - Capability to mux data from 2-4 chips
  - Power: ~0.5W/cm^2
- No module controller
- LPGBT:
  - 8 x 1.2Gbits/s data links = 10Gbits/s (user data !)
  - 8 x 320Mbits/s control/timing links = < 5Gbits/s down link (much less would be OK)

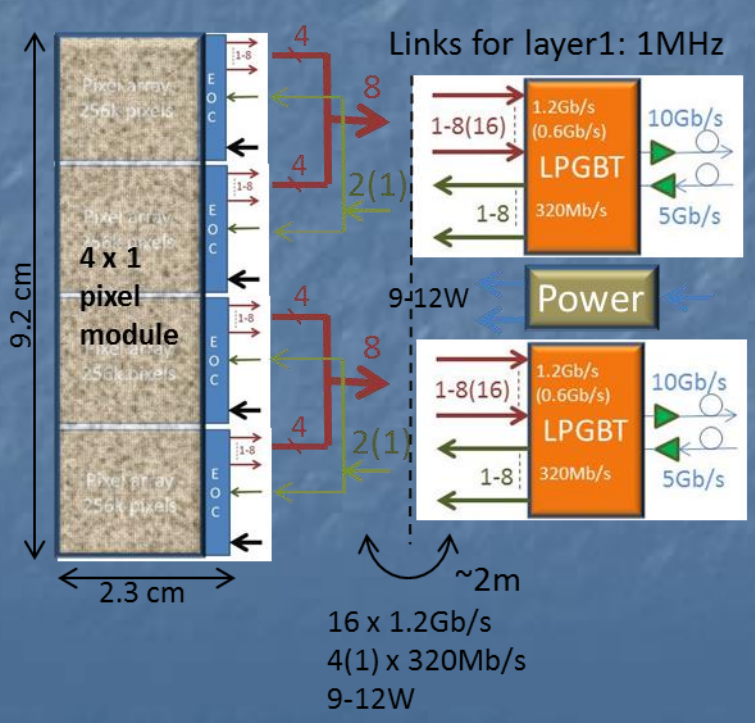


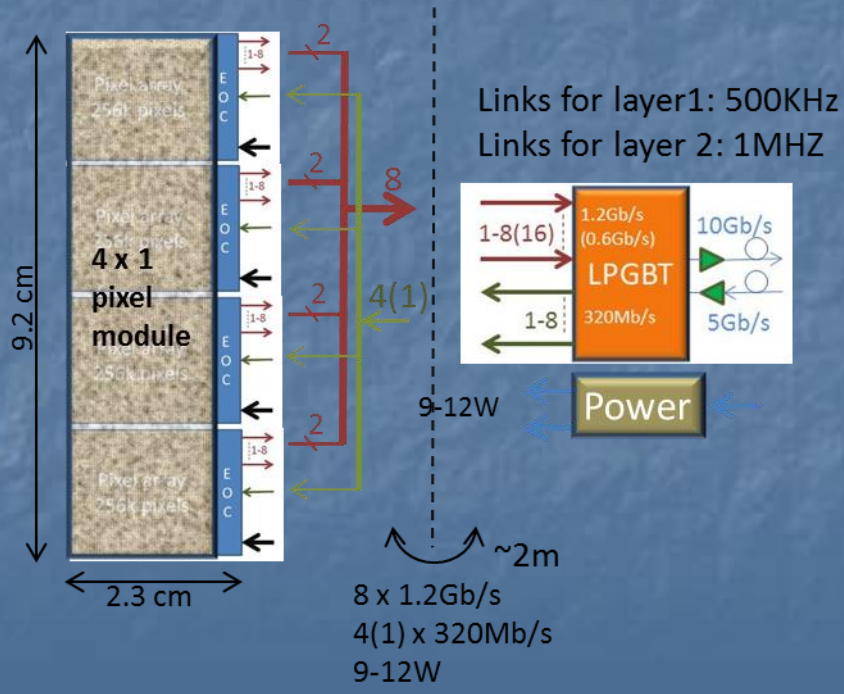


4x1 pixel module

- 4x1 pixel module for layer 1 & 2
- Different link configurations:

  Trigger: 1MHz (500kHZ)
  - Layer 1: 16(8) x 1.2Gbits/s E-links
  - Layer 2: 8(4) x 1.2Gbits/s E-links



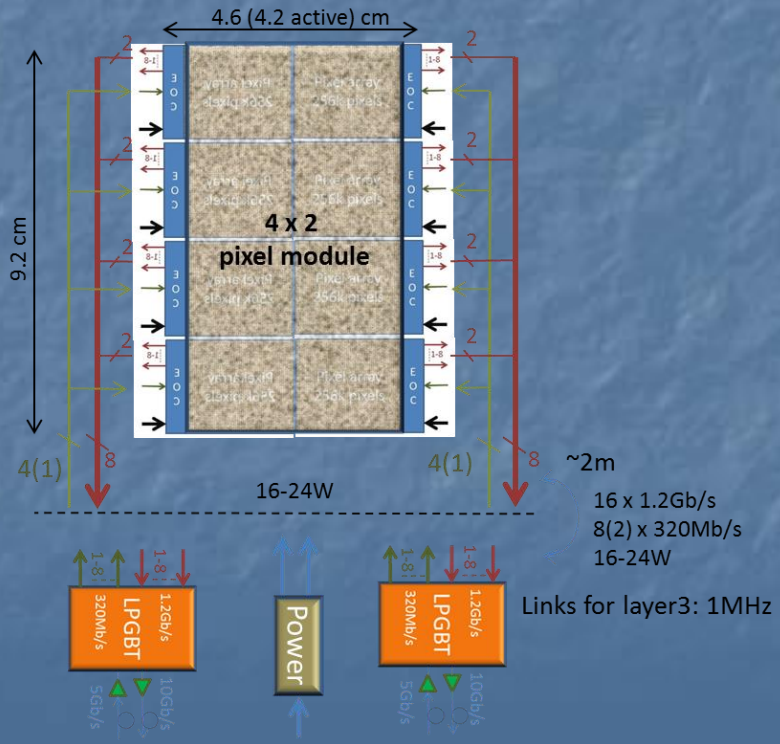


4 x 2 pixel module

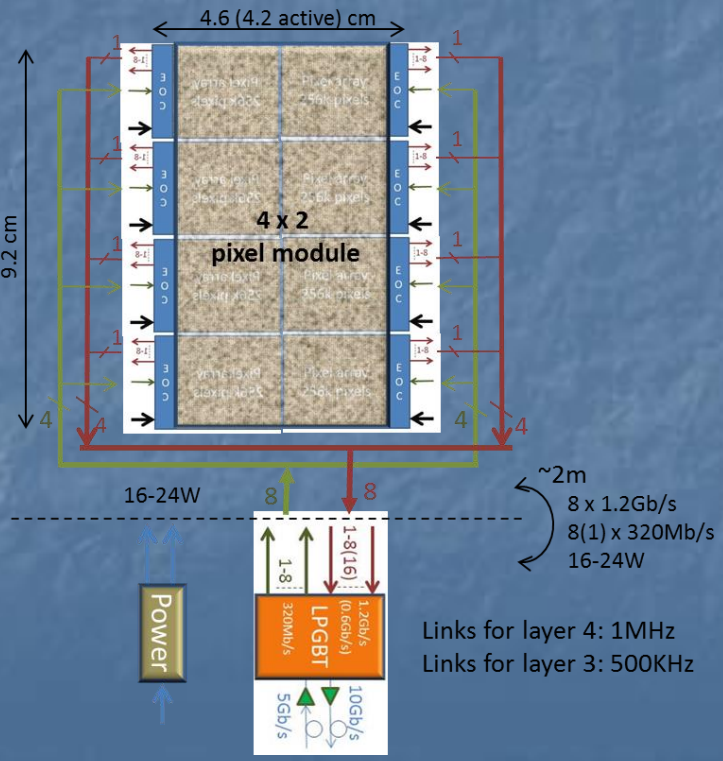
- 4x2 pixel module for layer 3 & 4 & endcap disks
- Different link configurations

  Trigger: 1MHz (500kHZ)
  - Layer 3: 16(8) x 1.2Gbits/s E-links
  - Layer 4: 8(4) x 1.2Gbits/s E-links

    On-chip data merging between 2-4 pixel chips for low rates



Links for layer3: 1MHz

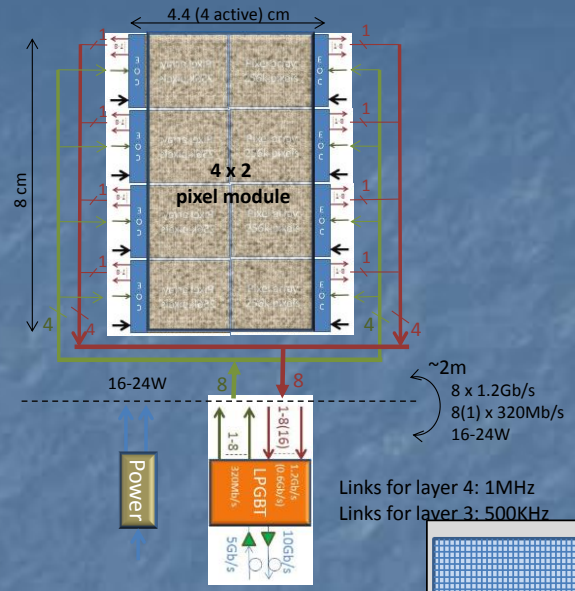


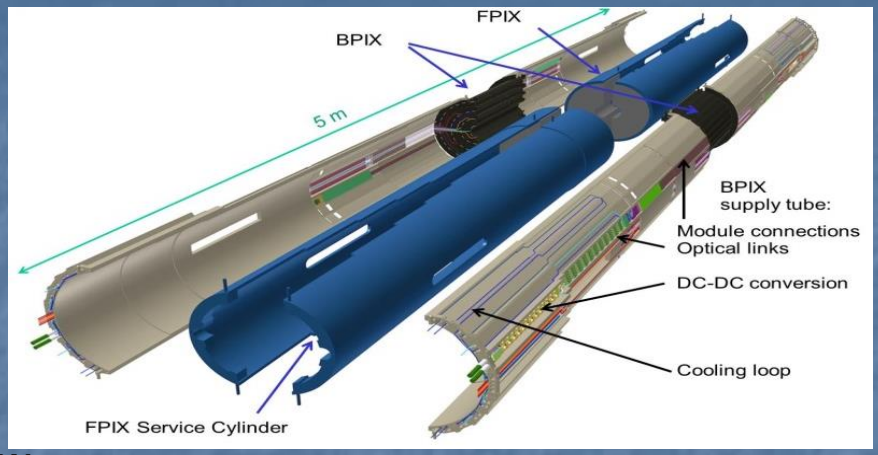
Links for layer 4: 1MHz
Links for layer 3: 500KHz

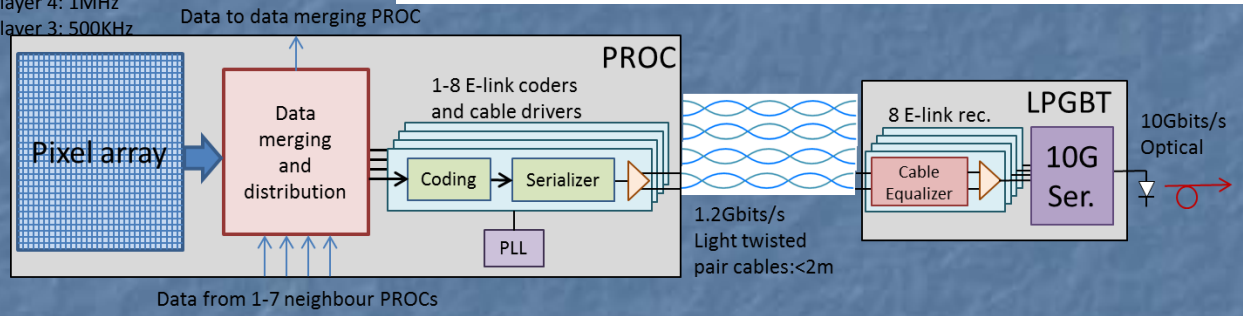
System summary

	Barrel L1	L2	L3	L4	Inner disks	Outer disks	Total
r (mm)	30	68	102	160	45 - 85	85-160	
Pixel size (um^2)	50x50	50x50	50x50	**100x100**	50x50	**100x100**	
Track rate: (relative)	500MHz/cm^2	1/4	1/8	1/16	1/5	1/10	
Hit rate: PU140: (PU200)	2GHz/cm^2 (3GHz/cm^2)	1/4	1/8	1/16	1/5	1/10	
Facets: Per ladder:	12 8	14 8	22 8	32 8	14	26	
Module size chips: mm:	1 x 4 20 x 80	2 x 4 40x80	2 x 4 40 x 80	2 x 4 40 x 80	2 x 2 40x40	2 x 4 40x80	
Disks					2 x 7	2 x 10	
Modules	96	112	176	256	196	520	**1356**
Chips	384	896	1408	2048	784	4160	**9680**
Hits per chip per Bx	200	50	25	13	40	20	
Event size per chip (bits)	4868	1264	664	364	1024	544	
Event size (KBytes)	228	138	114	91	98	276	**946**
Data rate per chip @ 500KHz trg. Gbits/s	2.43	0.63	0.33	0.18	0.51	0.27	
Data rate per module Gbits/s	**9.73**	**5.06**	**2.66**	**1.46**	**2.05**	**2.18**	
E-links per module @1.2Gbs/s	8 (16)	4 (8)	2 (4)	2 (4)	2 (4)	2 (4)	
E-links @ 1.2Gbs/s	768 (1536)	448 (896)	352 (704)	512 (1024)	392 (784)	1040 (2080)	**3512** (7024)

E-links







- Modest rate (1.2Gbits/s) serial to remote LPGBT
  - Rate that makes sense for input to LPGBT (10Gbits/s)
  - Speed could be seriously limited by radiation damage
  - Very low mass cable
  - 2x (4x) as option
  - Max 8 (4) per chip (high rate regions)
  - Data merging from max 8 pixel chips (low rate regions)
- 3500 (7000) links, 2m twisted pair or flex cable
  - 0.7 – 6 kg

100um sensors+100um pixel chips = ~2kg Si

Alternatives:

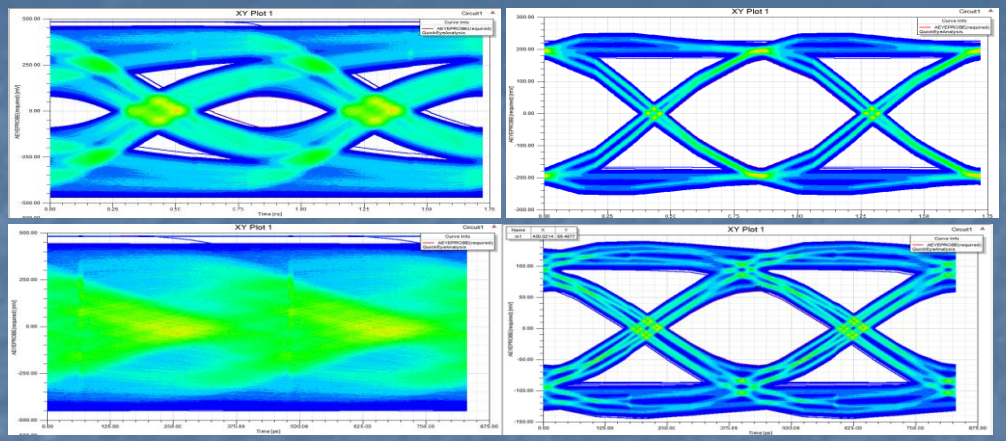
- Single High rate (4-6Gbits/s) electrical link per chip to remote laser
  - No use of LPGBT
- Opto conversion on pixel module
  - Outer modules with "low" radiation and low rates and less space constraints

E-link cable options

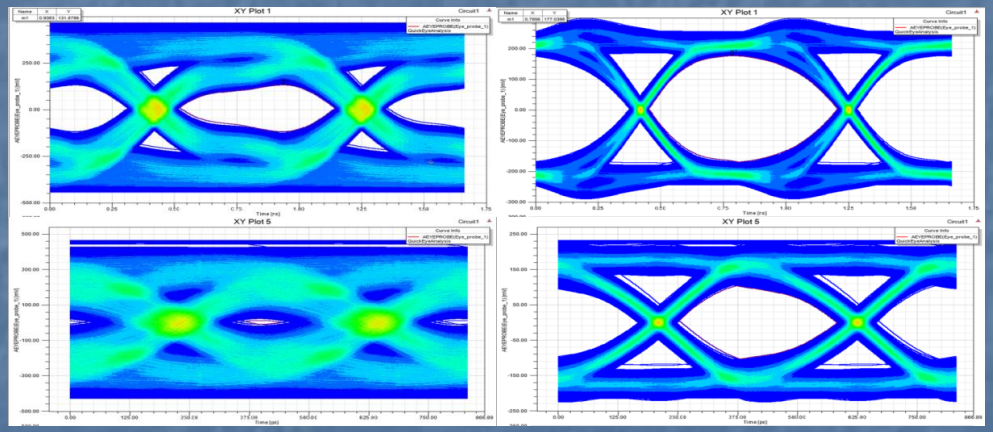
Cable option	Wire size, diameter	Wire resistance	Mass for ~3500 cables	% in signal pair	% in shield/ Gnd	% in insulator
36AWG Twisted pair, Cu, with shield	125um	2.7 ohm	**5.8 kg**	27%	40%	33%
36AWG copper pair, Cu, no shield	125um	2.7 ohm	3.5 kg	45%	-	55%
Twisted pair Cu with Polyimide insulation	125um	2.7 ohm	1.8 kg	92%	-	8%
Twisted pair, Cu cladded Alu, Polyimide insulation	125um Alu 5um Cu	4.0 ohm	**0.7 kg**	83%	-	17%
Kapton flat cable, Cu 35um gnd plane	140x35um^2	6.9 ohm	4.0 kg	15%	55%	20%
Kapton flat cable, Cu 10um gnd mesh	140x35um^2	6.9 ohm	1.5 kg	40%	10%	50%
Kapton flat cable, Alu 35um gnd plane	140x35um^2	11.5 ohm	2.0 kg	10%	33%	58%
Kapton flat cable, Alu 10um gnd mesh	140x35um^2	11.5 ohm	**1.0 kg**	20%	5%	75%

Cable simulation

- Simulation with ansys
- To be refined
  - Connectors
  - Detailed cable driver
  - Coupling to neighbours
- To be verified with cable measurements
- Verify cable insulation for radiation tolerance



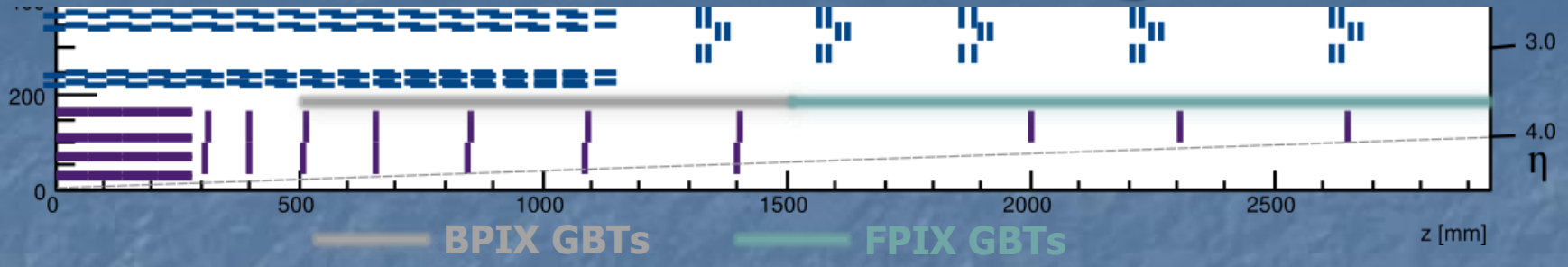
Signal eye diagram after 2m transmission on shielded twisted pair at 1.2Gbits/s (upper) and 2.4Gbits/s (lower) without (left) and with (right) driver pre-emphasis.



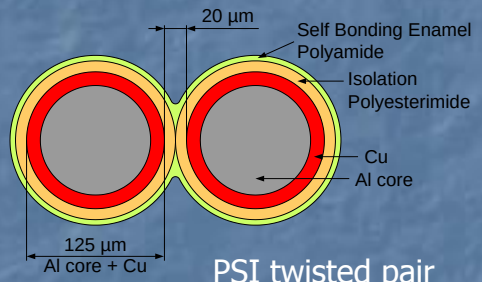
Signal eye diagrams after 2m transmission on Alu kapton flat cable at 1.2Gbits/s (upper) and 2.4Gbits/s (lower) without (left) and with (right) driver pre-emphasis

Mark Kovacs, PH-ESE

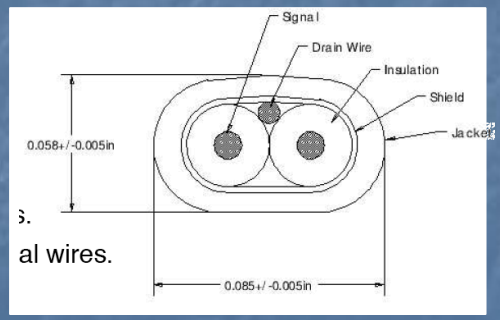
Readout cabling



- ~2m cabling from pixel module to LPGBT
  - Assume that LPGBT and opto can survive on service cylinder (100Mrad)
- Data rate: 1.2Gb/s (initial proposal/guess)
  - Appropriate interface to LPGBT
  - Optimal for minimal mass per Gbits/s ?
- Cable types:
  - PSI twisted pair: Cupper cladded aluminium, no shield
    - Phase1: 320Mb/s over 1m
    - Phase2: 1.2Gbits/s over 2m with active cable compensation ? Crosstalk ?
  - Habia UBT 3601 ST 2
  - Twinax cable: 4-6Gb/s over 4-6m



PSI twisted pair



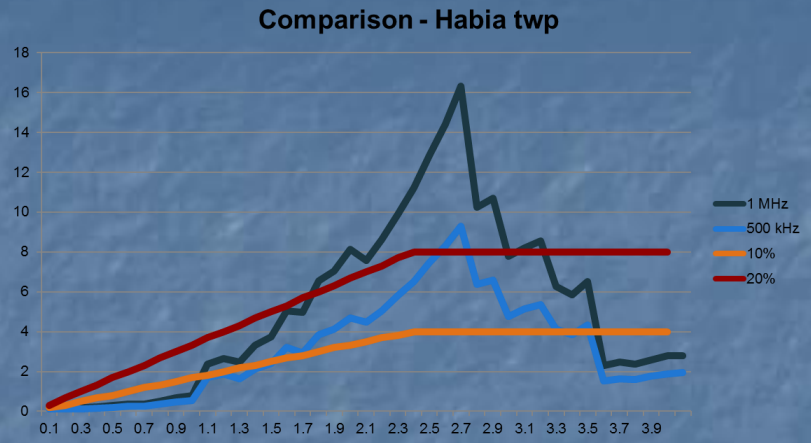
Twinax

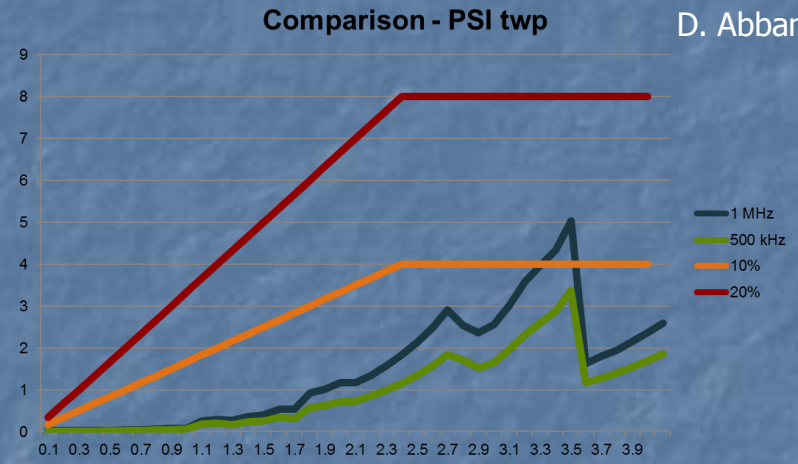
	Estimated mass in g/m		
	PSI	HABIA	TWINAX
Cu	0.027	0.339	0.083
Alu	0.058	0.330	1.390
Insulator	0.011	0.194	1.994
Total	**0.096**	**0.863**	**3.467**

D. Abbaneo

Material from readout cables

- PSI customized twisted
  - Acceptable material budget
  - Does it have the bandwidth ?
  - Very fragile
- Habia (commercial)
  - Has the bandwidth
  - Too heavy
- Solution: somewhere in between
  - Cu plated alu wire ?
  - Increased cross section ?
  - ALU shielding ?
  - Highly optimized cable driver receiver (cable equalization)
  - Dedicated study required !

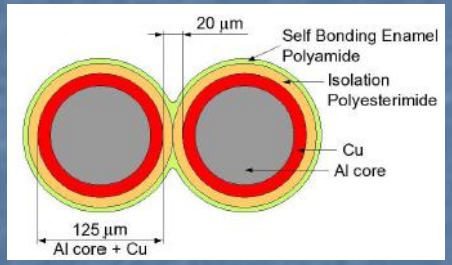




D. Abbaneo

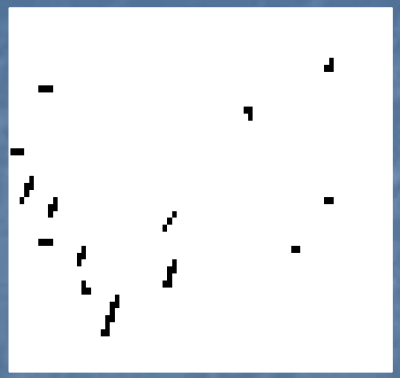
Pixel phase 2 spaghetti

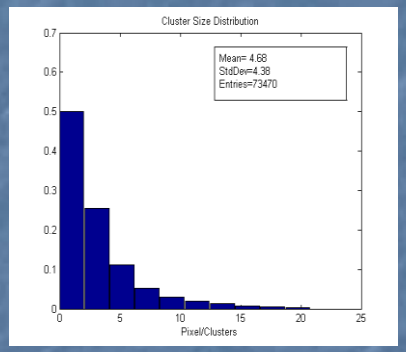
- Pixel detector: ~1000 modules
- Each module needs 8(16) – 2(4) 1.2Gbits/s E-links
- Needs ~5k electrical "low mass" links
  - What is a low mass electrical link ?.
    - Distance, Speed, Cable, Driver, Receiver, connector , ,
  - Routing/Installation ?
  - Material and physics impact ?
- Baseline: Low mass twisted pair as used in phase1
  - Needs to confirm that we can get 1.2Gbits/s on this with optimized drivers/receivers.
- How to improve:
  - Lowest possible trigger rate: 500KHz (1MHz)
  - Shortest possible distance
  - Confirmation of hit rates
  - On-chip track/cluster extraction: ½ ?
    - Local intelligence in very hostile radiation environment
  - Higher speed E-links: 2 – 10Gbits/s ?
    - How much "copper" needed for this ?
    - High speed circuits in extreme radiation environment ?.
    - E-links interface to LPGBT
  - Use of flex cables ?
  - Stave concept with integrated readout links ?
  - Opto on pixel module (Readout = VCSEL)
    - Can it survive radiation ?
    - Speed: 5 – 10Gbits/s ?
    - Power, compactness, ,
- And we still have to add power cabling !

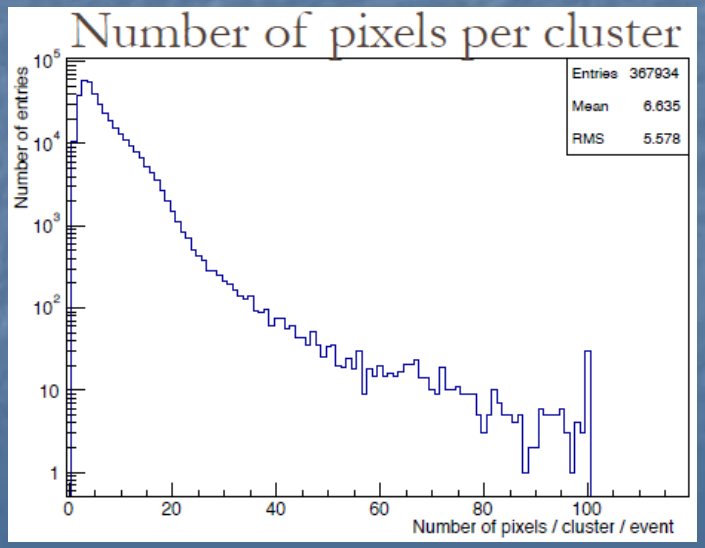


On-chip pixel "clustering"

- Pixel data clustering/formatting
  - Readout data reduction: Factor ~2
- Track position extraction
  - Readout data reduction: Factor ~3
  - Many questions/worries:
    - Effective resolution compared to off-line
    - Not having raw hit information for future improvements of resolution
    - Required hardware and timing







Pisa

Pixel chip power guesstimate

- High rate regions with 50x50um^2 pixels: Barrel L1
- Medium rate regions with 50x50um^2 pixels: Barrel L2, L3, Inner disks
- Low rate regions with 100x100um^2 pixels: Barrel L4, Outer disks

Pixel chip power: 2cm x 2cm	Conservative	Optimistic
Analog power supply	1.2v	
Pixel analog current (50x50um^2)	6uA per pixel	4uA per pixel
Pixel analog current (100x100um^2)	10uA per pixel	6uA per pixel
Digital power supply	0.8 (1.0) v	
Digital power density, low rate	0.2W/cm^2	0.1W/cm^2
Digital power density, medium rate	0.25W/cm^2	0.12W/cm^2
Digital power density, high rate	0.5W/cm^2	0.25W/cm^2
High rate pixel chip (50x50):		
Analog (1.2v) current per chip	0.96A	0.64A
Digital (0.8v) current per chip	2.50A	1.25A
Total chip power (high rate 50x50)	**3.15W**	**1.77W**
Medium rate pixel chip (50x50):		
Analog (1.2v) current per chip	0.96A	0.64A
Digital (0.8v) current per chip	1.25A	0.60A
Total chip power (med rate 50x50)	2.15W	1.25W
Low rate pixel chip (100x100):		
Analog (1.2v) current per chip	0.40A	0.24A
Digital (0.8v) current per chip	1.00A	0.50A
Total chip power (low rate 100x100)	**1.28W**	**0.69W**

Chip power density:
Conservative: 0.3 – 0.8 W/cm^2
Optimistic: 0.2 – 0.4 W/cm^2
(Current pixel: 0.2 -0.3 W/cm^2)

Pixel system power overview

Pixel module power	Conservative	Optimistic
L1 pixel module power (50x50um2, 4 chips)	12.6W	7.0W
L2 pixel module power (50x50um2, **8 chips**)	**17.2W**	**9.9W**
L3 pixel module power (50x50um2, 8 chips)	17.2W	9.9W
L4 pixel module power (100x100um2, 8 chips)	10.2W	5.5W
ID pixel module power (50x50um2, **4 chips**)	**8.6W**	**5.0W**
OD pixel module power (100x100um2, 8 chips)	10.2W	5.5W

Module power:

- Conservative: 9 – 17W
- Optimistic: 5 – 10W

(Module current = ~Module power)

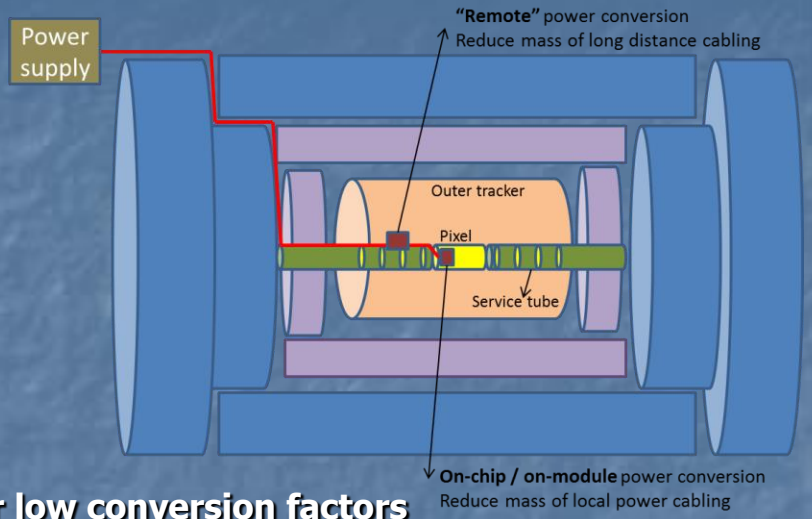
Total power:

- Conservative: 16kW
- Optimistic: 9kW

(Total current= ~9-16KA)

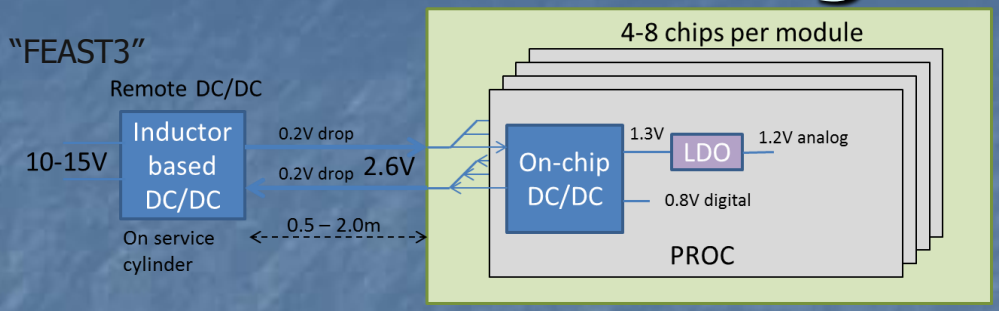
Pixel power overview	Conservative	Optimistic	Fraction power (%)	Fraction chips (%)
L1 (96 modules)	1210W	678W	7.7	4.0
L2 (112 modules)	1928W	1118W	12.2	9.3
L3 (176 modules)	3030W	1757W	19.2	14.5
L4 (256 modules)	2621W	1409W	16.6	21.2
ID (196 modules)	1687W	978W	10.7	8.1
OD (520 modules)	5324W	2862W	33.7	43.0
Total	**15801W**	**8803W**	100.0	100.0

Powering options



- **Direct from external PS: Excluded**
  - Huge power cables and huge power losses in cables
  - $\Omega = V_{drop}/I = L/A * \sigma$, $Mass = L*A*\rho$, Total voltage drop $= 2*V_{drop}$
  - $Mass = L^2 * I * \sigma * \rho / V_{drop}$ per wire (2 wires required)
  - Alu: $\sigma = 2.82 \times 10^{-8}\ \Omega*m$, $\rho = 2700 kg/m^3$
  - **Local power cabling** within acceptance: 1-2m (in practice more)
    - L=1m, V_{drop}=0.2V, I=16kA => Mass= **12kg**
    - L=2m, V_{drop}=0.2V, I=16kA => Mass= 48kg (L^2 dependency)
  - **Global power cabling**: 50m
    - L=50m, V_{drop}=1V (problematic !), I=16kA => Mass= 6100kg, 2/3 power lost in cables
- **One-stage on-chip/on-module DC/DC: Not attractive for low conversion factors**
  - On-chip power conversion ratio will be limited by technology and radiation: 2-4
    - Local 1m: 12kg/ 2-4 = 3-6kg
    - Local 2m: 48kg / 2-4 = 12-24kg
    - Global 50m: 6100kg/ 2-4 = 1500 – 3000kg
  - **If on-chip/on-module power conversion factor of 6-10 can be envisaged then this can be attractive**
- **One-stage remote DC/DC: Excluded**
  - Local power cables mass will be the same as "direct from external".
    - Local 1-2m power cabling: 12-48kg
    - Global power cabling: 6100kg / ~10 = 610kg
- **Two stage DC/DC (remote + on-chip): More detailed study**
- **Serial powering: More detailed study**
  - Cable mass reduced proportional to number of units put in series (e.g. 8)
  - Within pixel module or Across multiple pixel modules
- **Combination of serial and DC/DC: Exotic combination not yet considered**
  - Local serial powering from "remote" DC/DC converter with current output
  - Global serial powering with on-chip DC/DC
  - Complicated and no significant gain.

Two stage DC/DC



On-chip DC/DC: Switched capacitor
- Analog: Factor 2 + 0.1 V LDO
- Digital: Factor 3
  - Higher conversion factor (4-8) would be very advantageous but seems unrealistic

On-chip capacitors ?

Module current at 2.6V:
- Conservative: 4-8A
- Optimistic: 2-5A

(On-chip DC/DC: 90% efficiency)

On-chip DC/DC: Reduce mass of local power cabling

Remote DC/DC: Reduce mass of long distance power cabling
- Resolve over-voltage problems with dynamic load variations

Local power cabling mass

Voltage drop/ Distance	0.1v, 9kW	0.1v, 16kW	0.2v, 9kW	0.2v, 16kw	0.4v, 9kW	0.4v, 16kW
0.5m	1.5 kg	2.7 kg	0.75 kg	1.3 kg	0.37 kg	0.67 kg
1.0m	6.0 kg	11 kg	**3.0 kg**	**5.3 kg**	1.5 kg	2.7 kg
2.0m	24.0 kg	43 kg	**12 kg**	**21 kg**	6.0 kg	11 kg

Local power cable losses

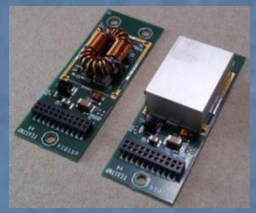
Voltage drop	Opt: 9kW	Con: 16kW
0.1v	780 W	1400 W
0.2v	**1570 W**	**2800 W**
0.4v	3140 W	5600 W

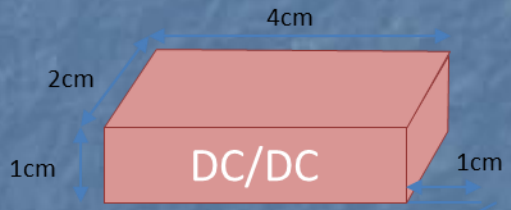
Dedicated cable cooling required ?

Integration of remote DC/DC

- Integration of remote DC/DC on service cylinder critical/difficult
  - Remote DC/DC as close to pixel modules as possible (move opto conversion further out)
  - Connectors for pixel detector insertion ?
  - Cooling, mechanics, etc.
  - Part of forward coverage

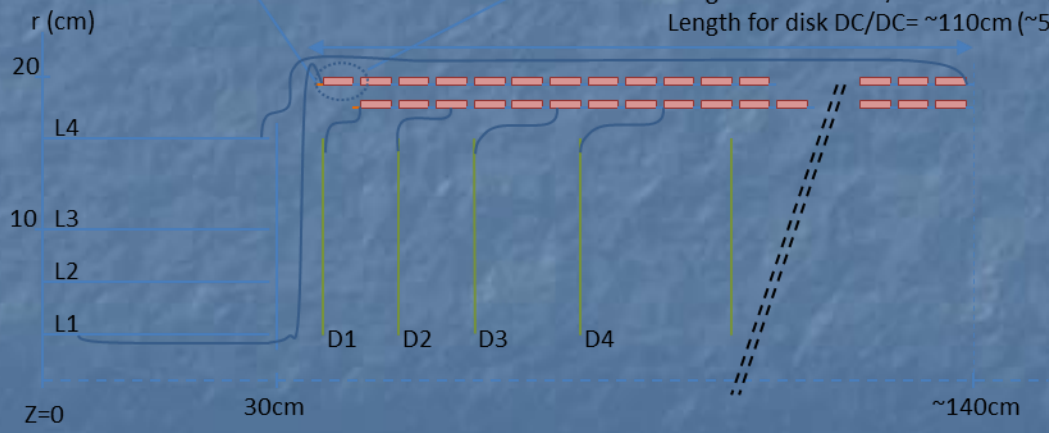
~1g for 4A converter:
Conservative: 2.8kg
Optimistic: 1.4kg

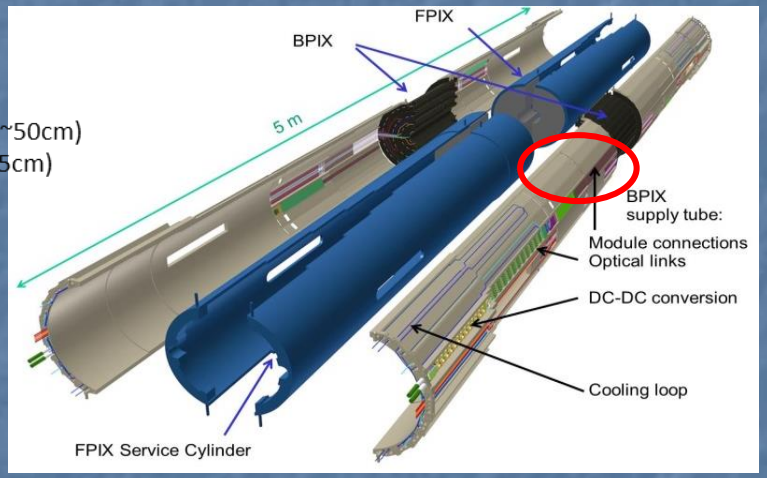




DC/DC filling in z = 0.8
DC/DC filling in Φ = 0.5

Length for barrel DC/DC = ~100cm (~50cm)
Length for disk DC/DC= ~110cm (~55cm)





Two stage DC/DC summary

Two stage DC/DC overview	Cons: 16kW	Opt: 9kW	Unit
Analog pixel chip voltage	1.2		V
Digital pixel chip voltage	0.8		V
Intermediate DC/DC voltage	2.6		V
Local power converter efficiency	0.9		
local analog DC/DC conversion ratio	**2**		
Analog LDO voltage drop	0.1		V
Local digital DC/DC conversion ratio	**3**		
Total pixel chip power	15802	8804	W
Power loss in local converters	2402	1391	W
Total power to local converters	18204	10194	W
Local power routing distance	**1.00**		m
Max voltage drop on power wire	**0.20**		V
Power loss in cables	**2801**	**1568**	W
Power delivered by remote DC/DC	21005	11763	W
Minimum module current (ID)	3.84	2.24	A
Minimum power wire diameter (ID)	0.83	0.63	mm
Max module current (L2, L3)	**7.69**	4.49	A
Max power wire diameter (L2,L3)	1.17	0.90	mm
Number of power cables (with 2 wires)	1356	1356	
Total power cable mass (Alu)	**5.33**	**2.99**	kg
Remote DC/DC mass	**2.8**	**1.4**	kg

Critical points:

- Remote DC/DC distance: <1m
  - Place for remote DC/DC + cooling on service cylinder
- 1Grad on-chip DC/DC realistic ?
  - Nobody working actively on this !
  - On-chip capacitors ?
  - Higher on-chip power conversion factor ?
- Remote DC/DC
  - Rad. Tol.: ~100Mrad, ~10^{15} neu/cm^2
  - Current rating: 4-5A (or 8A)
  - Can they be put in parallel ?.
  - 1g mass realistic ?
  - Synergy/same as for CMS OT ?.
- Cable cooling ?
- Overvoltage protection
  - Dynamic changes
  - Low power state
- Material in forward region within phase 2 coverage !.
  - 8(4)kg (cables + remote DC/DC)
  - Other material

Effective local cable reduction: 12kg/5.3kg= **2.2**
If including remote DC/DC mass this is reduced to 12kg/8kg =**1.5**
(determined by on-chip DC/DC conversion factor)

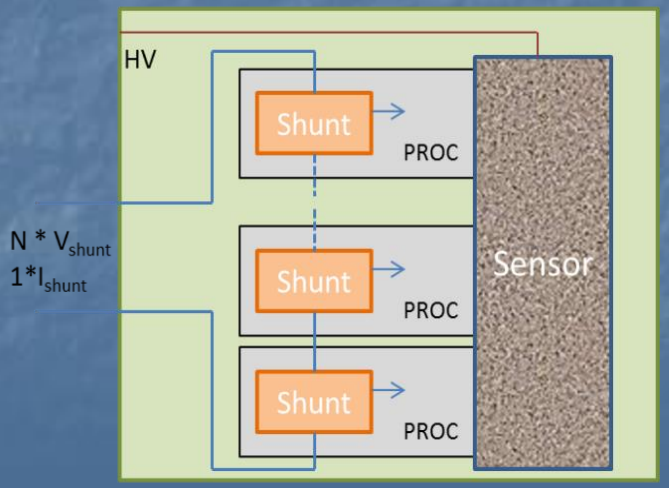
Serial power

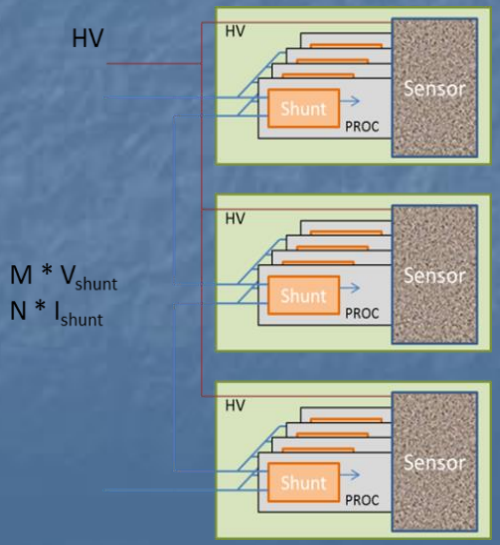
- Inject current and "develop/regulate" required voltage with local shunt regulator
  - Ensure to always inject enough current: ~10% more than max required
  - If chip burns less power during a time period this power will be burned by local shunt -> Constant current -> Constant voltage -> Constant power
    - Slow external control loop (software) to adjust injected current according to consumption

A. Between chips on same module
  - Good: No power chaining between modules (failure propagation)
  - Bad: Chips on same module at different potentials: comm., sensor interface (DC coupled)
    "Power conversion gain" limited by number of chips on module: 4 or 8

B. Between modules
  - Put local shunts in parallel. Requires specific Shunt-LDO that enables this.
  - Good: All chips on same module at same potential
    "Power conversion gain" can be increased by having many modules in power chain
    Current from failing shunt can be taken by 3(7) other shunts on module
  - Bad: Failure propagation across modules in power chain

Has been evaluated/tested by ATLAS pixel with FEI chips.
Favours a chain/stave structure with option to short circuit failing modules

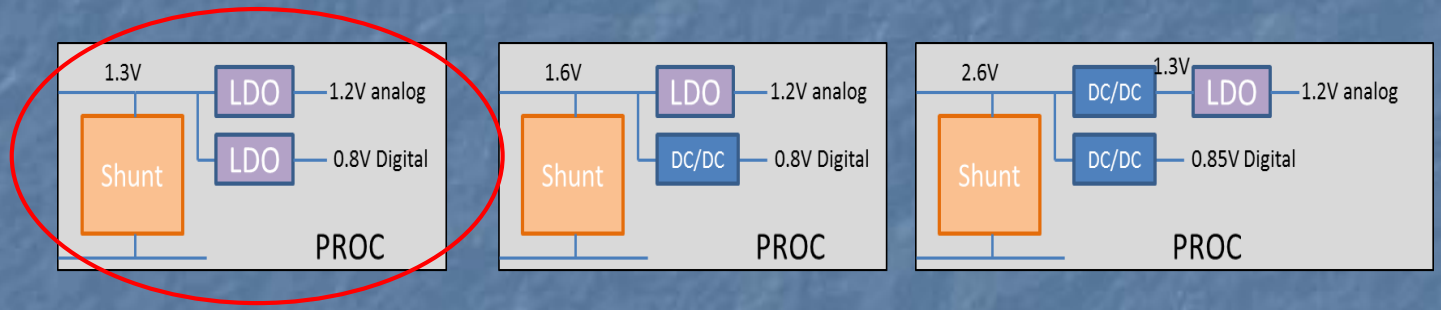




N: chips on module
M: modules in chain

Serial power shunt

- On-chip Shunt - LDO
  - Flexible design to allow:
    - Multiple chips in parallel
    - Multiple Shunt-LDOs per chip to generate multiple voltages (e.g. 1.2V, 0.8V)
  - Higher power loss (but still very attractive)
- On-chip shunt - DC/DC
  - Too complicated



Serial power across modules

Modules in series:
- Barrel: 8 (stave)
- ID: 7 (½ rings)
- OD: 8 (1/3 rings)

Effective local cable reduction:
12kg/1.74kg= **6.9**
(determined by number of modules in series)

Across-module Serial power overview	Con: 16kW	Opt: 9kW	unit
Local Shunt voltage	1.3		V
Analog pixel chip voltage	1.2		V
Digital pixel chip voltage	0.8		V
Total active pixel chip power	**15392**	**8584**	W
Analog LDO voltage drop	0.1		V
Digital LDO voltage drop	0.5		V
Total Power loss in LDO's	**5923**	**3002**	W
Excessive current fraction	0.10		
Total excessive current power	**2132**	**1159**	W
Total power to modules	**23447**	**12744**	W
Local power routing distance	1.00		m
Max voltage drop on power wire	0.20		V
Total power loss in 1m cables	**915**	498	W
Total power delivered	24362	13242	W
Power loops	**168**	**168**	
Total loops current (all)	**2289**	**1244**	A
Average loop current	**13.62**	**7.41**	A
Minimum loop current (Inner disk)	9.72	5.46	A
Minimum wire diameter	1.32	0.99	mm
Maximum loop current (L2, L3)	19.45	10.91	A
Maximum wire diameter	1.87	1.40	mm
Loop voltage (typical)	10.80	10.80	V
Local power cable weight (Alu)	**1.74**	**0.95**	kg

Serial power within modules

8 chip modules
- 88% of chips
- 82% of power

4 chip modules:
- 12% of chips
- 18% of power

Effective local cable reduction:
12kg/2.08kg= **5.8**
(determined by number chips per module)

If only 4 chip modules can be produced/used then power cabling mass will double: 4-2kg (Reduction = ~4)

In-module Serial power overview	Con: 16kW	Opt: 9kW	Unit
Local Shunt voltage	1.3		V
Analog pixel chip voltage	1.2		V
Digital pixel chip voltage	0.8		V
Total active pixel chip power	15802	8804	W
Analog LDO voltage drop	0.1		V
Digital LDO voltage drop	0.5		V
Total Power loss in LDO's	6096	3090	W
Excessive current fraction	0.10	0.10	
Total excessive current power	2190	1189	W
Total power to modules	24087	13083	W
Local power routing distance	1.00		m
Max voltage drop on power wire	0.20		V
Total power loss in cables	1095	597	W
Total power delivered	25182	13679	W
Power loops	**1356**		
Total loops current (all)	2737	1491	A
Average loop current	2.02	1.10	A
Minimum loop current (L4)	1.54	0.81	A
Minimum wire diameter	0.53	0.38	mm
Maximum loop current (L1)	3.81	2.08	A
Maximum wire diameter	0.66	0.49	mm
Loop voltage (typical)	10.40	10.40	V
Local power cable weight (Alu)	**2.08**	**1.14**	kg

Comparison

Power system	Two stage DC/DC		In-module Serial		Across-Module serial		Unit
Power scenario	Cons.	Opt.	Cons.	Opt.	Cons.	Opt.	
Active pixel chip power	15.8	8.8	15.8	8.8	15.8	8.8	kW
On-chip DC/DC, LDO	2.4	1.4	6.1	3.1	6.1	3.1	kW
Excessive power			2.2	1.2	2.2	1.2	kW
Total module power	**18.2**	**10.2**	**24.1**	**13.1**	**24.1**	**13.1**	kW
Power cable losses	**2.8**	**1.6**	1.1	0.6	**0.9**	**0.5**	kW
Total power	21.0	11.8	25.2	13.7	25.0	13.6	kW
Power cabling mass	**5.33**	**2.99**	**2.08**	**1.14**	**1.79**	**0.97**	kg
Power cabling in barrel	0.45	0.25	0.17	0.09	0.15	0.08	kg
Remote DC/DC mass	**2.8**	**1.4**					kg
Local cable reduction	**1.5 (2.2)**		**5.8 (4)**		**6.9**		

Same Basic assumptions:
- 1m local power cabling counted
- Max 0.2V voltage drop on 1m wire

Other materials:
- Chips + sensors: ~2kg
- Readout links: ~2-5kg
- Cooling, Mechanics, beam pipe: ?

- Serial power looks attractive
  - ~1/3 material in power cables
  - ~1/3 power losses in cables (less worries about cabling cooling)
  - No remote DC/DC with associated mass and integration problems
  - Smart Shunt – LDO currently under design in 65nm
  - Can possibly be even more advantageous:
    - Higher voltage drop on local power cables can possibly be supported.
    - When including the long distance power cabling of which some will be in forward acceptance
  - Major worries: Noise injection, Failure propagation, Grounding
    - R&D and extensive testing required

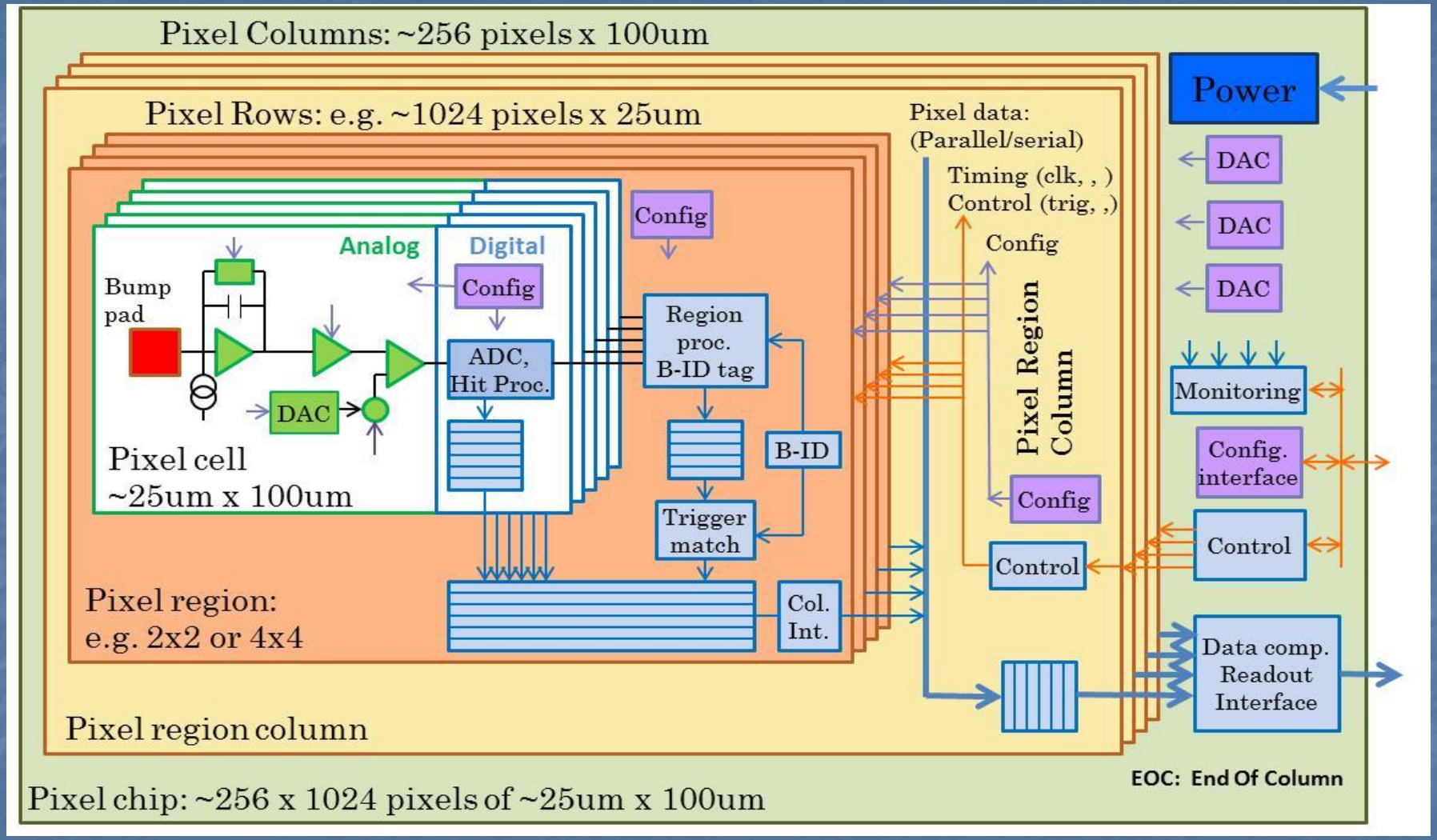
Advantages - Disadvantages

- **In-module serial powering**
  - **Advantages**: Low mass cabling (~2kg), Low power dissipation on power cables (~1kW), Individual module powering.
  - **Disadvantages**: High module power (~24kW). Different voltage potential of chips connected to same sensor. AC coupling required between chips on same module, Many (1300) power chains.
  - **Required R&D**: Development of shunt-LDO (RD53). **Verify if possible to have pixel chips at different potentials connected to one sensor**.
- **Across-module serial powering**
  - **Advantages**: Low mass cabling (~2kg), Low power dissipation on power cables (~1kW), Few (160) power chains, All chips connected to same sensor at same potential, On-module communication without AC coupling,
  - **Disadvantages**: High module power (~24kW). Failure propagation across modules.
  - **Required R&D**: Development of shunt-LDO (RD53). **Development of scheme/system to short circuit failing module ?.**
- **Two stage DC/DC**
  - **Advantages**: Individual module powering, Low power on module (18kW). No AC coupling required between pixel chips.
  - **Disadvantages**: High mass cabling (~5kg), Additional material (3kg) for remote DC/DC on service cylinder, High power losses on power cables (~3kW), Problem of available space on service cylinder for remote DC/DC converters.
  - **Required R&D**: **Development of rad hard on-chip DC/DC. Development of remote DC/DC. Detailed integration study of remote DC/DC on service cylinder.**
- **One-stage on-chip /on-module DC/DC:**
  - **Attractive if high conversion factor (6-10) can be obtained**

Any power system will need extensive test and verification

Buffer simulations

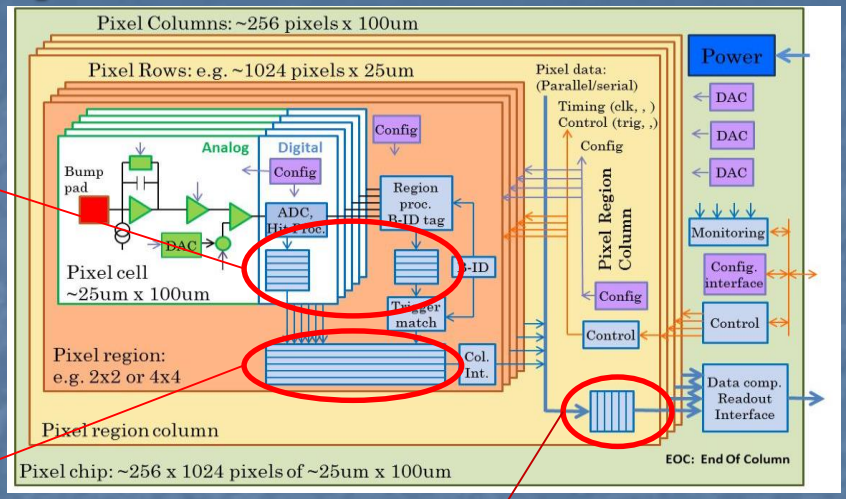
3rd generation pixel architecture



- 95% digital (as FEI4)
- Charge digitization (TOT or ADC)
- ~256k pixel channels per chip
- Pixel regions with buffering
- Data compression in End Of Column
- Chip size: >20 x 20 mm^2

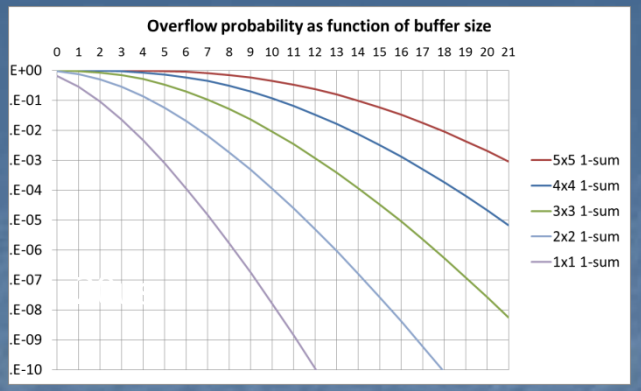
Buffering requirements

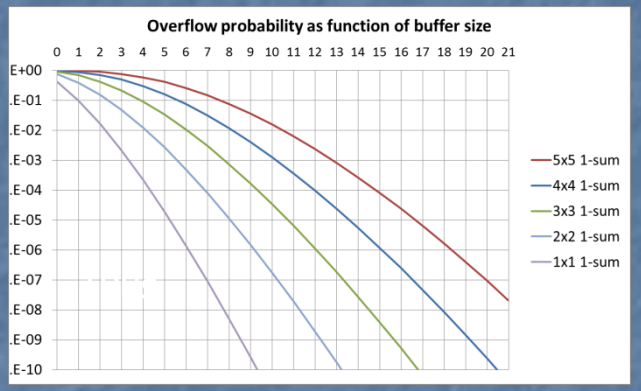
- Data buffering
  - A. **During trigger latency**
    - Location: Pixel region
    - Size: Hit rate, Trigger latency, PR organization/sharing, Data per hit (TOT/ADC, BX-ID, etc.)
    - Buffer type: FIFO
      - FIFO/RAM
      - Latches
    - Data buffer with individual counters
      - Registers + latches
  - B. To get data out of PR to EOC
    - Location: PR region
    - Size: Hit * Trigger rate * Data, Bandwidth to EOC, Sharing with other PR's
    - Buffer type: Small FIFO or back pressure to latency buffer
  - C. To assemble and compress all hits related to one event
    - FIFO buffer per pixel column to align event fragments
    - Buffers for compression/extraction ?.
    - Output FIFO
- Acceptable losses:
  - Hit loss:
    - Whish: <0.1%
    - Acceptable: <1%, in worst case locations ?.
  - Event loss: Never, as implies system de-sync.



Buffer depth

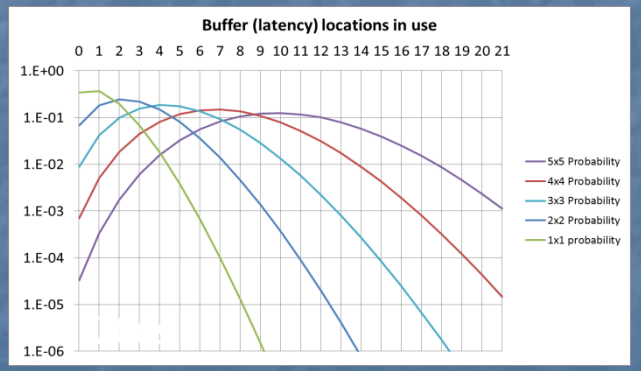
- Hits random in time: In 25ns BX
- Store hits during latency: 20us or10us (ATLAS 6us).
- Hit loss: 0.1% would be comfortable
  - 1% could possibly be acceptable in hottest regions. (especially if we really want to have small pixels)
- Buffer depth required per pixel region: Plots and Table
  - Does NOT scale linear !
- Buffer bits required per pixel is the real physical requirement
  - (10bit BX + N x 4 bit TOT/ADC)* Depth / N
- Conclusions
  - **Base line: 20us, 0.1%, 4 x 4: 16 buffers of 74bits = 1184bits**
  - Accept 1% loss: 2/16 = ~15% size reduction
  - Shorter latency: 10us, 0.1%: 5/16 = ~30% size reduction
  - **10us, 1% loss:** 8/16 = **~50% size reduction**
  - 2x2 instead of 4x4: ~25% reduction in number of bits (but not in area)

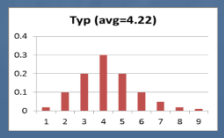




Required buffer locations (Bits/pixel)

	20us, 1%	20us, 0.1%	10us, 1%	10us, 0.1%
1x1	4 (56)	5 (70)	3 (42)	4 (56)
2x2	7 (45)	9 (59)	5 (33)	6 (39)
3x3	10 (51)	12 (61)	6 (31)	8 (41)
4x4	14 (65)	**16 (74)**	8 (37)	11 (51)
5x5	18 (79)	21 (92)	11 (48)	13 (57)





Physical buffer size: PR 4x4

- 16 words x 74bits = 1184 bits
- 4x4 pixel region:
  - Total area: ~25um x 100um x 16 = 40.000um^2
  - Digital: ~1/2 = 20.000um^2
- Total memory size (with guessed overhead):
  - Standard RAM: 1.05x0.5um^2 x1184 = 621um^2 x 1.25 = 777um^2
  - **Rad tol. RAM: 1.5x2.6 um^2 x1184 = 4617um^2 x 1.25 = 5771um^2**
  - Latches: 1.8x3.8 um^2 x1184 = 8099um^2 x 1.5 = 12147um^2
    - A 16x74 memory with minimum latches has been implemented in 7136 um^2 (Half size than conservative guess !, comparable to rad hard RAM)) Thanks to S. Bonacini
- Percentage of digital area used for latency buffer
  - Standard RAM: 4% Not rad hard
  - **Rad tol. RAM: 29% OK, Overhead TBC**
  - Latches: 60% Too large
    - **Mini latches 35% Would be OK, Rad tol ?**

Physical buffer size: PR 2x2

- 9words x 26bits = 234 bits
- 2x2 pixel region
  - Total area: ~25um x 100um x 4 = 10.000um^2
  - Digital: ~1/2 = 5.000um^2
- Total memory size (with guessed overhead):
  - Standard RAM: 1.05x0.5um^2 x 234 = 123um^2 x 1.25 = 154um^2
  - Rad tol. RAM: 1.5x2.6 um^2 x 234 = 913um^2 x 1.25 = 1140um^2
  - Latches: 1.8x3.8 um^2 x 234 = 1628um^2 x 1.5 = 2400um^2
- Percentage of digital area used for latency buffer
  - Standard RAM: 3% Not rad hard
  - Rad tol. RAM: 23% Overhead largely underestimated ?
  - Latches: 50% Could be OK,
    - Mini latches **27%** **Looks promising, Rad tol ?**

Physical buffer size: PR 1x1

- 5words x14bits = 70 bits
  - **Impractical small RAM (use latches)**
- 1x1 pixel region
  - Total area: ~25um x 100um = 2500um^2
  - Digital: ~1/2 = 1250um^2
- Total memory size (with guessed overhead):
  - Standard RAM: 1.05x0.5um^2 x70 = 37um^2 x 1.25 = 50um^2
  - Rad tol. RAM: 1.5x2.6 um^2 x 70 = 273um^2 x 1.25 = 340um^2
  - Latches: 1.8x3.8 um^2 x 70 = 478 um^2 x 1.5 = 720um^2
- Percentage of digital area used for latency buffer
  - Standard RAM: 4% Not rad hard
  - Rad tol. RAM: 27% Overhead largely underestimated
  - Latches: 58% Large !
    - Mini latches ~35% Could be OK, Rad tol. ?

Latency and buffer conclusions

- 20us latency buffer, <0.1% loss, seems feasible for a 25um x 100um pixel size
  - ½ area assigned to analog front-end.
  - ½ area assigned to digital:
    - Buffer shared across pixels in pixel regions
    - **4x4 PR: ~30% of dig. area needed for 16 buffer Rad RAM**
    - 2x2 PR: <50% of dig. area needed for latches
    - 1x1 PR: <60% of dig. area needed for latches
- 10us latency: ~30% memory reduction
- Accept 1% loss: ~15% memory reduction
- 10us, <1% loss: ~50% memory reduction.
- Based on conservative assumptions (inner layer):
  - Track/particle rate: 500MHz/cm^2
  - Cluster size: ~4 (middle barrel)
- What if Cluster size ~2x (~4GHz/cm^2):
  - Loss < 1%, Acceptable for small high rate regions

Details of rad hard RAM/latch to be confirmed:

- Area overhead for small memories
- Radiation tolerance to 1Grad.