The LHCb VELO Upgrade

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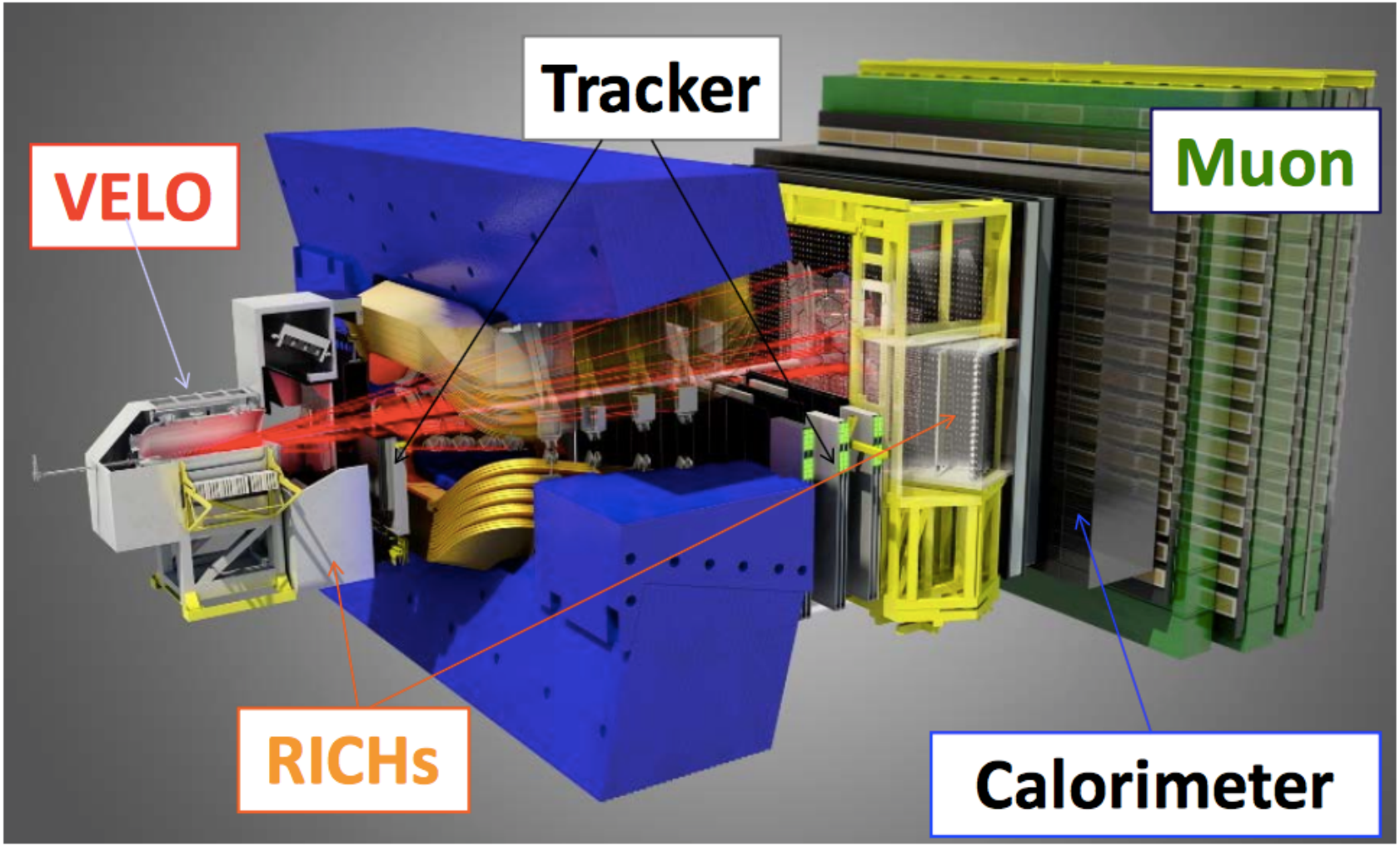
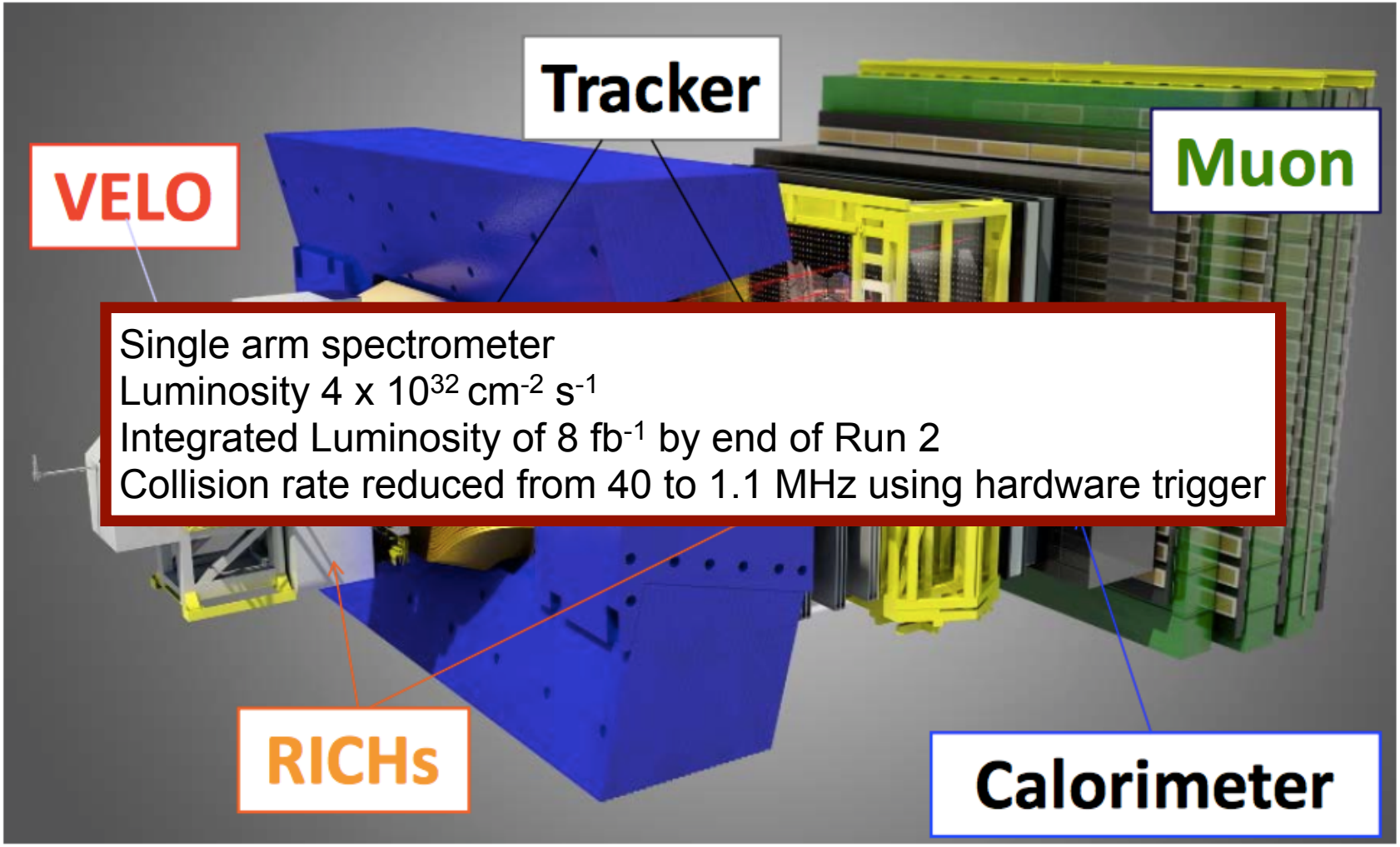
INFIERI workshop: 28th April 2015

The LHCb Experiment



The LHCb Experiment



Single arm spectrometer
Luminosity 4 x 10^{32} cm^{-2} s^{-1}
Integrated Luminosity of 8 fb^{-1} by end of Run 2
Collision rate reduced from 40 to 1.1 MHz using hardware trigger

Why Upgrade?

No evidence for New Physics in LHC Run 1

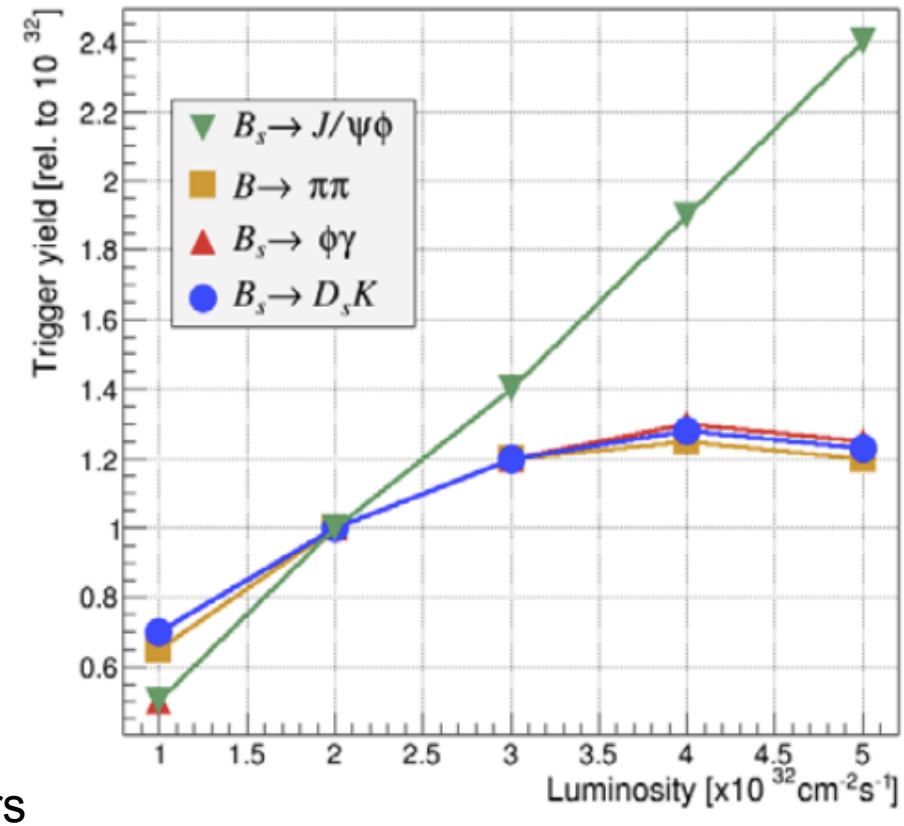
- Need x10 more data
- Need to increase luminosity from $4x10^{32}$ to $2x10^{33}cm^{-2}s^{-1}$

but….

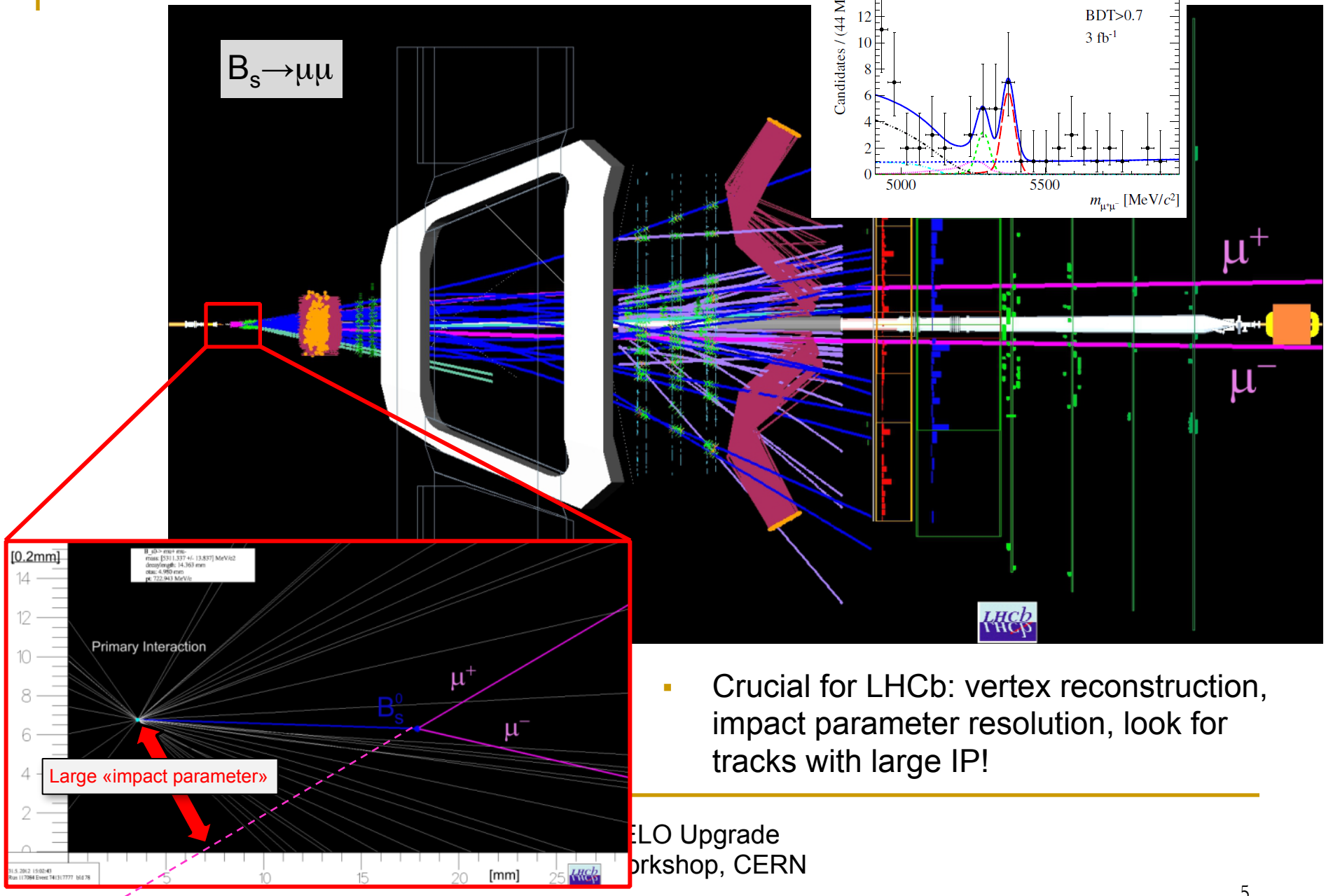
With 1 MHz limit we can't do this!

- Increase lumi -> raise Pt thresholds
- Trigger yield of hadronic events saturates

No gain … unless we eliminate trigger completely and upgrade all subdetectors to readout experiment at 40 MHz!!

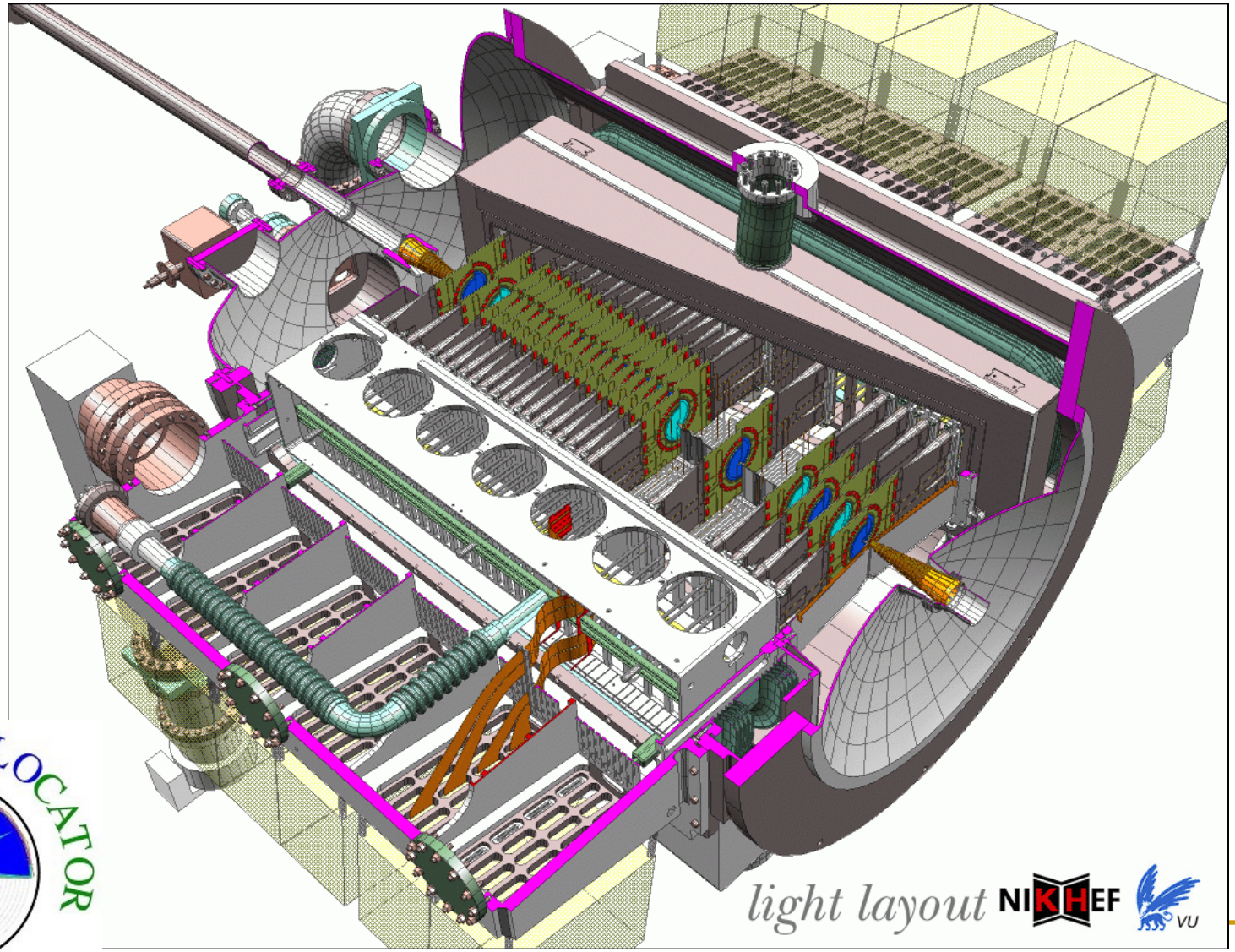


Role of the VELO

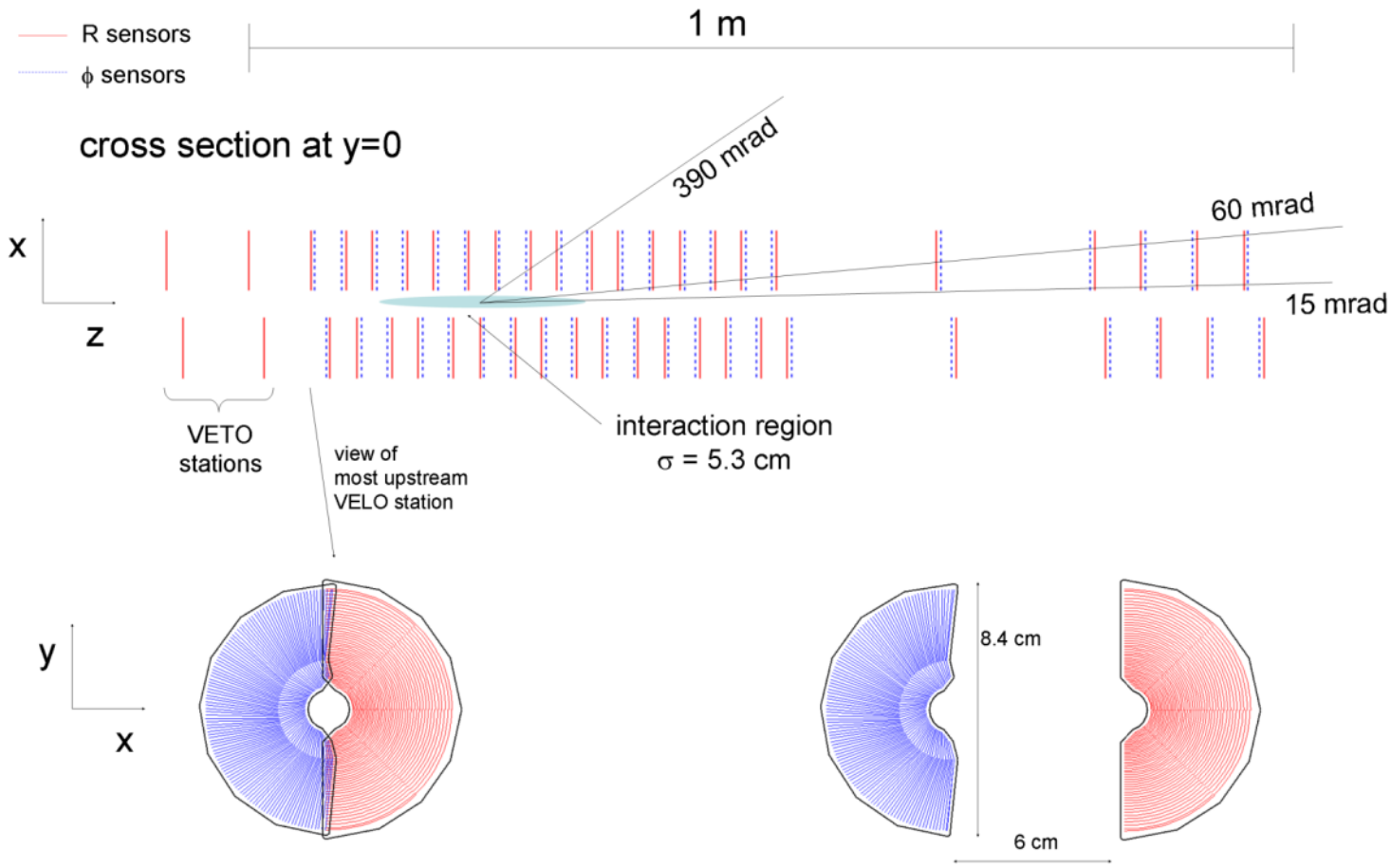


- Crucial for LHCb: vertex reconstruction, impact parameter resolution, look for tracks with large IP!

Current Vertex Locator (VELO)



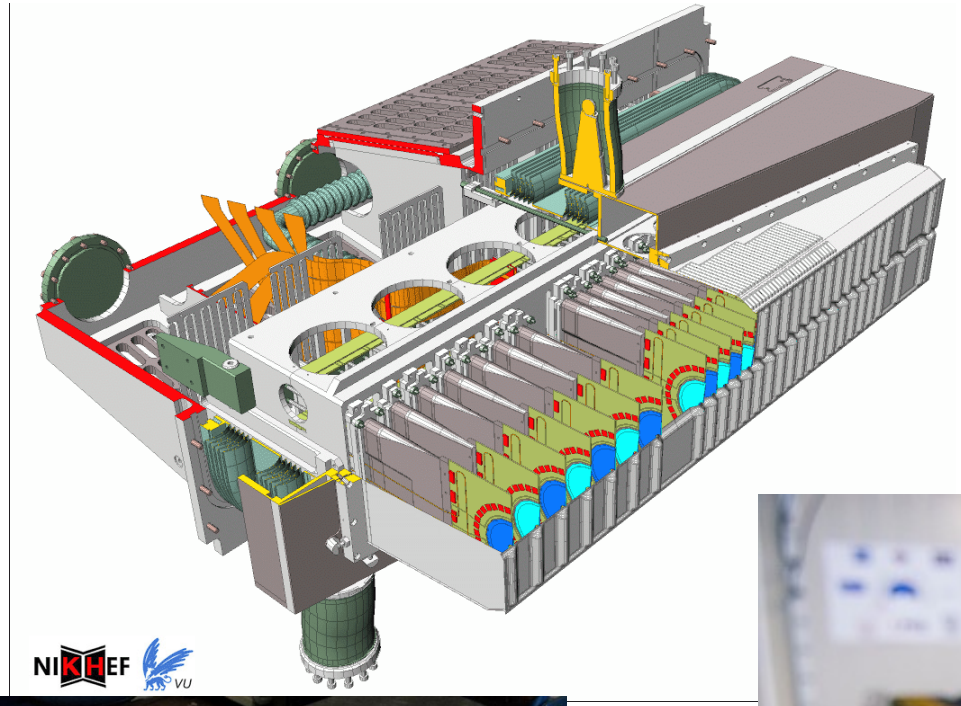
Current VELO layout



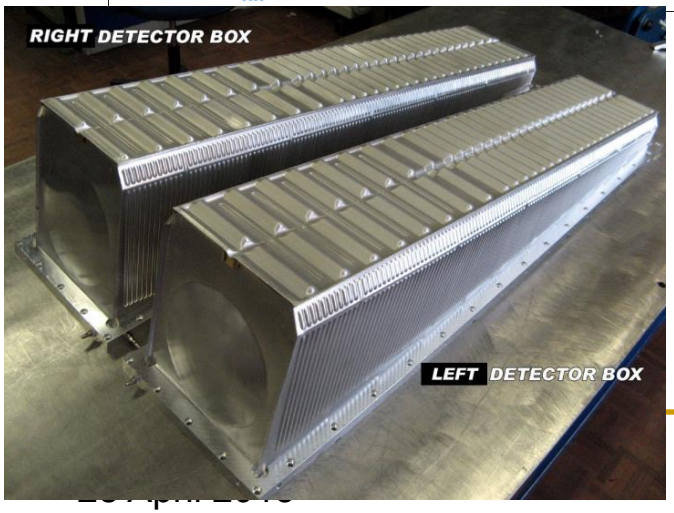
VELO fully closed (stable beam)

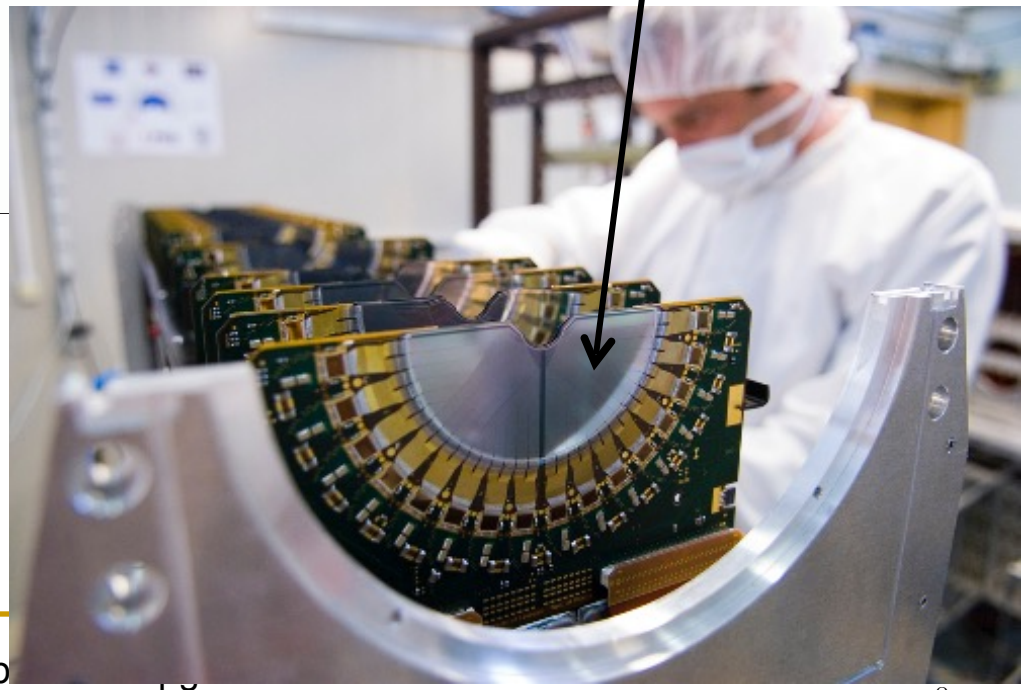
VELO fully open

Current VELO half with silicon detectors



- Silicon microstrip sensors

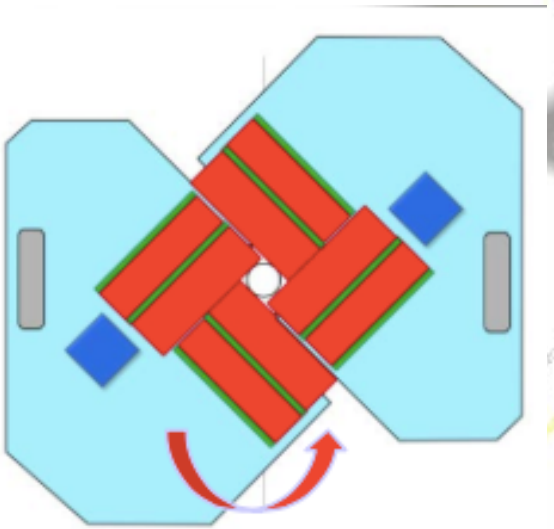


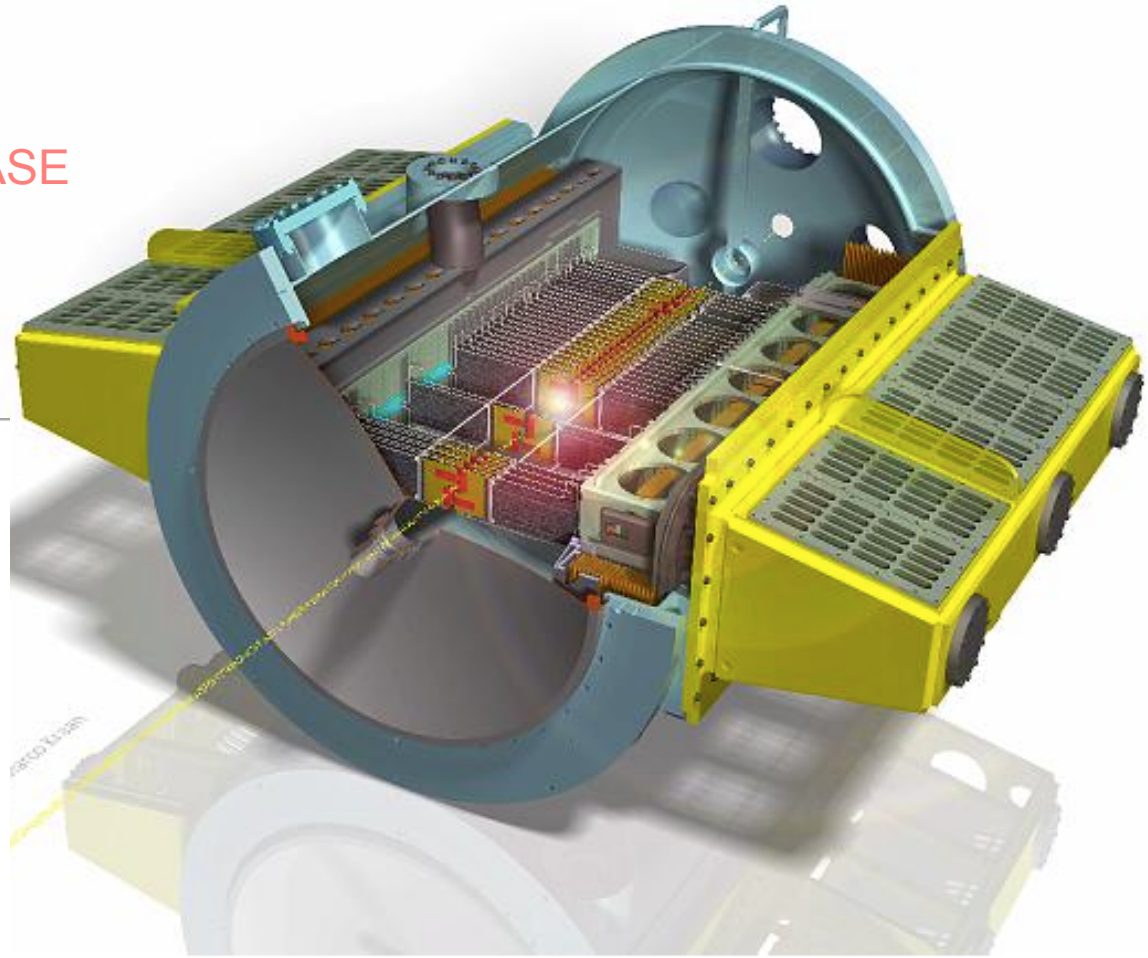


Challenges for Upgraded VELO

Function of VELO remains: provide precise tracking and trigger on displaced vertices.
Conditions more challenging: increased occupancies, data rates and radiation damage.

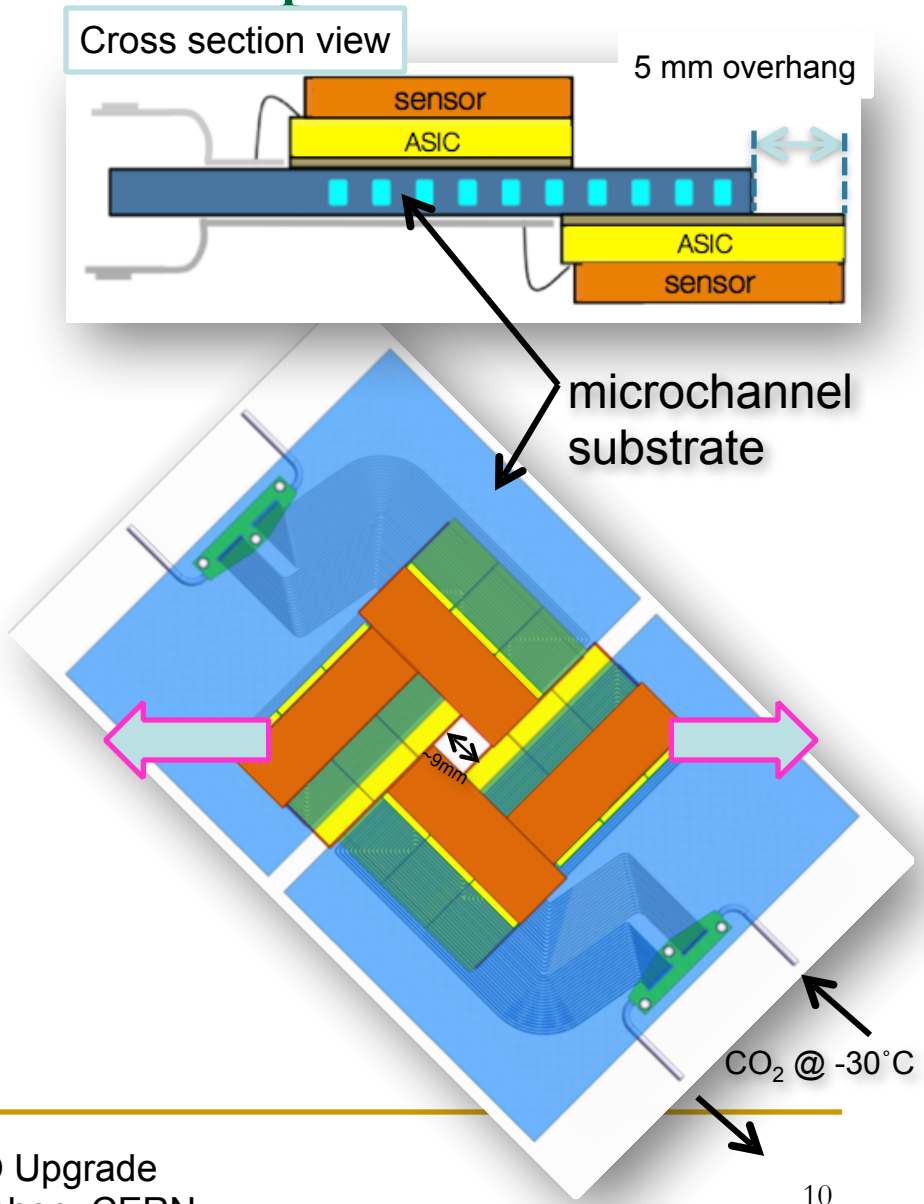
Choice made for
new PIXEL detector
equipped with TWO PHASE
CO_2 MICROCHANNEL
cooling





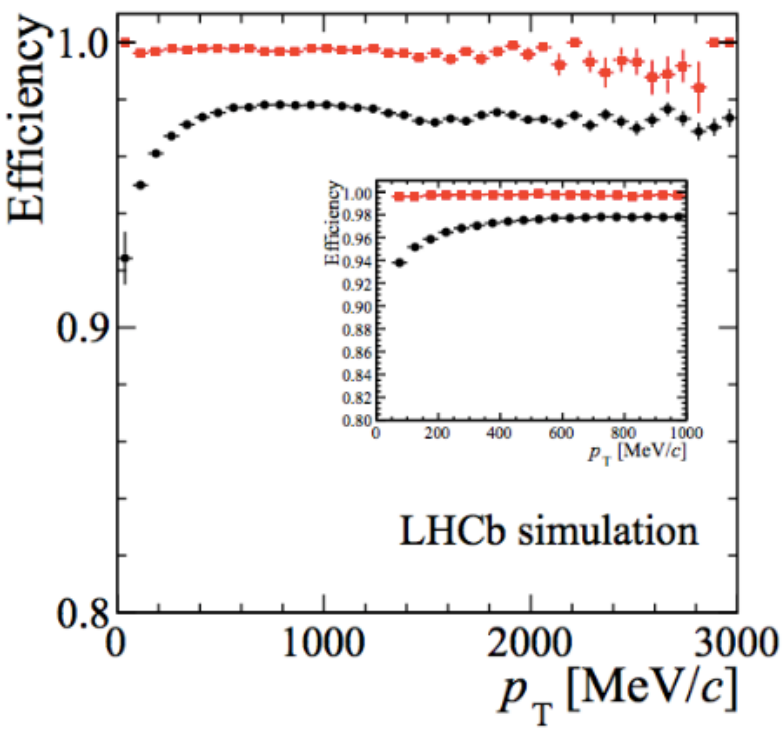
Upgrade VELO modules: pixel sensor

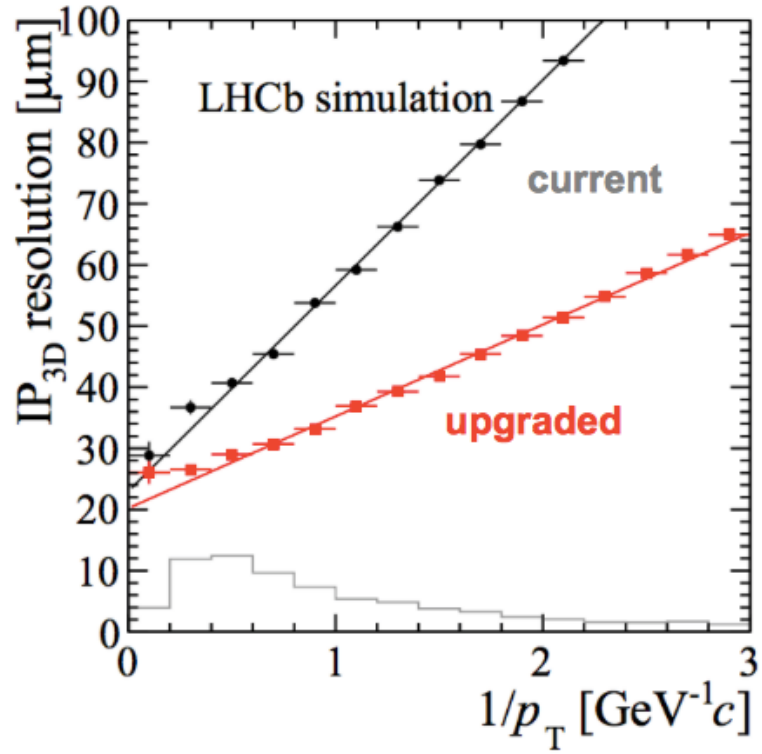
- Active silicon: the closest distance to LHC beam will be 5.1 mm (down from 8.2 mm).
- Very high ($8 \times 10^{15} n_{eq}/cm^2$ for 50 fb^{-1}) & non-uniform radiation ($\sim r^{-2.1}$)
- Huge data bandwidth: up to ~15 Gbit/s for central ASICs and 2.9 Tbit/s in total.
- Sensor temperature < -20˚C
- Total dissipation/module is ~26W.
  - ~2W/ASIC and ~2W on the innermost sensors.
  - Active cooling area ~ 24 cm^2
  - Power density: 1.1 W/cm^2
- Minimal material: cooling substrate is retracted 5 mm at the inner region.



Upgraded VELO Pixel Performance

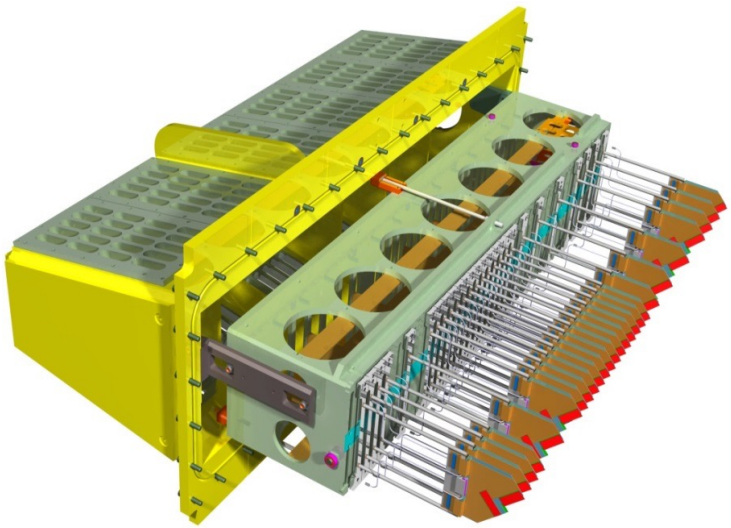
Predicted performance at $2 \times 10^{33}/cm^{-2}s^{-1}$ is superior in almost every aspect with respect to the current VELO operating at high luminosity





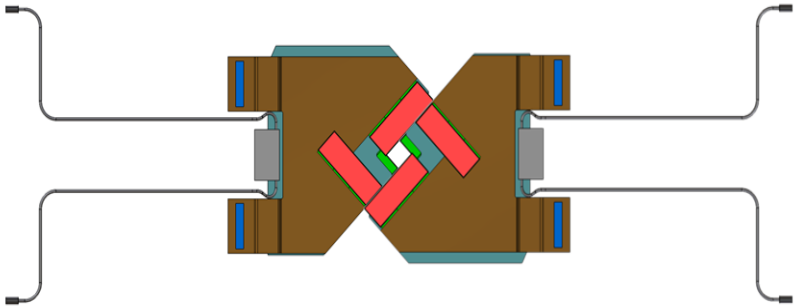
Upgraded VELO

Sensors
ASICS
Cooling Substrate

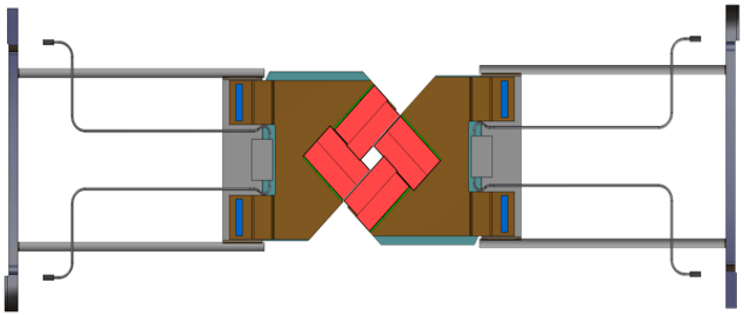


52 modules
Module pitch:
N*25 mm

VELO halves closed

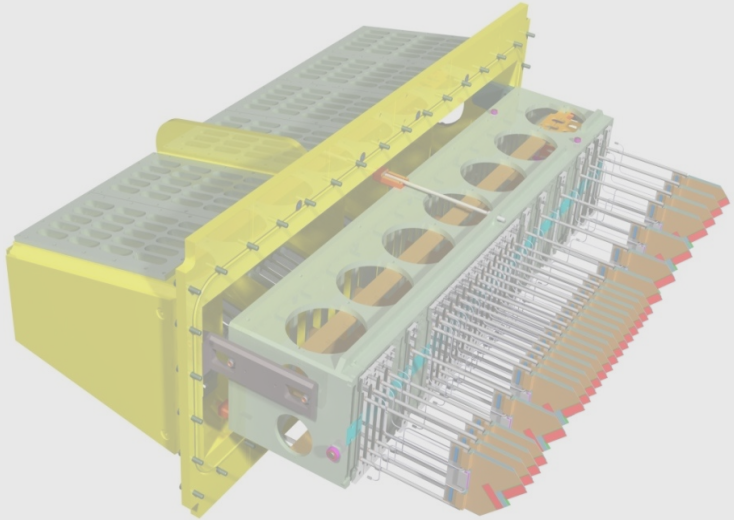


front view



projected view of sensors

The Upgraded VELO is…



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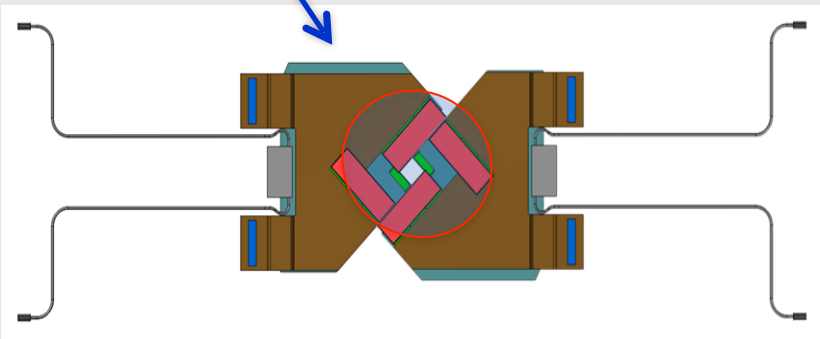
Sensors



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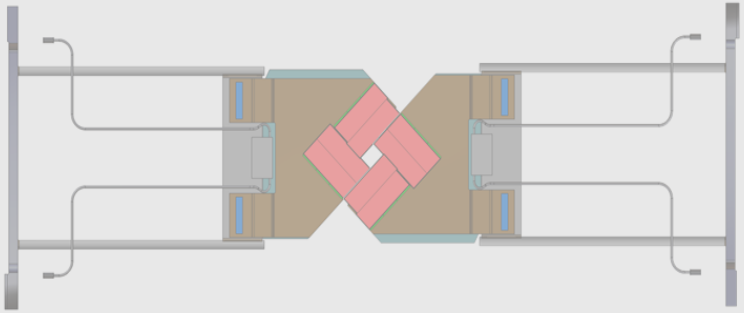
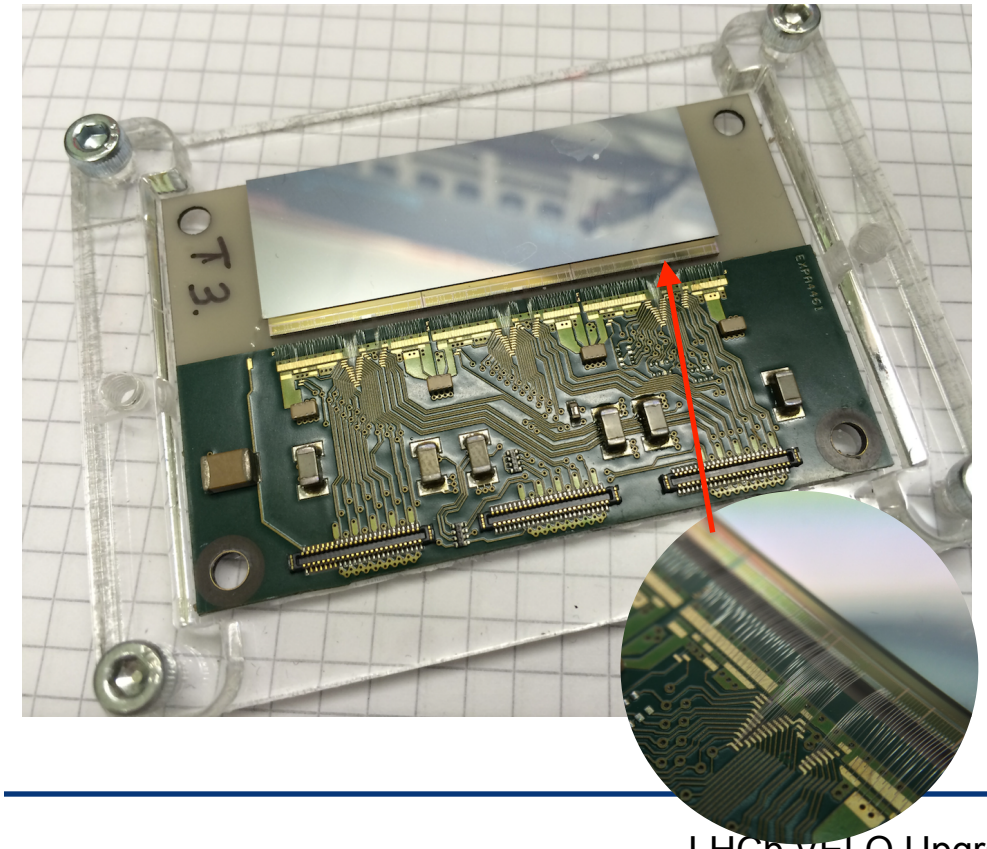


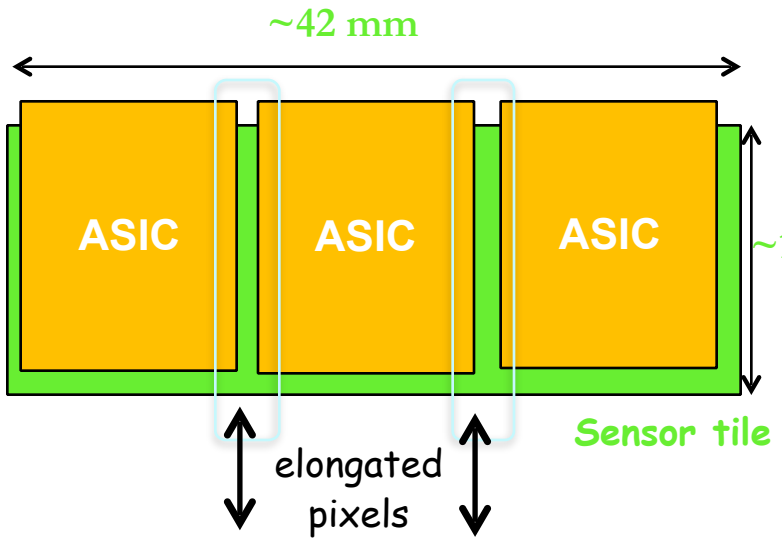
projected view of sensors

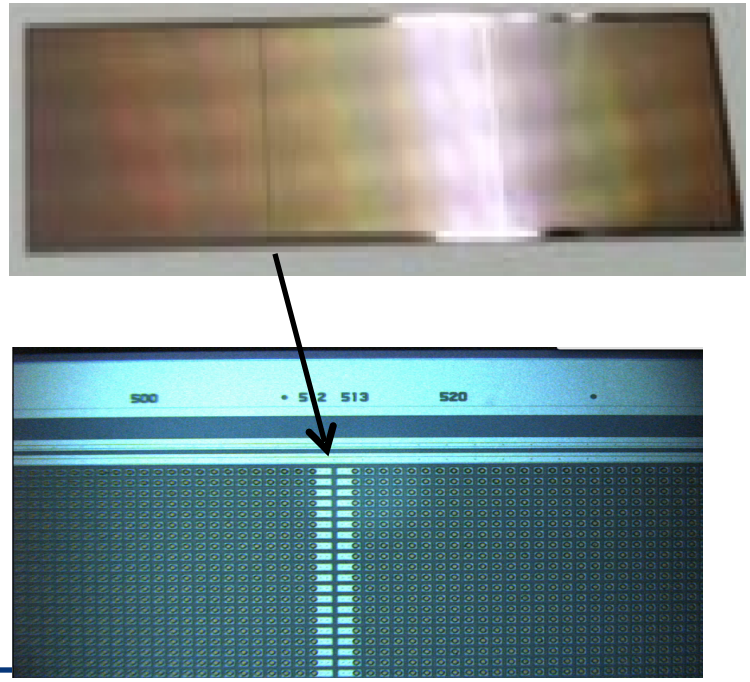
Sensors

Triple sensor prototypes in hand from two vendors

- 55 μm x 55 μm pixels
- Baseline: n-in-p, 200 μm thick, but other flavours also tested
- Bonded to hybrids and evaluated in lab/testbeam
- Irradiated with neutrons/protons







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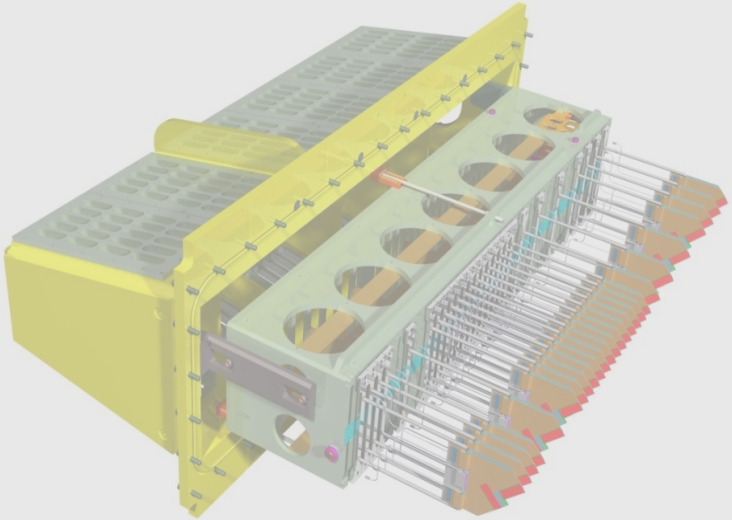

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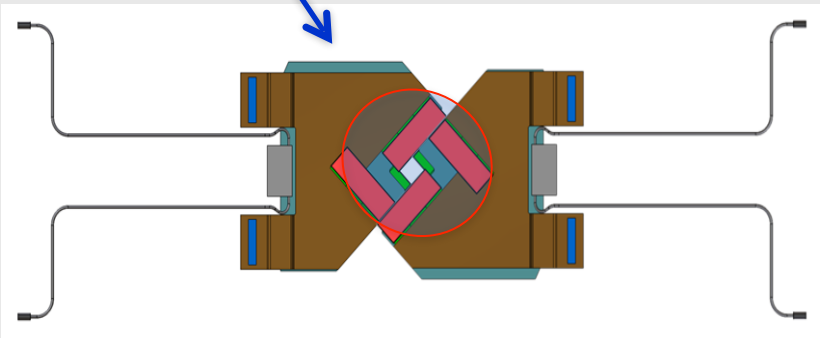
VELO halves closed

ASICs



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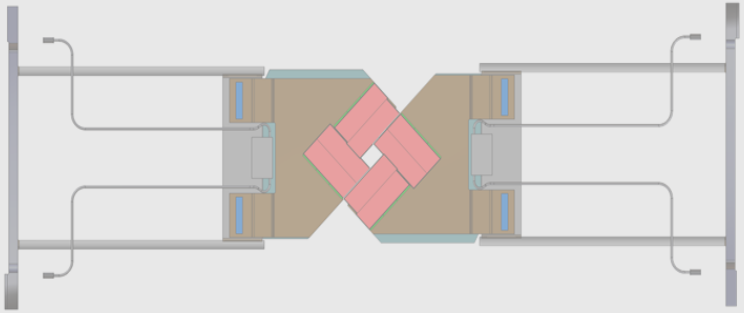
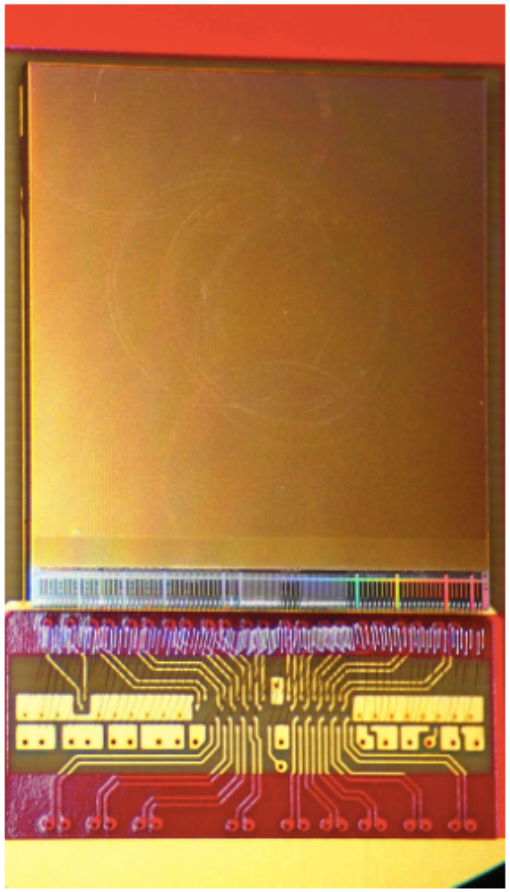


projected view of sensors

VeloPix: A pixel ASIC for VELO



Picture of Timepix3 chip, predecessor of VeloPix.

- Based on Timepix3
- 256 x 256 square pixels of 55 μm size
- 130 nm CMOS technology
- Measures
  - Position (x,y)
  - Time of Arrival with 25 ns precision
- Peak Hit rate 900 MHits/s per ASIC
- Radiation hard up to 400 MRad
- Zero suppressed data driven binary readout

Velopix ASIC specifications

Feature	VeloPix	Timepix3 [2]
Readout type	Continuous, trigger-less, binary	Continuous, trigger-less, ToT
Timing resolution/ range	25 ns, 9 bits	1.5625 ns, 18 bits
Power consumption	< 1.5 W cm^{-2}	< 1.0 W cm^{-2}
Pixel matrix, pixel size	256 x 256, 55 um x 55 um	256 x 256, 55 um x 55 um
Radiation hardness	400 Mrad, SEU tolerant	-
Peak hit rate	900 Mhits/s/ASIC 50 khits/s/pixel	80 Mhits/s/ASIC 1.2 khits/s/pixel
Sensor type	Planar silicon, e- collection	Various, e- and h+ collection
Max. data rate	20.48 Gbps	5.12 Gbps
Technology	130 nm CMOS	130 nm CMOS

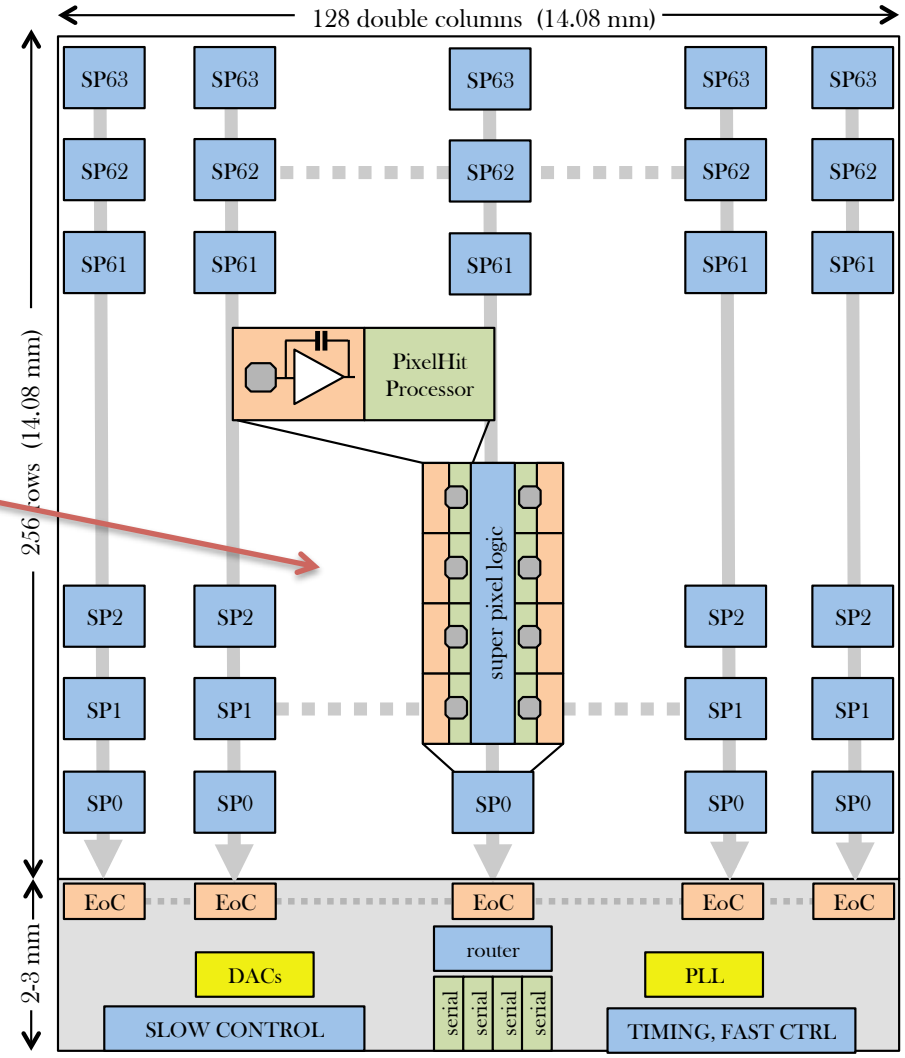
> x 10

x 4

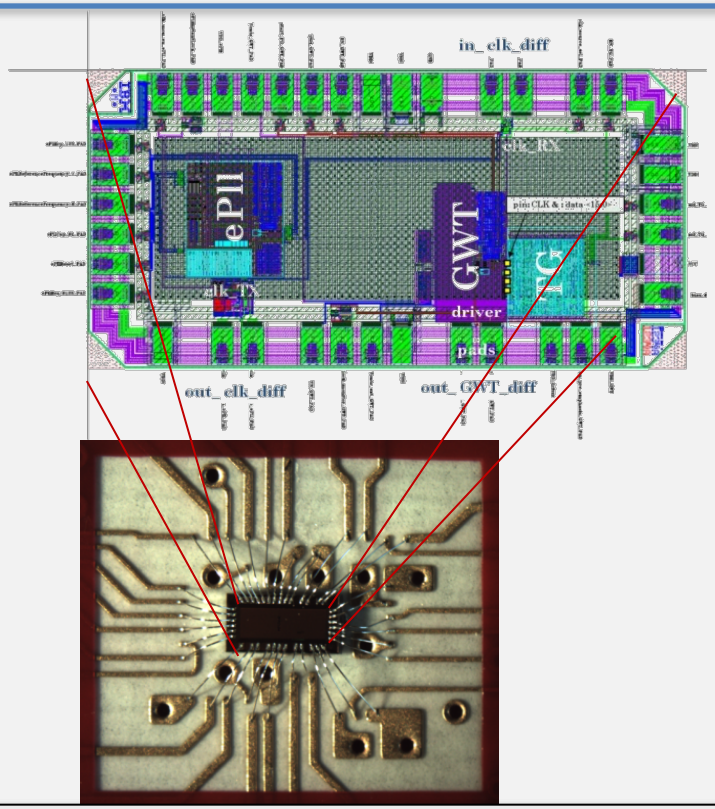
VeloPix Architecture

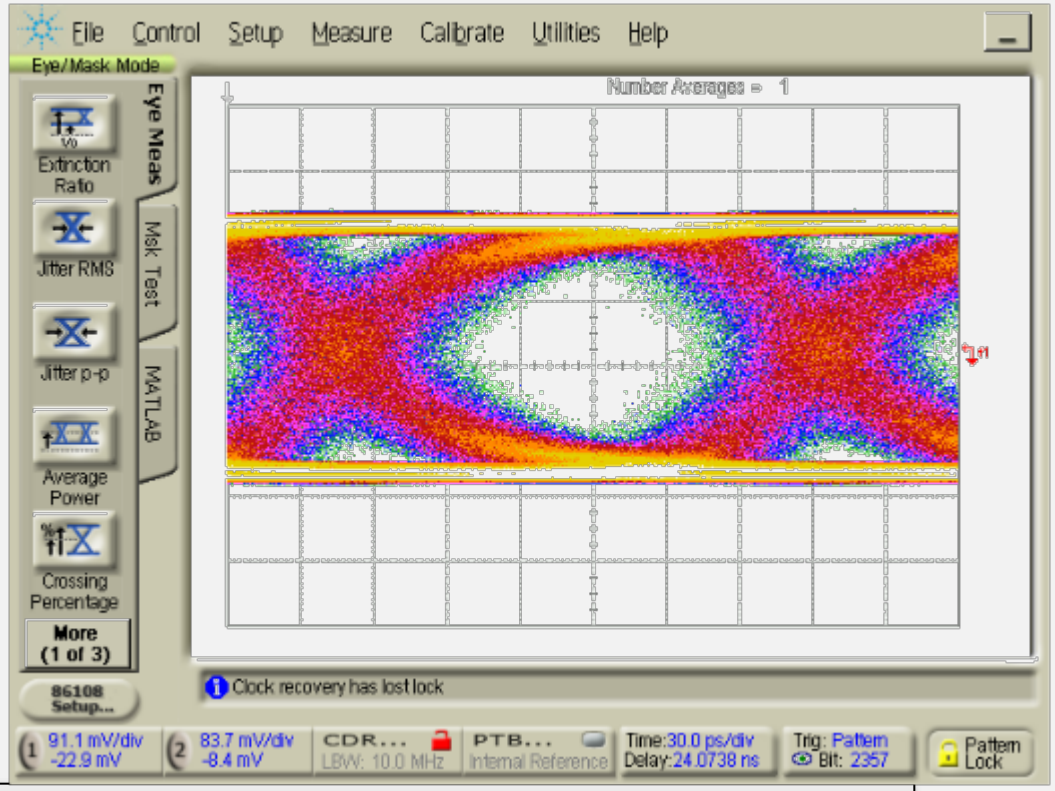
Super pixel:

- 2x4 pixels to reduce the data rates
- 30% reduction vs single-pixel



Velo_GWT test chip in 130nm CMOS technology

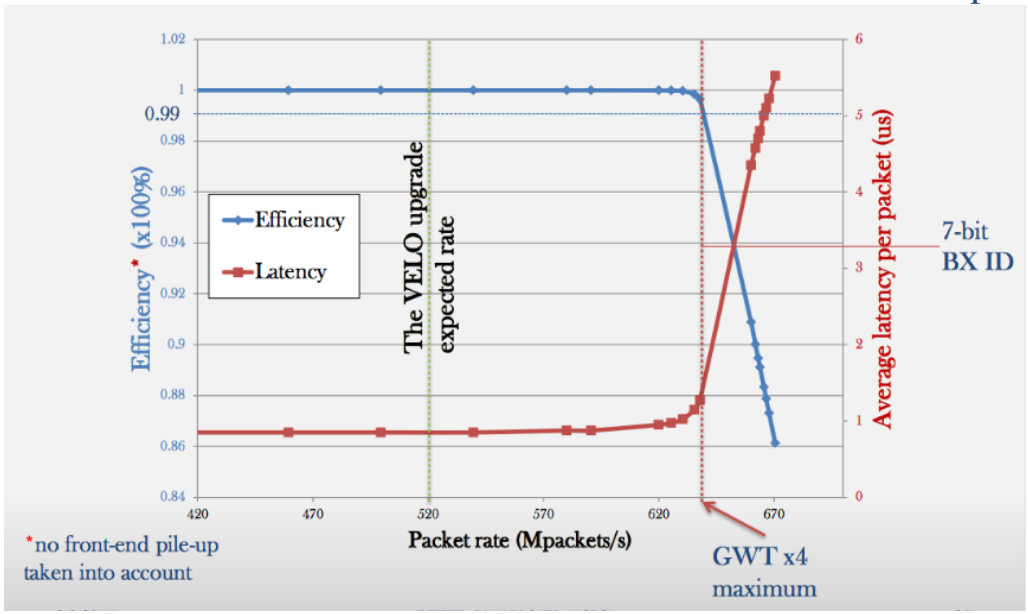


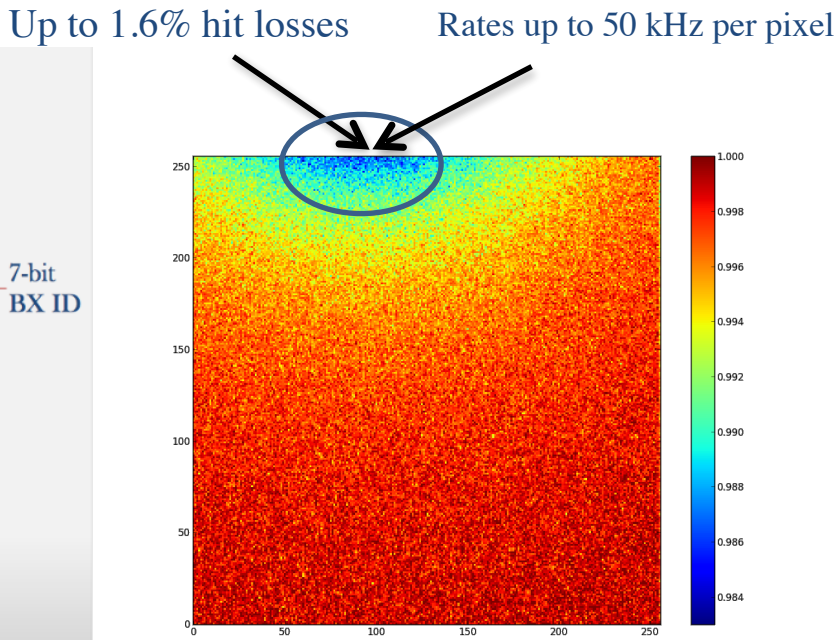


- ➢1 mm x 2 mm test chip in 130 nm CMOS technology
- ➢Power : 5.12 Gbps serializer: 15 mW, wireline driver: 45 mW
- ➢Eye diagram: +/- 200 mV is 60 ps (pseudo-random pattern)

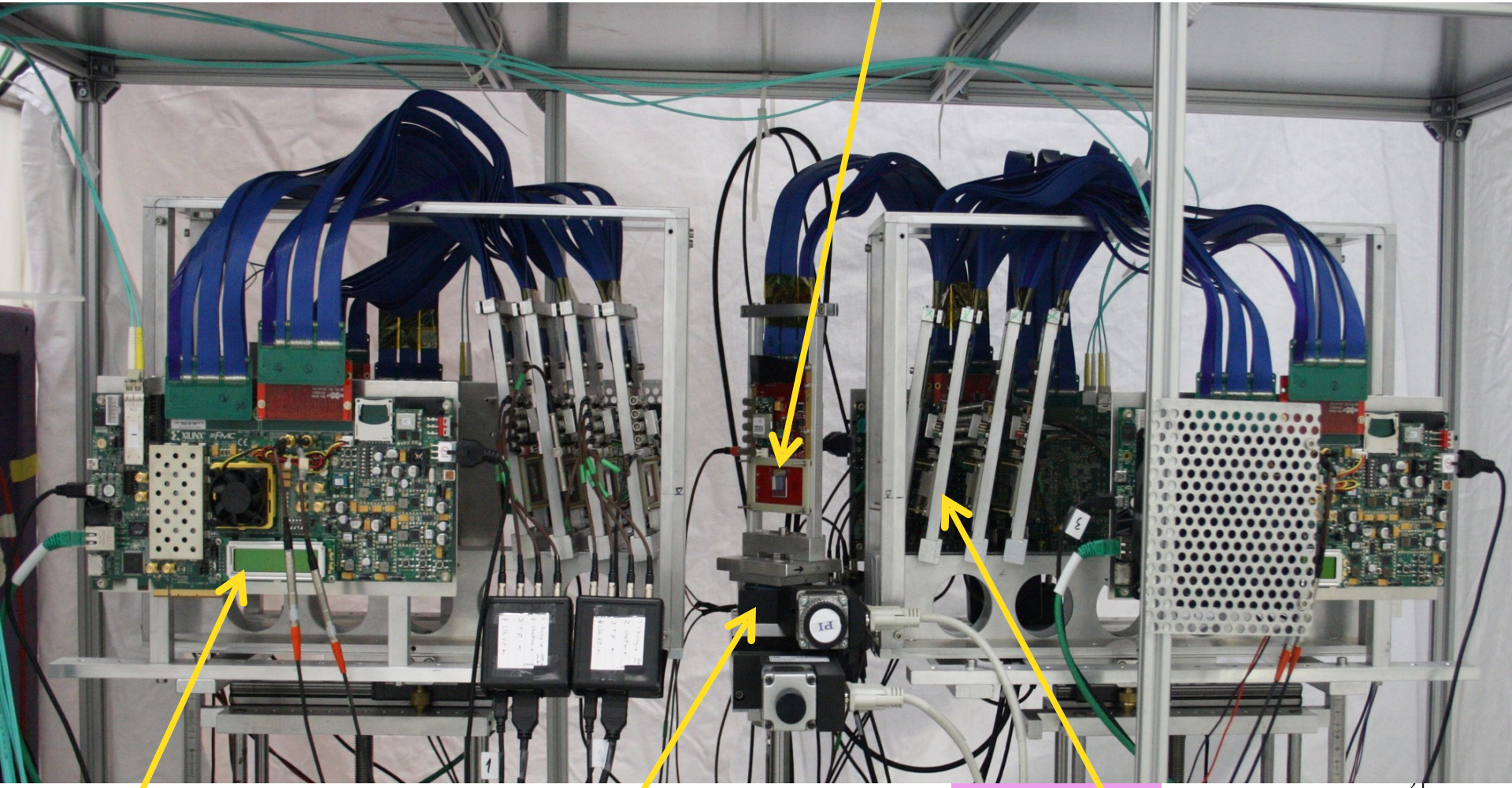
Velopix Data Rates

- Chip performance simulated with MC data
  - 15.2 Mbps for hottest ASICS
  - 27% headroom in bandwidth for hottest ASICs

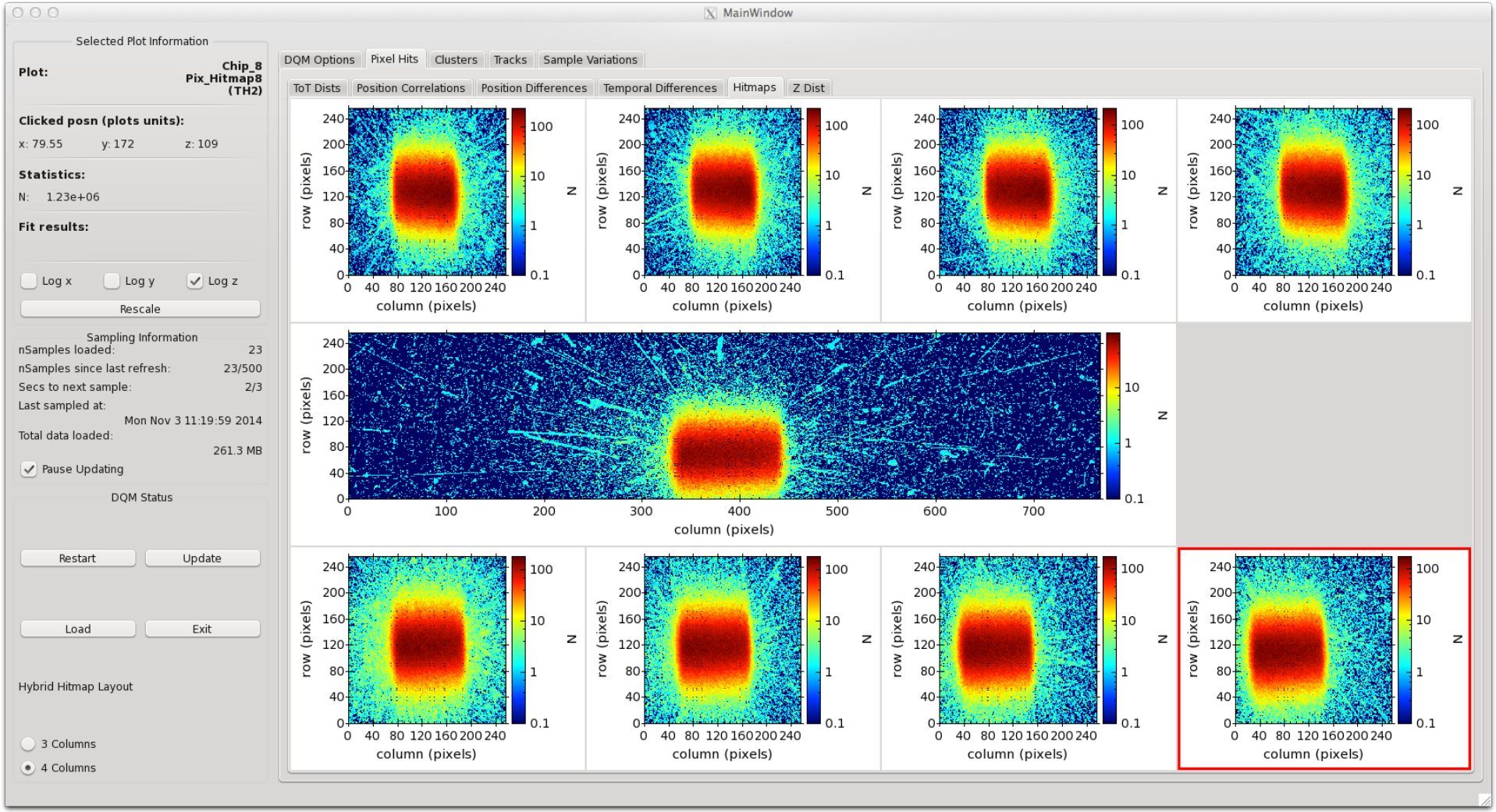




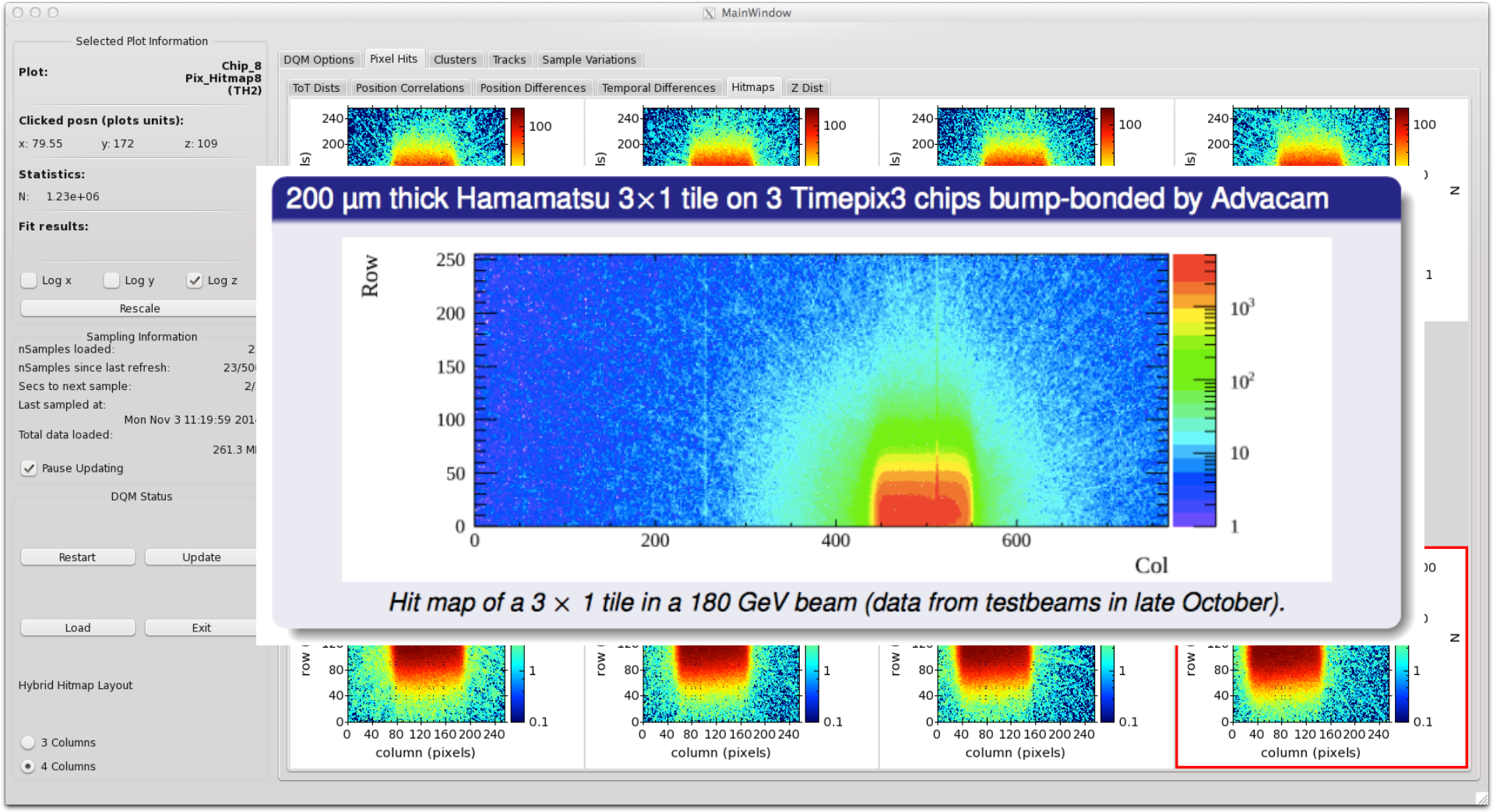
Timepix3 Telescope



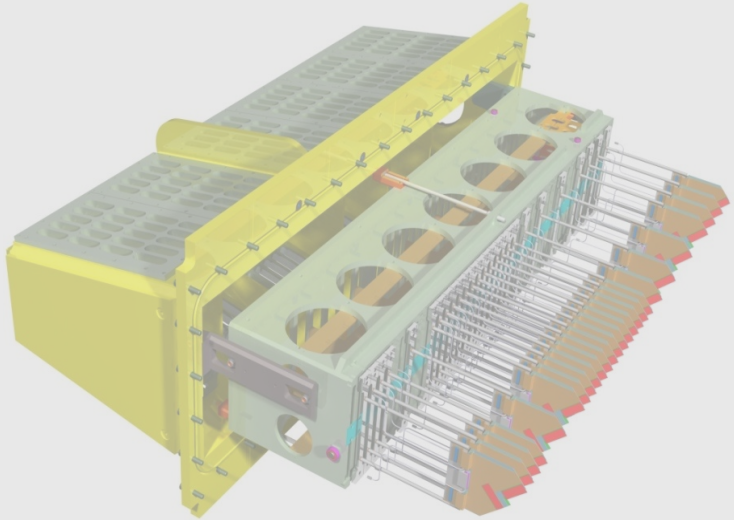
Testbeam - in one picture



Testbeam - in one picture



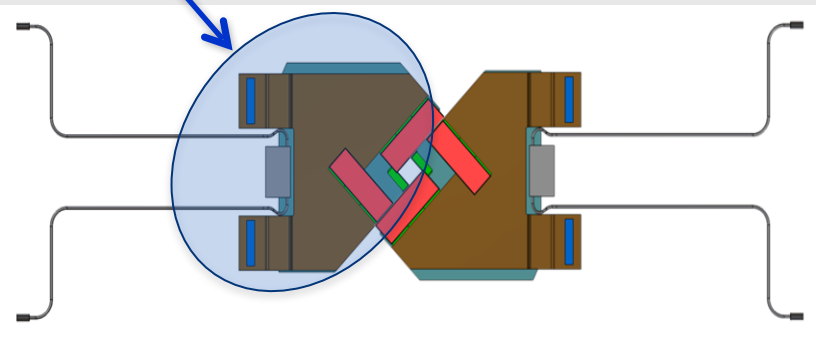
The Upgraded VELO is…



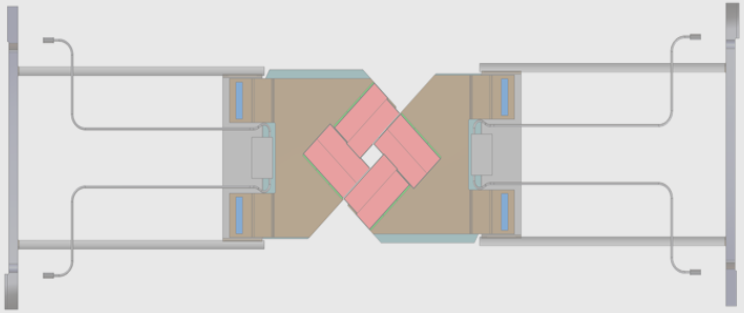
52 modules
Module pitch:
N*25 mm

COOLING SUBSTRATE

VELO halves closed

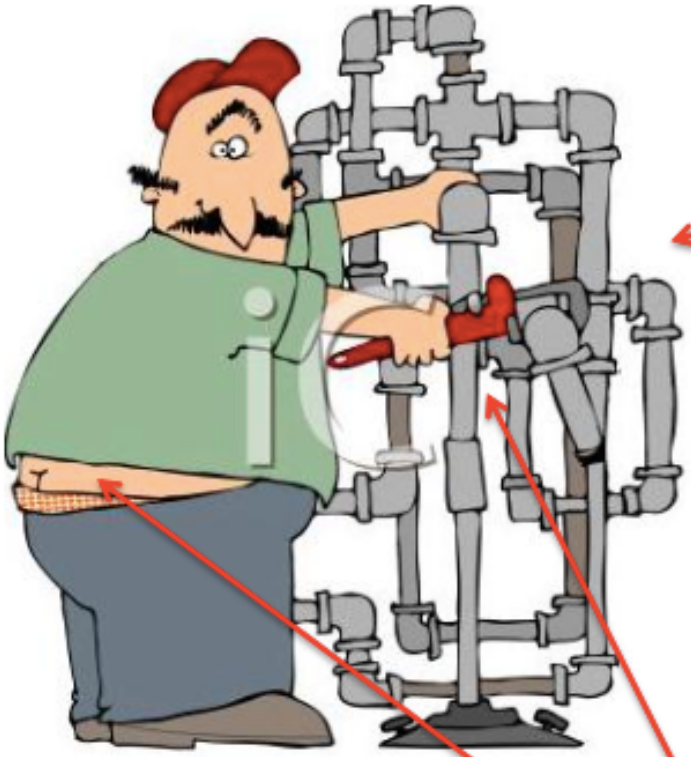


front view



projected view of sensors

Cooling – very exciting (and challenging) area



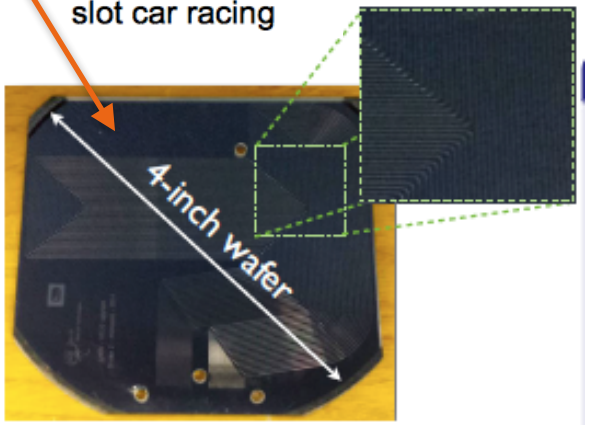
VELO CO_2 cooling a fantastic (and widely copied) success
But still there are disadvantages in the implementation:
Pipes are far from heat sources and items requiring cooling
System is bulky at point of contact and connections inefficient
CTE mismatches lead to movements and openings in the system

Microchannel cooling for VELO

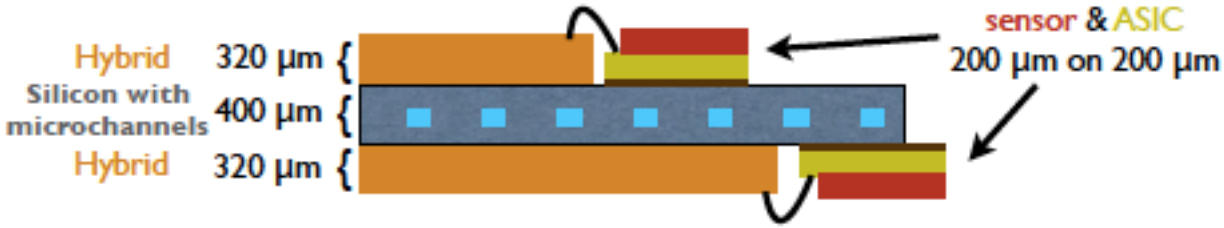
Local thermal management of detector electronics through ultra-thin micro-structured silicon cooling plates

- Combines high thermal efficiency with very low addition of mass and space
- Supresses all problems of CTE mismatch between heat source and heat sink

Same principle as slot car racing



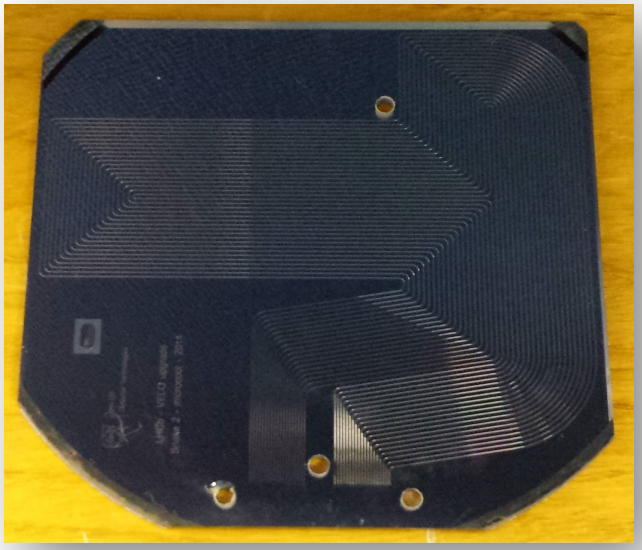
"Snake" sample on a Si-Pyrex prototype plate



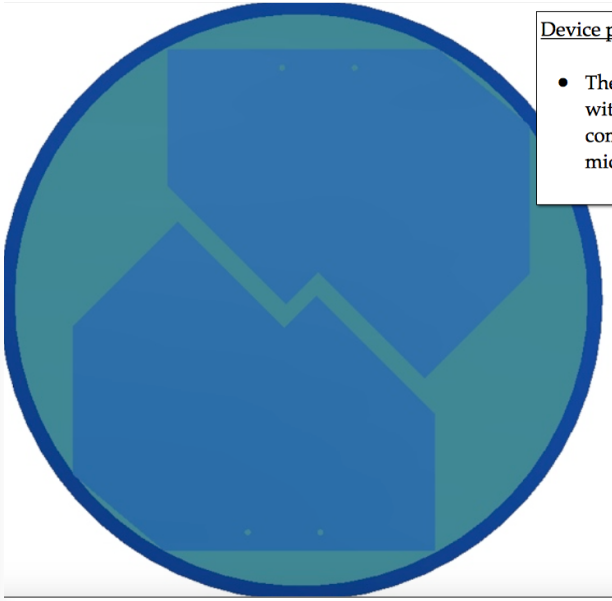
400 µm thick silicon substrate
19 parallel microchannels of 200 µm width & increasing depth up to 120 µm
Pressure up to ~65 bar at room temperature, system will be qualified to 170 bar
Cooling requirement: > 3 W / ASIC, > 36 W / module

Plate Design

Si–Pyrex prototype

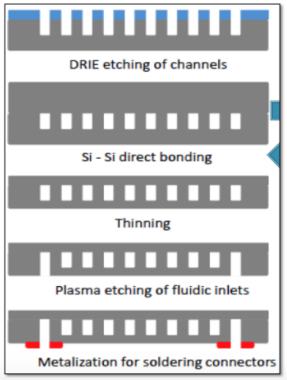


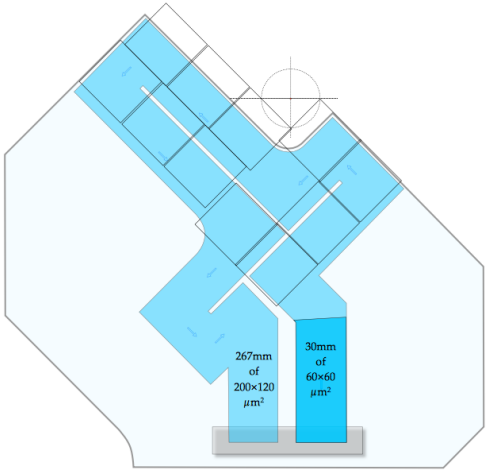
All 19 channels have nearly the same length and fluidic resistance.



Device production by industrial partner

- The microchannel substrate shall be delivered with all steps related to the silicon fabrication complete including metallisation around the microchannel ports and final dicing.

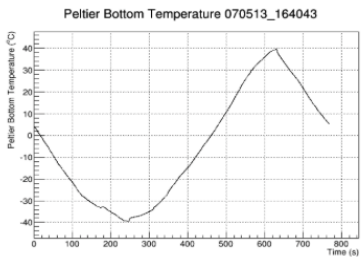




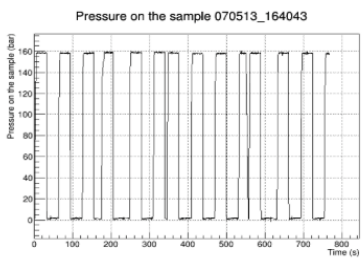
Resistance to automatic temperature/ pressure cycles

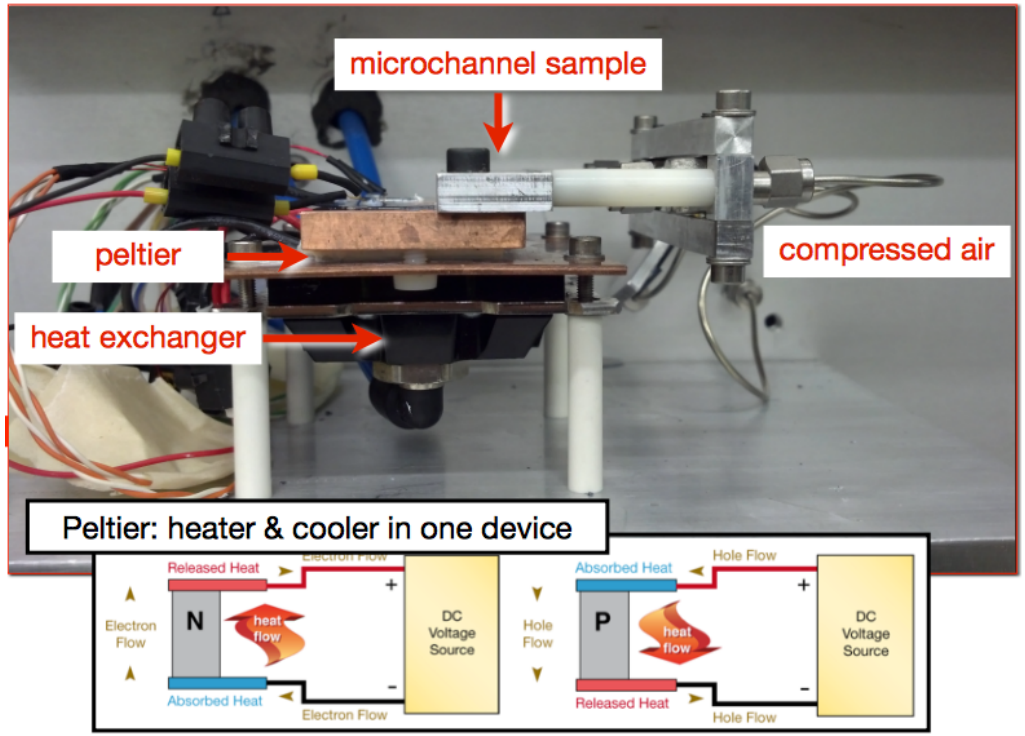
14 Pressure cycles during each temperature cycle
Thousands of cycles performed
No rupture due to stress/fatigue

80°C range
[-40°,40°]



170 bar
[0,185max]





Conclusions

- LHCb VELO Upgrade is ambitious in terms of
  - Data rate
  - Radiation hardness
- The pixel technology solves many issues, but is only possible due to the marriage with advanced cooling technology which allows efficient cooling in vacuum
- Installation for end 2018, production is close!