INFIERI 5th Workshop

April 27th 2015

CERN

Development of Novel Pixel Sensors based on 3D CMOS technology for tracking devices

*Matteo Maria VIGNETTI**

27/04/2015

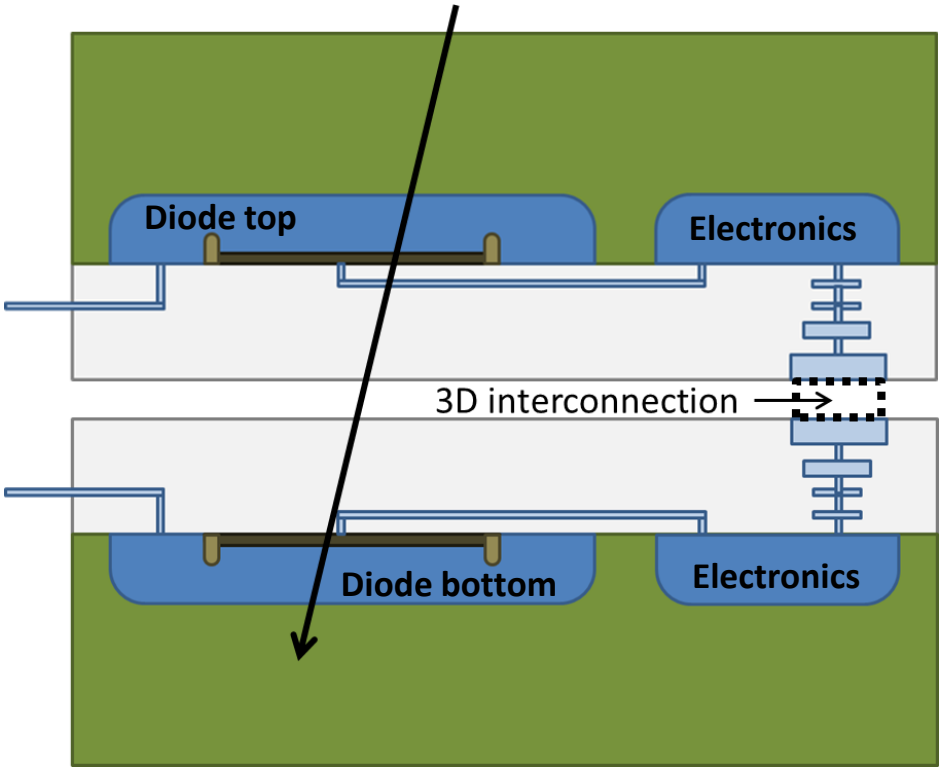
ESR WP2. Starting day February 3rd 2014

*Supported by the European Union's Seventh Framework Programme for research, technological development and demonstration under grant agreement n° 317446 (INFIERI)

Introduction

The goal of this work is to demonstrate the feasibility and the advantage of a 3D pixelated detector based on vertically aligned avalanche diodes operated in Geiger-mode where the coincidence between their output is verified*

What does 3D detector mean in this case?



- *Two tiers with avalanche diode cells.*
- *Avalanche cells from the 2 tiers are vertically aligned and interconnected defining a 3D pixel*
- *In the 3D pixel, a dedicated electronics senses coincidence events between the two avalanche diodes*

*V. Saveliev, "Avalanche Pixel Sensor and Related Methods", US Patent. 8,269,181 (2012)

Outline

- Coincidence-based Avalanche Detector concept
- Design of the avalanche diode
- Design of the pixel electronics
- Design of the 3D pixel electronics
- 3D integration
- Tape-out

Coincidence-based Avalanche Detector concept

In particles tracking systems, the ideal detector should provide a large signal while featuring a thin sensitive volume

Geiger-mode avalanche diodes:

☺ *provide strong signals thanks to a self-sustaining avalanche charge multiplication process by impact ionization in a thin space charge region*

☹ *suffer of false counts, due to dark thermal and field-assisted e/h pair generation and background photons*

3D coincidence-based detector:

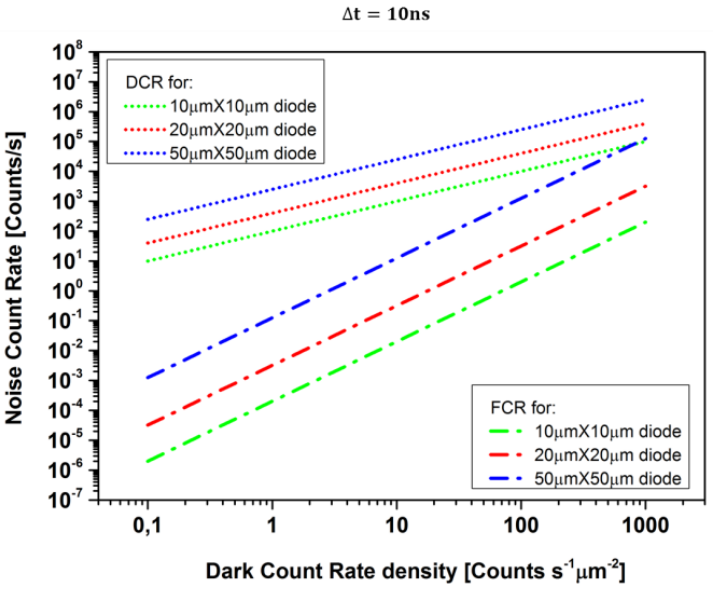
- *the coincidence between the output signals of two avalanche diodes is checked within a coincidence window Δt of a few nanoseconds*

- *In absence of an incoming particle, a **false count** may be detected if a diode is activated by a generated e-/h+ pair and, within a coincidence window Δt the other diode is activated as well:*

Fake coincidence rate:

$$FCR = 2DCR'^2 A^2 \Delta t$$

DCR': dark count rate of the diode per unit surface
A: diode active area



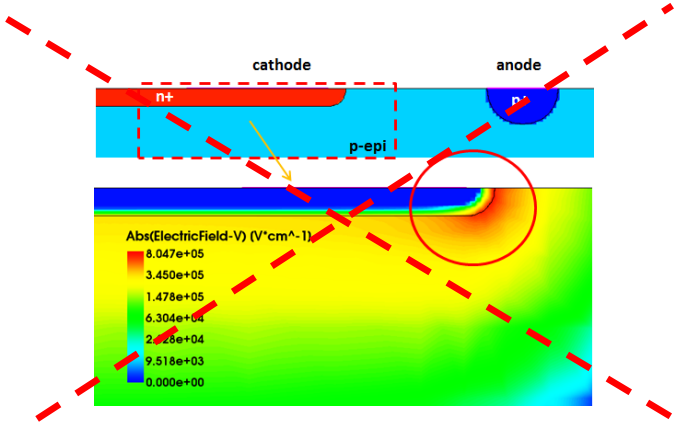
DCR vs FCR				
Technology	*DCR' (T=25°C)*	*Area*	*DCR*	*FCR (Δt = 10 ns)*
Hamamatsu	$0.1\frac{Hz}{\mu m^2}$ [1]	50x50 μm^2	250Hz	1.25mHz
Commercial HV CMOS 350nm	$\sim 10\frac{Hz}{\mu m^2}$ [2]	50x50 μm^2	25kHz	12.5Hz
Commercial CMOS 130nm	$\sim 100\frac{Hz}{\mu m^2}$ [3]	50x50 μm^2	250kHz	1.25kHz

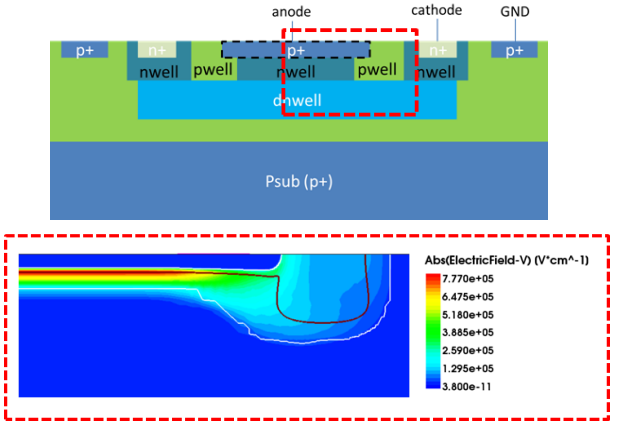
http://www.hamamatsu.com/eu/en/product/category/3100/4004/4113/S12571-010C/index.html [1]
E. Vilella "Feasibility of Geiger-mode avalanche photodiodes in CMOS standard technologies for tracker detectors", PhD Thesis – University of Barcelona (Spain) – October 2013 [2]
C. Niclass et al "A single photon avalanche diode implemented in 130-nm CMOS technology", IEEE J. Sel. Top.Quant. Electron. 13 (2007) 863–869 [3]

Design of the avalanche diode

The design has to accomplish:

- ***premature edge breakdown (PEB) prevention***

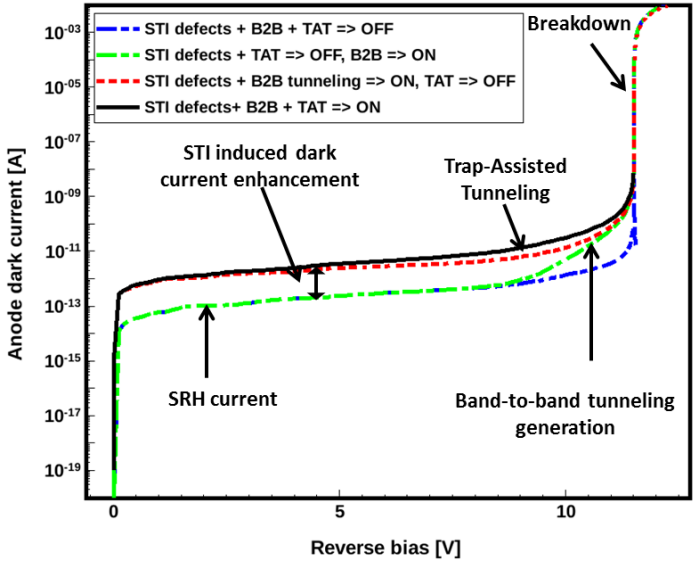




OK!

Electric Field @ 15V (Vbd=11,8V):

- ***Dark counts minimization***

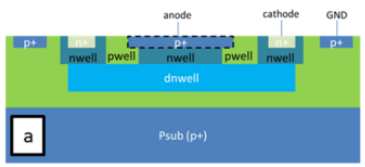


- **Band-to-band generation:**
  high doping concentration levels cause a very narrow depletion region resulting in a significant tunneling dark current and therefore an enhanced DCR

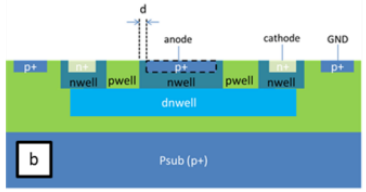
- **STI-induced dark count enhancement:**
  Below the 250nm node, standard CMOS processes feature STI which may increase the density of deep-level carrier generation centers at the Silicon/STI interface and therefore the dark generation of the diode

Design of the avalanche diode

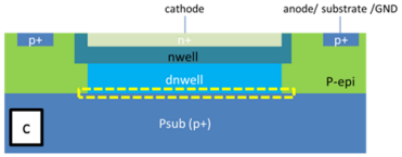
TCAD simulations of several avalanche diode architectures found in literature:



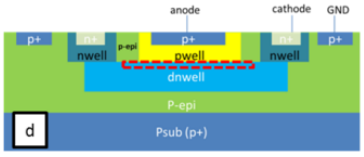
Low doped p-well guard ring



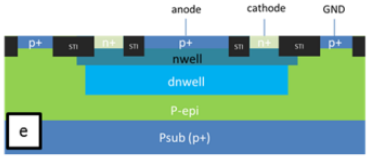
Slightly spaced low doped p-well guard ring



Deep N-Well/Psubstrate based avalanche diode



P-Well/Deep N-Well based avalanche diode



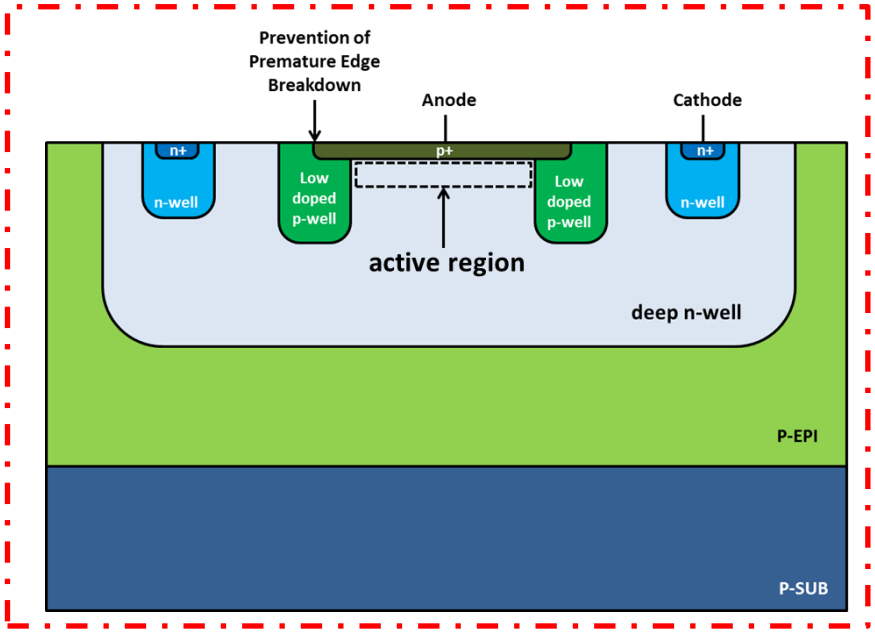
Shallow Trench Isolation (STI) based guard ring

Choice of the architecture based on:

- *Affordable CMOS technology in terms of tape-out costs*
- *Best performing architecture among those compatible with the chosen CMOS technology*

Implementation in AMS HV-CMOS 0,35µm tech

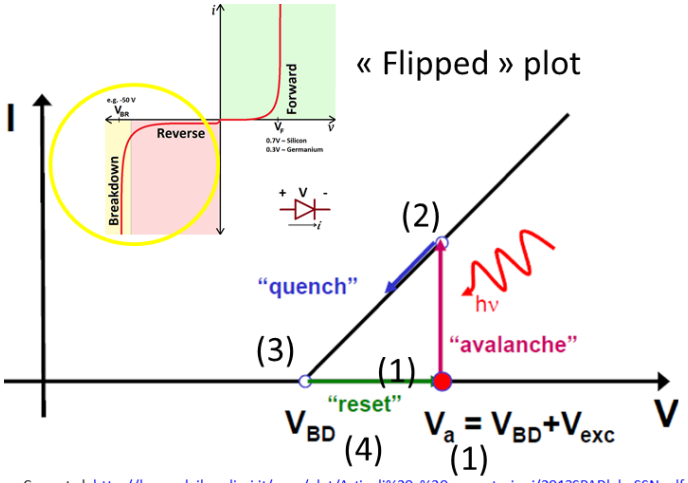
- *PEB prevented thanks to a low doped p-well guard-ring*
- *Expected low B2B tunneling generation thanks to a low n-type doping in the multiplication region*
- *Already used for design of CMOS avalanche diodes showing good DCR levels*



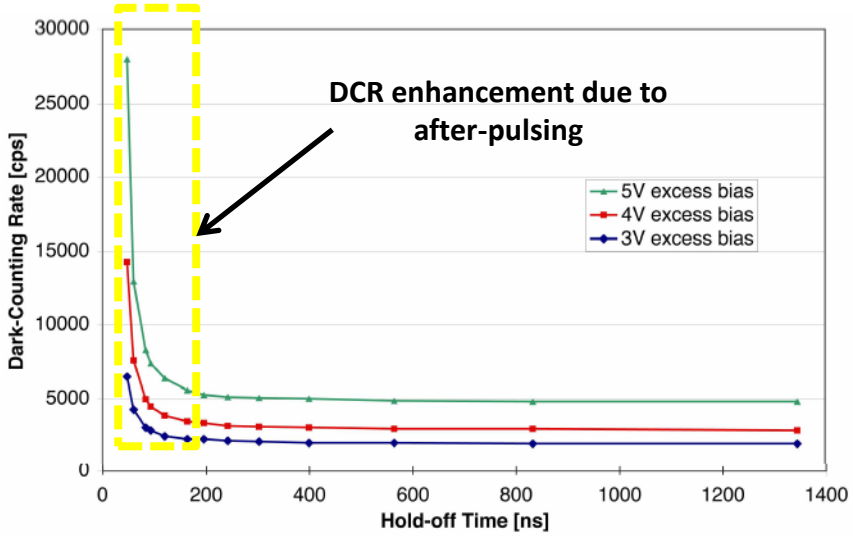
Design of the pixel electronics

The pixel electronics has to:

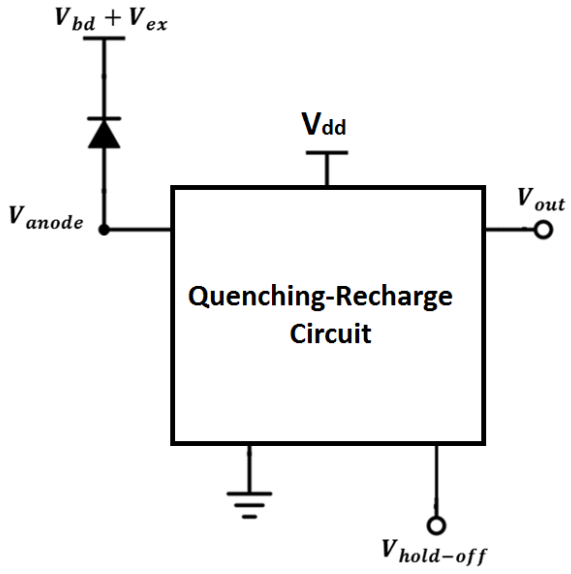
- **effectively drive the avalanche diode in the Geiger-mode**
- **Be a flexible tool to fully characterize the avalanche diode noise performance:**



Cova et al. http://home.deib.polimi.it/cova/elet/Articoli%20e%20presentazioni/2013SPADlab_SSN.pdf



S. Tisa, F. Guerrieri, and F. Zappa "**Variable-Load Quenching Circuit for single-photon avalanche diodes**"Optics Express, Vol. 16, Issue 3, pp. 2232-2244 (2008)



Need for electronics enabling an external tuning of the hold-off time within a wide range, i.e. 10ns up to 1us*

** The time the avalanche diode is not biased above the breakdown voltage*

Design of the pixel electronics

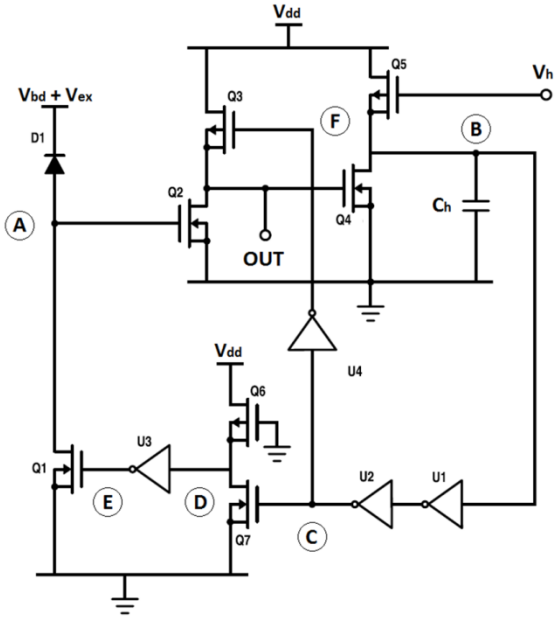
Variable resistor-based approach

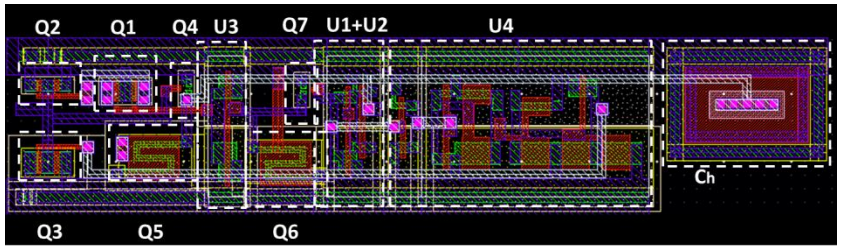
- *Easy: a simple variable resistor is required for quenching and recharge*
- *There is not a real hold-off time: recharge phase is simply slow down*

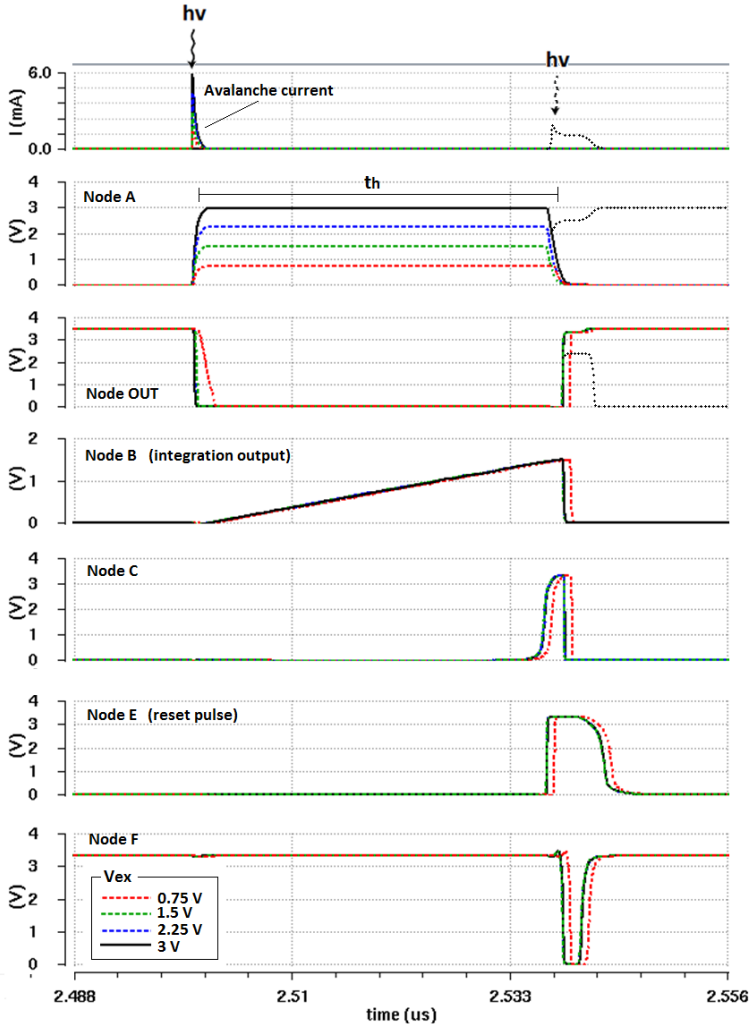
Passive quench - active recharge based approach

- *hold-off period is well defined: recharge phase is **delayed***
- *Some efforts in circuit design are required*

Passive quench-active recharge circuit proposed in this work



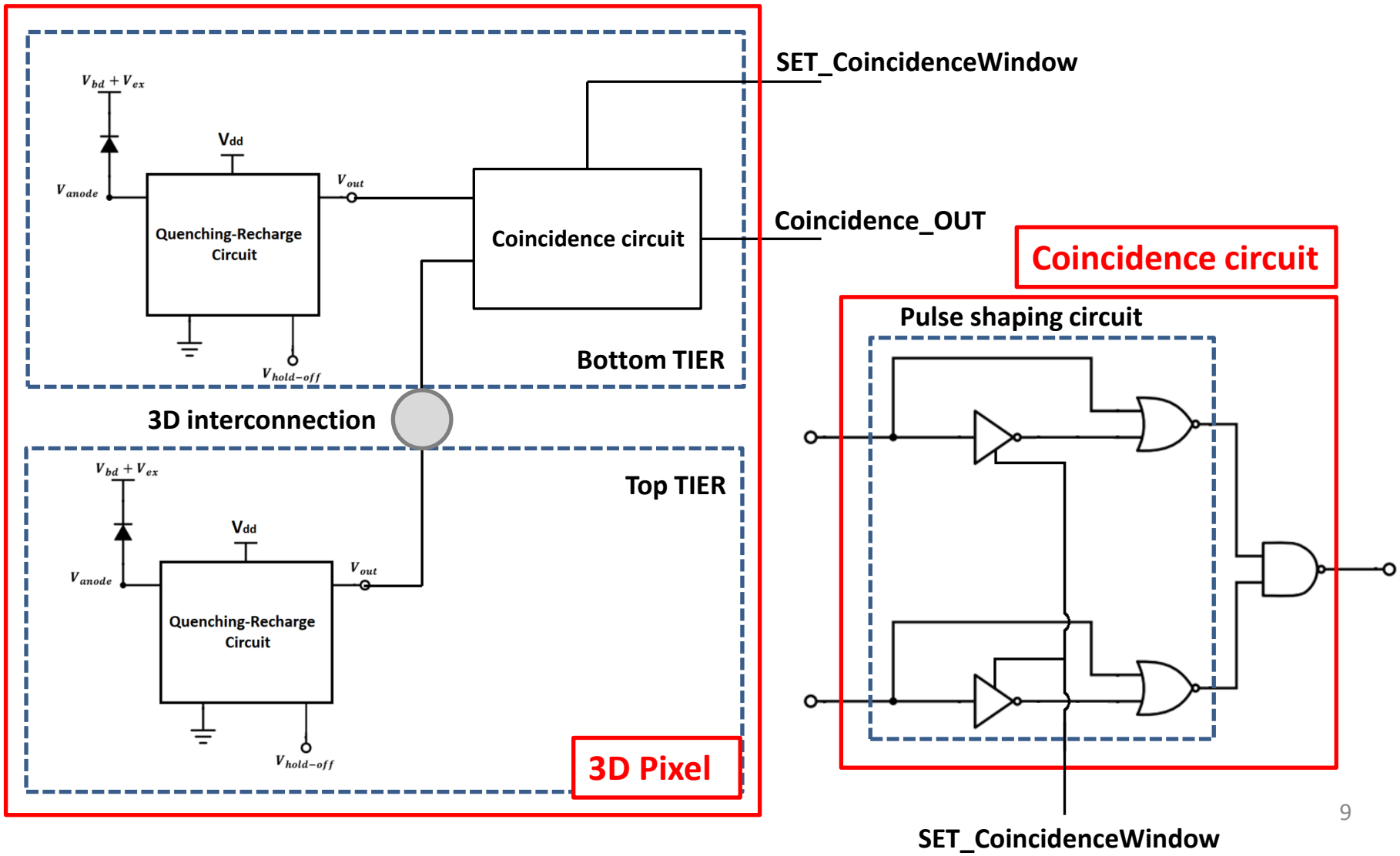




M. M. Vignetti et al. "*A time-integration based quenching circuit for Geiger-mode avalanche diodes*" IEEE NEWCAS 2015

Design of the 3D pixel electronics

The 3D pixel electronics has to be conceived in order to account for the possible parasitics introduced by the vertical interconnections.



3D integration

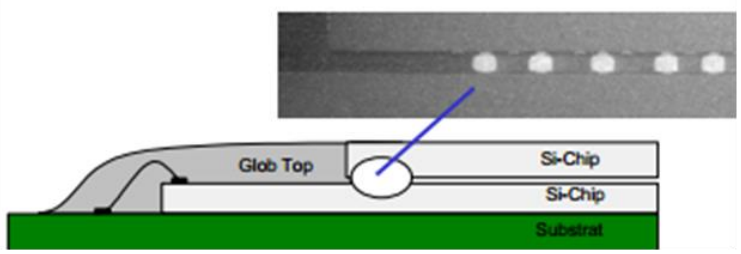
Choice of the 3D integration technology

Dedicated 3D technologies:

- *Optimized for 3D design: negligible parasitics, very large scale integration enabled*
- *Expensive: wafer level manufacturing, uncertainty on MPW runs.*

Flip chip assembly:

- *It's rather a 3D assembly than a real 3D integration*
- *No TSV, large surface required for bump bonding*
- *Affordable, chip-to-chip assembly is possible*



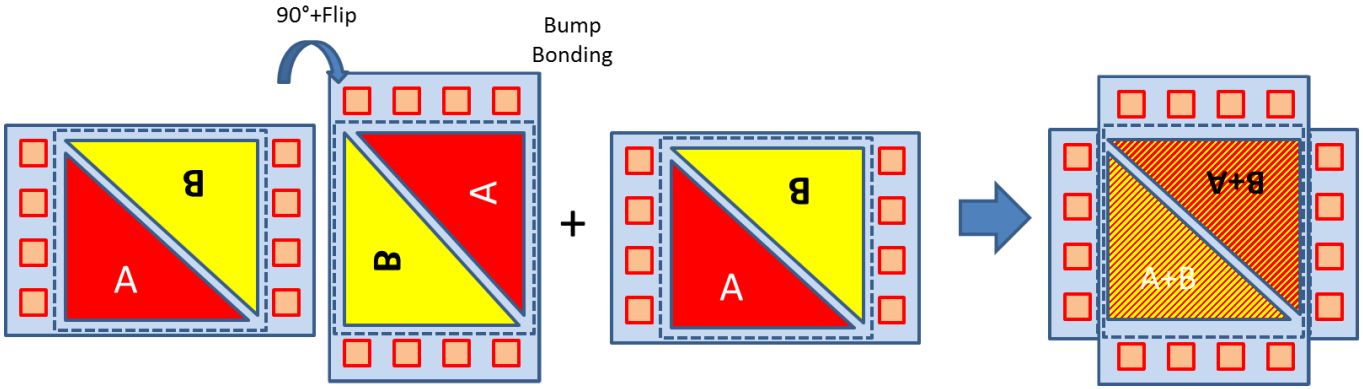
P. Ramm, A. Klumpp, R. Merkel, J. Weber, R. Wieland, A. Ostmann, J. Wolf "3D System Integration Technologies" Mat. Res. Soc. Symp. Proc. Vol. 766 © 2003 Materials Research Society

Design strategy:

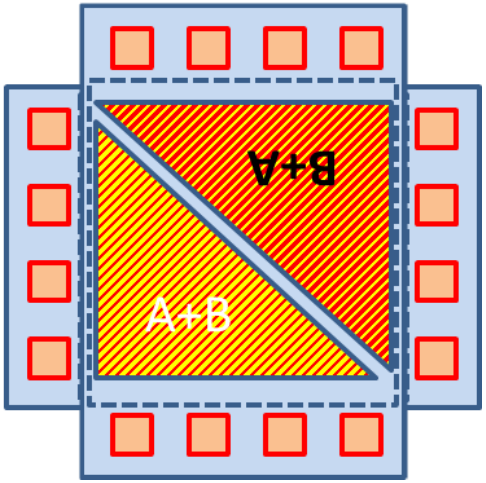
- *One test chip for the TOP tier and another one for the BOTTOM tier: not affordable!*
- *ONLY one test chip by adopting a smart solution…*

3D integration

3D integration strategy: ***TOP tier and BOTTOM tier on the same chip***



- *TOP tier will be on triangle "A" while BOTTOM tier will be on triangle "B"*
- *Flip-chip assembly of 2 identical test-chips after 90° rotation and flip of one test chip*



- B will be over A after flip-chip (B_{TOP}) and vice-versa
- Only external PADs on BOTTOM die will be wire-bonded
- B_{TOP} can be controlled and observed only via BOTTOM external PADs through vertical interconnections

Tape-out

A test-chip has been submitted for TAPE-OUT on April 23rd 2015 in a MPW run.

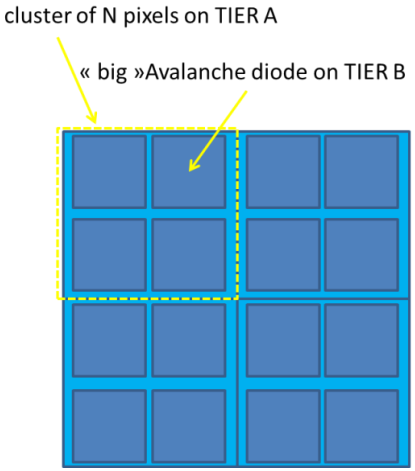
In the test chip we placed:

Avalanche diode test structures

Several 3D pixels cells for coincidence-based detection:

- *avalanche diodes are driven by the passive quench – active recharge circuit proposed in this work and by simple variable-resistance quenching elements*
- *the coincidence is verified thanks to the circuit proposed in this work.*

Small 2x2 matrix cells exploiting a hybrid coincidence-based detection:



- ONLY a single 3D vertical connection (instead of N) is required!
- However for each pixel of one cluster, the FCR gets worse by a factor N

Conclusions

- An avalanche diode has been designed accounting for the noise performance and the technological limitation imposed by the adopted CMOS process
- A passive quench – active recharge circuit for driving avalanche diodes in the Geiger-mode has been devised
- A circuit for detecting the coincidence between two avalanche cells has been proposed as well
- A 3D coincidence-based pixel as well as a small hybrid matrix has been successfully designed.
- Test-chip submission for tape-out has been successfully accomplished
- A test board design for the submitted test-chip is in progress
- A design based on a dedicated real 3D technology is still to be considered

Thanks!

Back-up

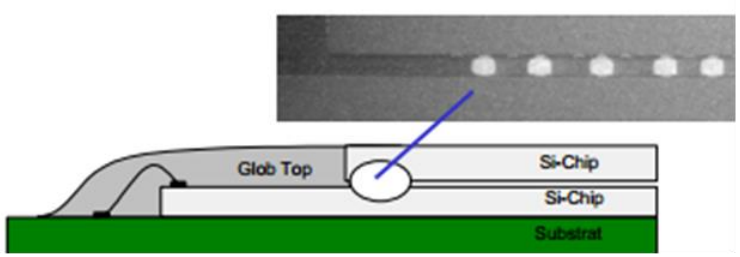
Flip-chip assembling features

- Flip-chip bonding PAD:

  size: ~100um X 100 um (for reliability)
  spacing: 100 um
  Diameter of gold balls: 70um

- Wire bonding PAD

  size: ~60um X 60 um
  spacing: ~70 um



P. Ramm, A. Klumpp, R. Merkel, J. Weber, R. Wieland, A. Ostmann, J. Wolf "3D System Integration Technologies" Mat. Res. Soc. Symp. Proc. Vol. 766 © 2003 Materials Research Society

Back-up