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L1 TRACK FINDING FOR A TIME MULTIPLEXED TRIGGER

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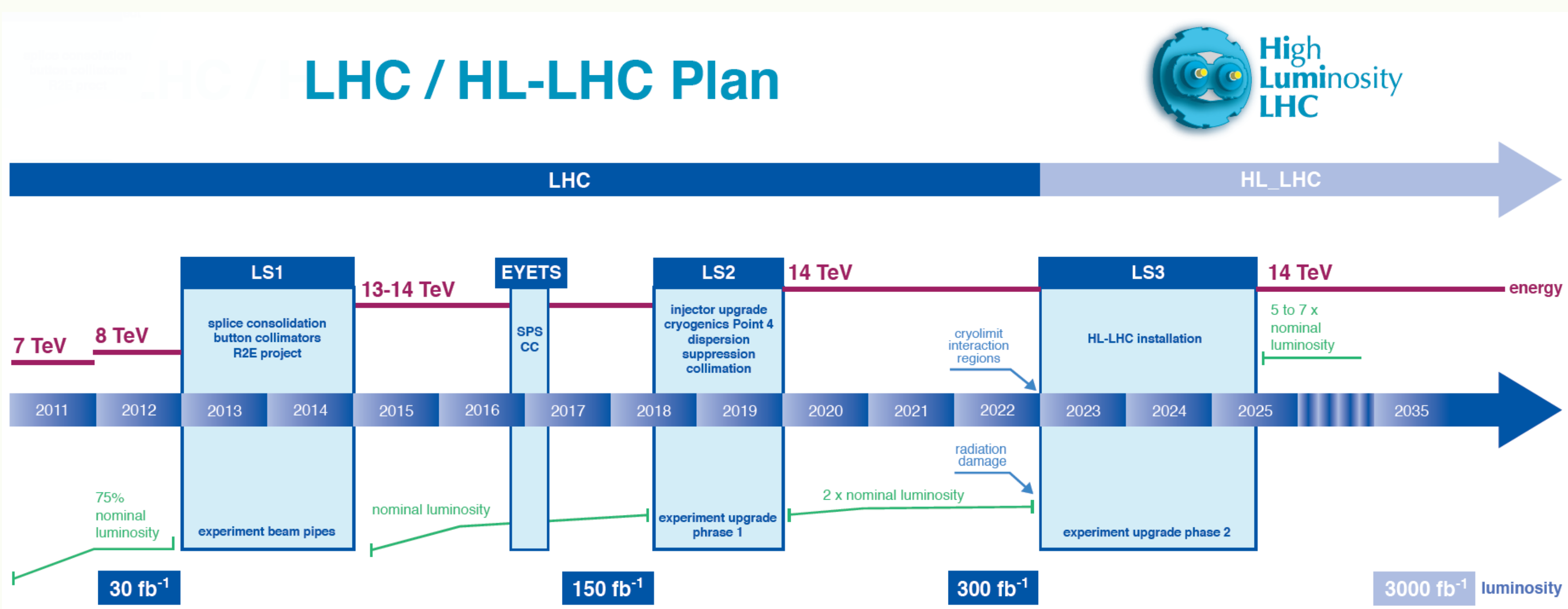
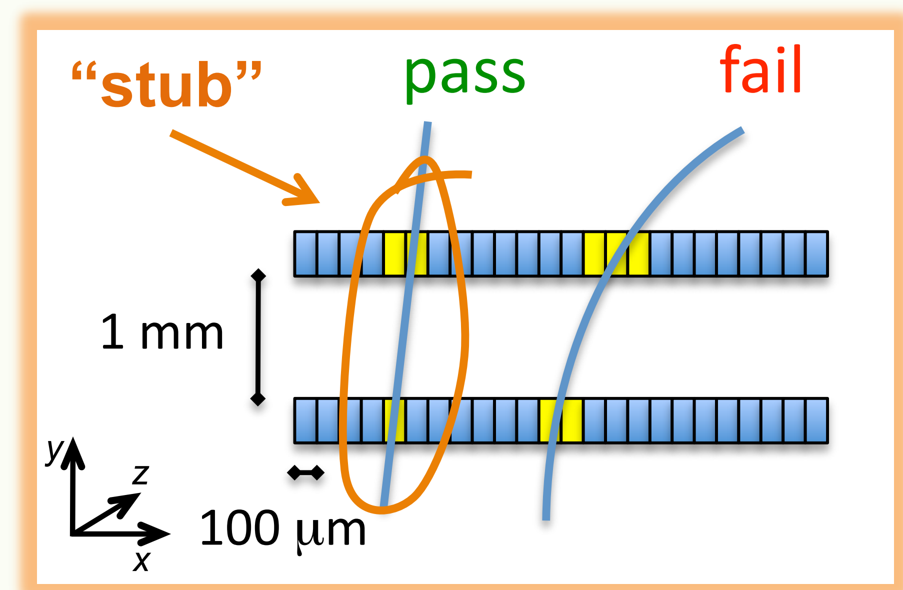
INTRODUCTION

- THE TIME MULTIPLEXED TRIGGER
- SYSTEM ARCHITECTURE
- TRACK FINDING USING HOUGH TRANSFORM
- SOFTWARE SIMULATION
- HARDWARE IMPLEMENTATION
- DEMONSTRATOR
- THE FUTURE

THE TIME MULTIPLEXED TRIGGER

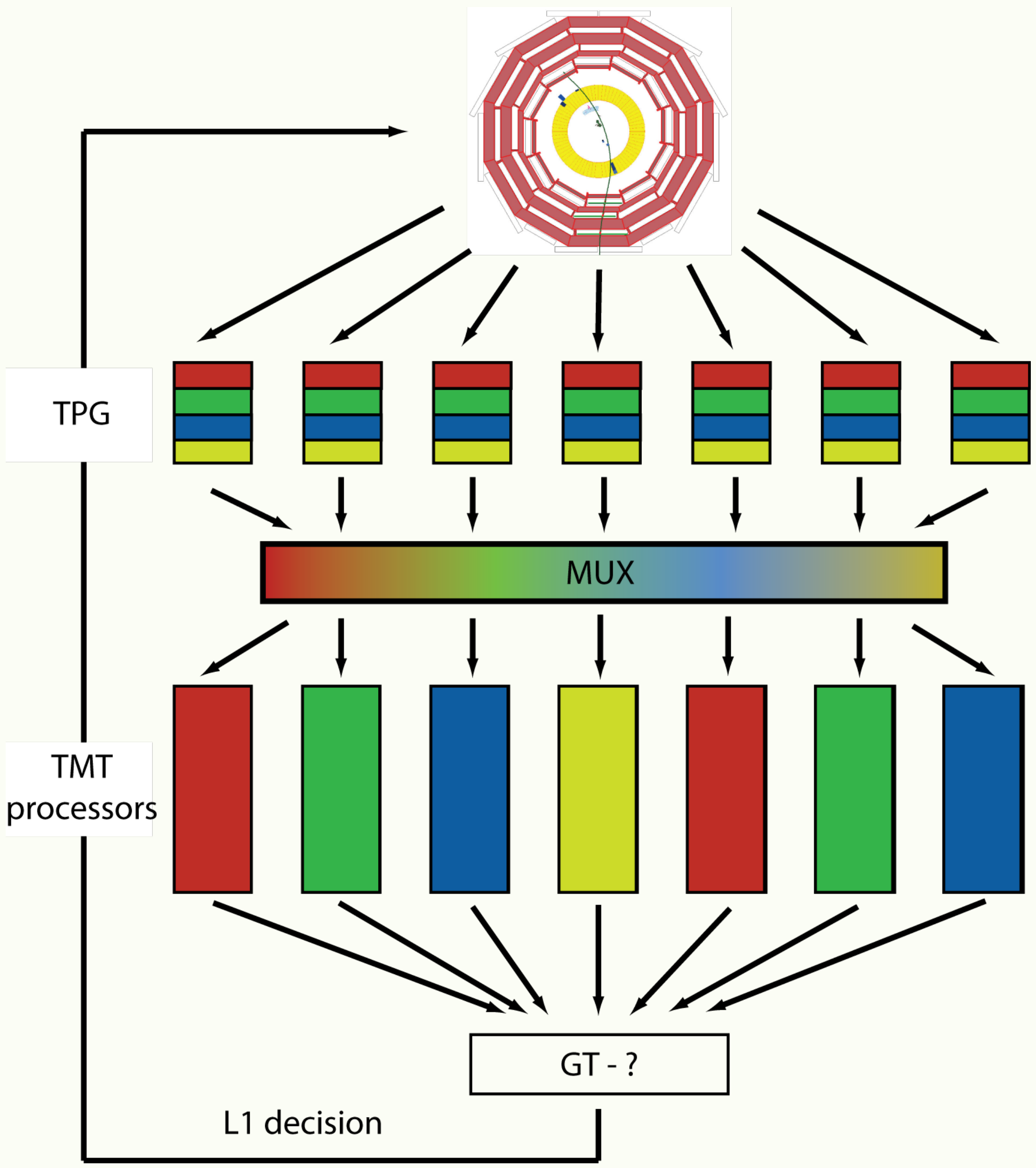
- **HL-LHC** will run up to an integrated luminosity of 3000 fb^{-1}
- To constrain trigger rate CMS will need to use also **tracker** informations for **L1 trigger** purpose
- CMS will have a complete new tracker for the Phase II upgrade
- New tracker will adopt **double sensors** module (PS & 2S modules)
- A correlation between hits in a two sensors consistent with high pT track will be called a **stub**
- Tracks under a certain threshold can be then rejected



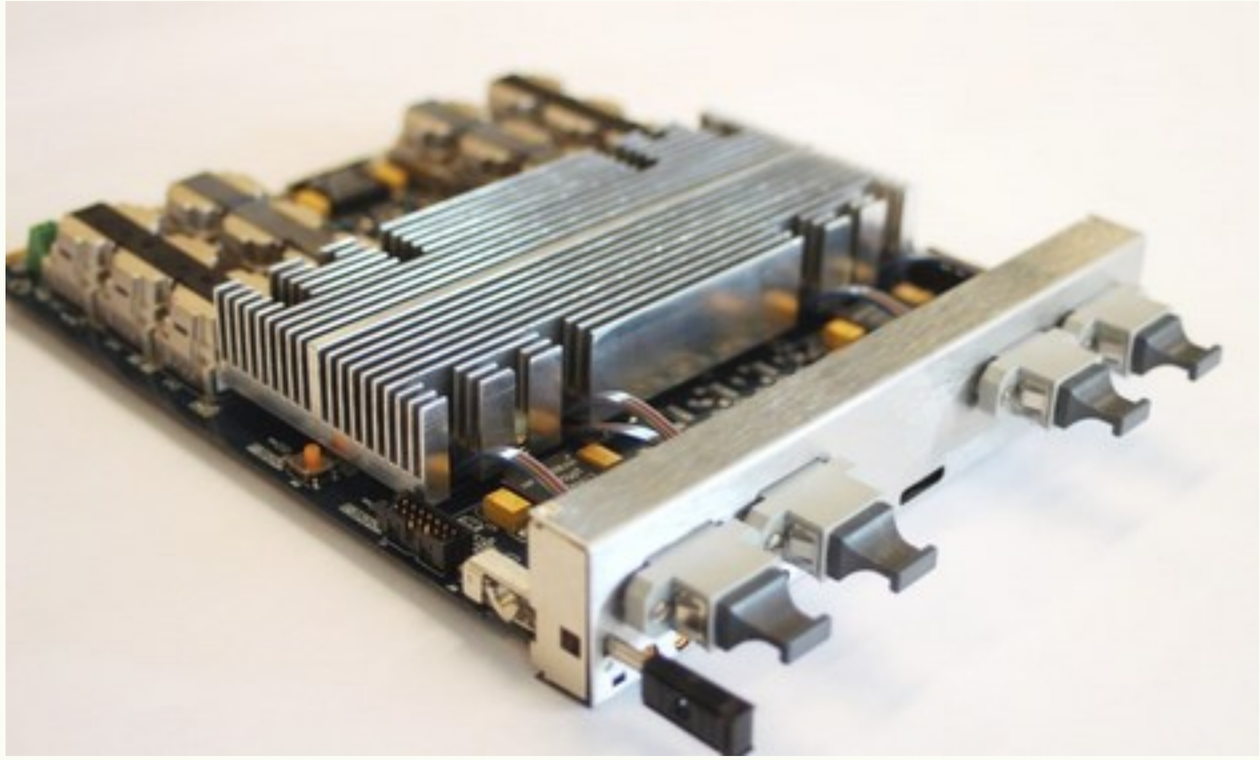


THE TIME MULTIPLEXED TRIGGER

- Similar concept used in the HLT
- All data from one event flow to a **single** processing node
- Requires **two layers** with passive switching network between them (Pre-processors & Main processors)

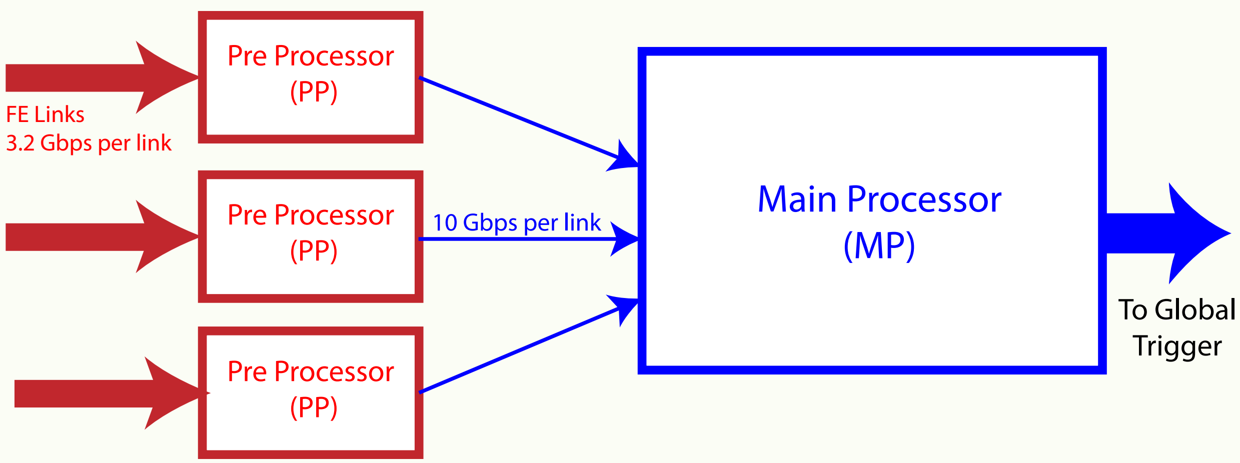


TMT ARCHITECTURE

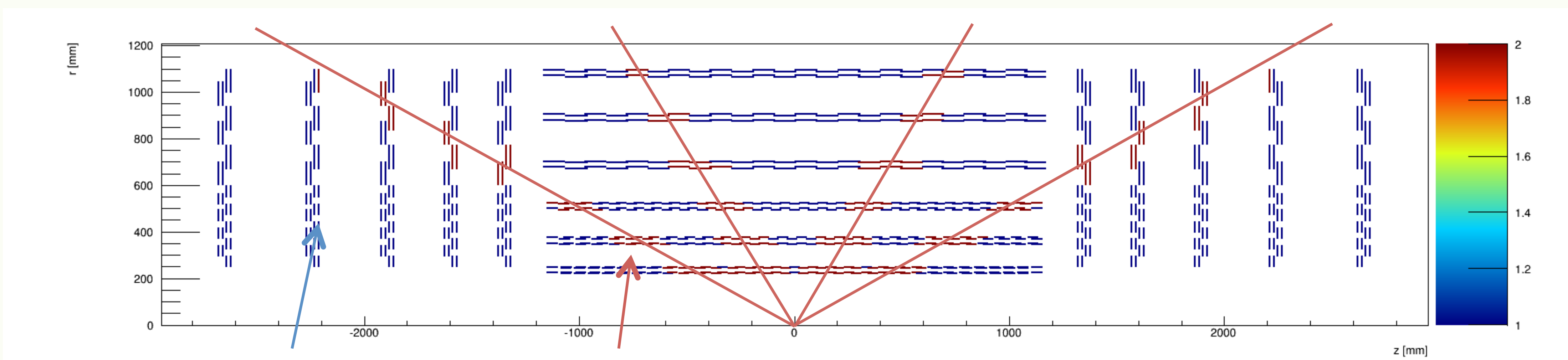


- Conceptual architecture defined using current hardware (Imperial MP7)
  - µTCA card designed for CMS upgrade L1 calorimeter trigger
  - FPGA Virtex-7
  - 72 I/O optical links (12 Gbps)
  - Total bandwidth > 0.9 Tbps

TMT ARCHITECTURE: DETECTOR MAPPING



- Maximum # links to the MP (72) limits # PP connected
- Need to divide tracker into 5 trigger regions in η (Δη ~ 1.0)



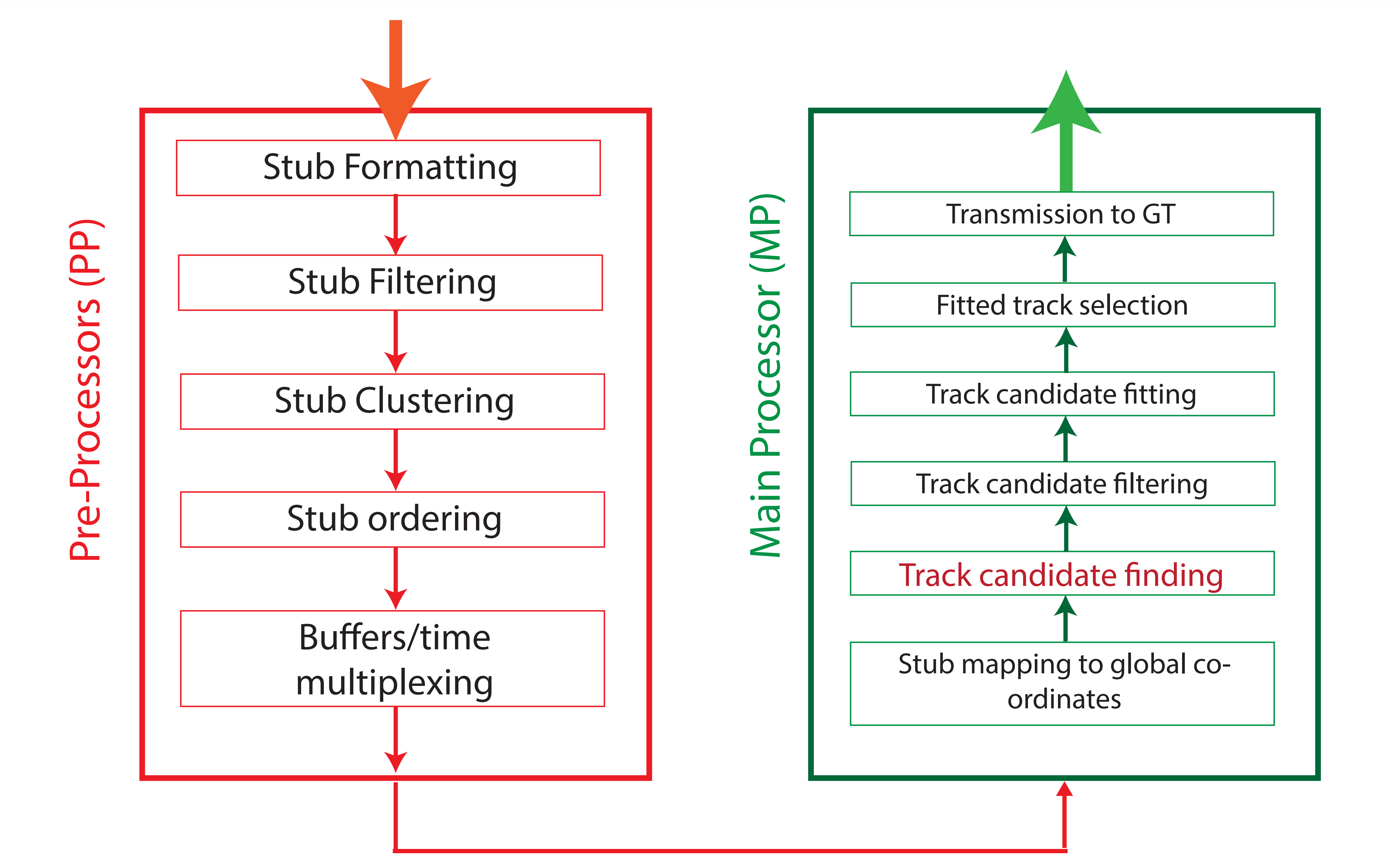
unshared modules   shared modules   TP definition (σ_z=5cm) for luminous region in z

ONE TRIGGER REGION

~ 40 unshared PPs, ~15 shared PPs (sending data to two MPs in different η regions)

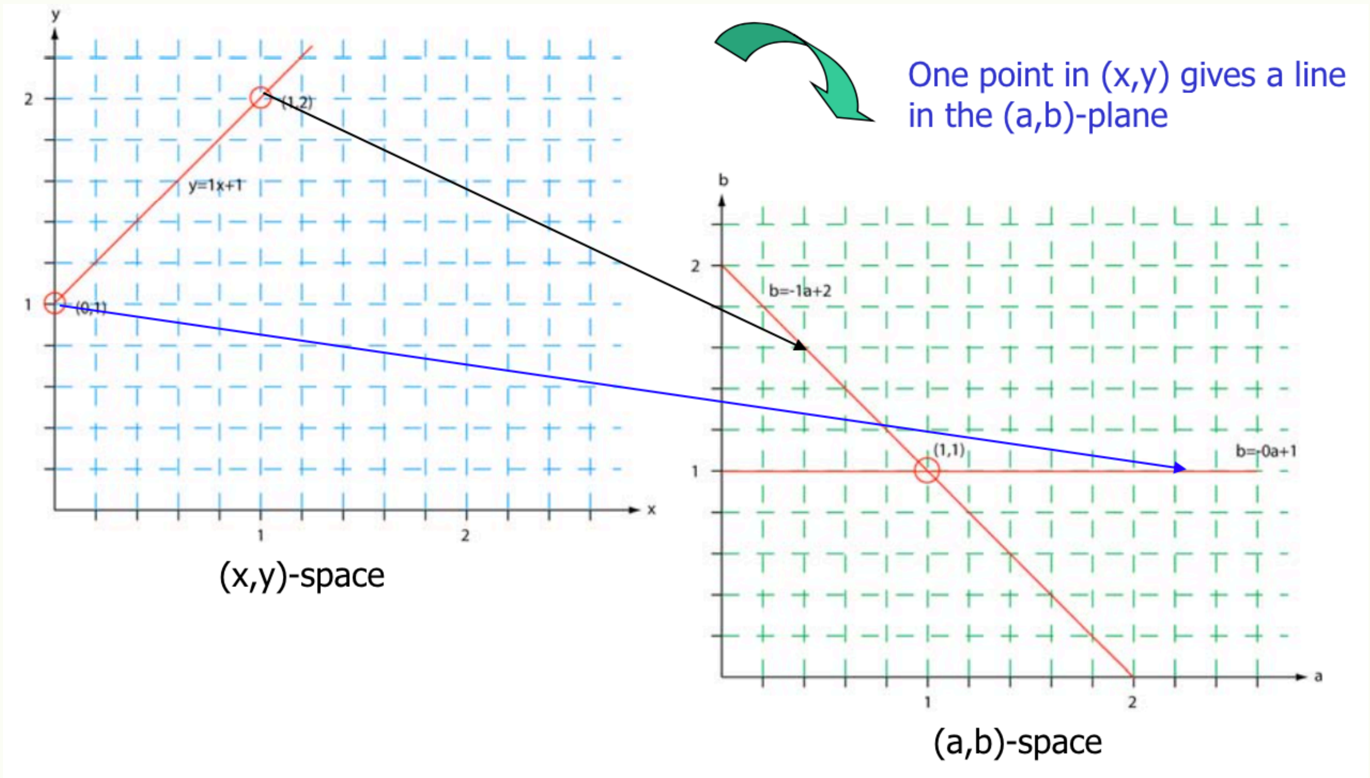
Stream data into each MP over 24 BX ➤ 24 MPs required

ALGORITHM OVERVIEW



TRACK FINDING: HOUGH TRANSFORM

- To build track candidates we proposed an approached based on the **Hough Transform**
- HT sorts stubs into candidates before selection and final track fitting



HT BASICS

Straight lines considered in terms of slope-intercept parameter (a,b)

Point (x, y) —> Line (a,b)
Line (x, y) —> Point (a, b)

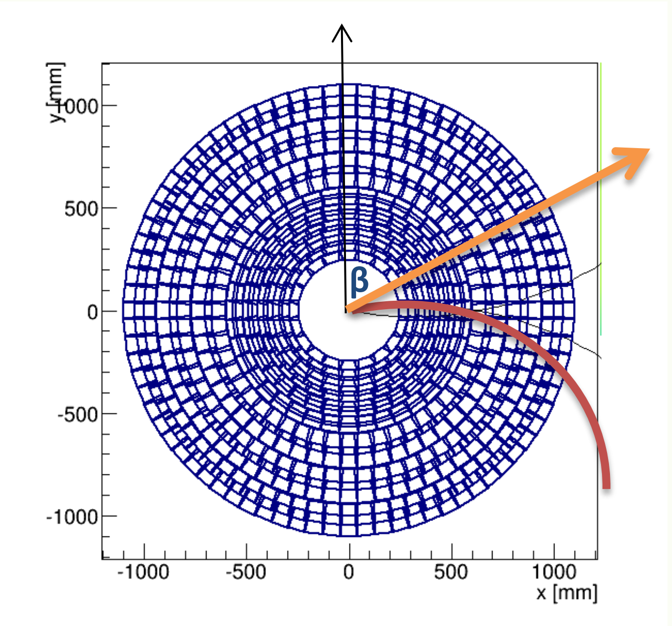
$$y = a \cdot x + b$$
$$b = -x \cdot a + y$$

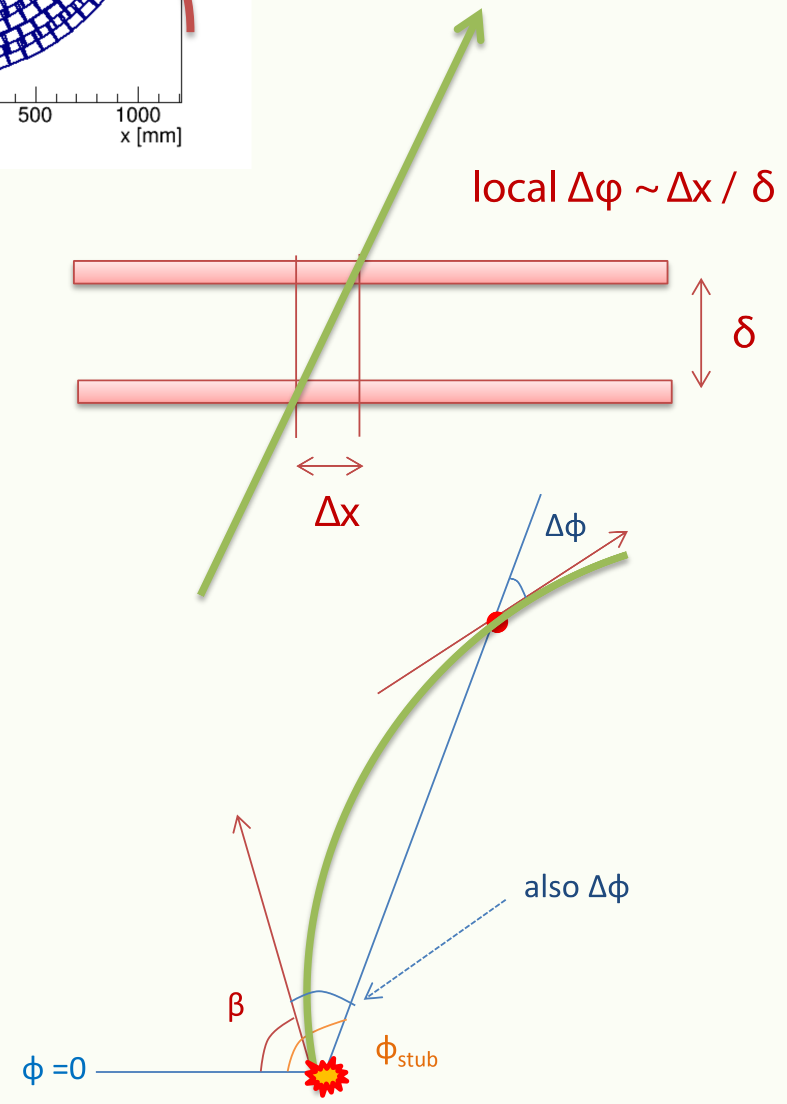
TRACK FINDING: HOUGH TRANSFORM

HT PARAMETERS

- Stub Parameter from detector
  - Φ, r; (better resolution)
- Stub coordinate transformation
  - Estimating production angle β, using angle of locally straight line
    $\beta = \phi_{stub} - \Delta\phi$
- Track Parameters in HT
  - $m = 0.006 / p_T$; $c = \beta$
    - Valid for $p_T > 2$ GeV/c

$$\phi(r) = \pm \frac{cB}{2p_t} r + \beta$$

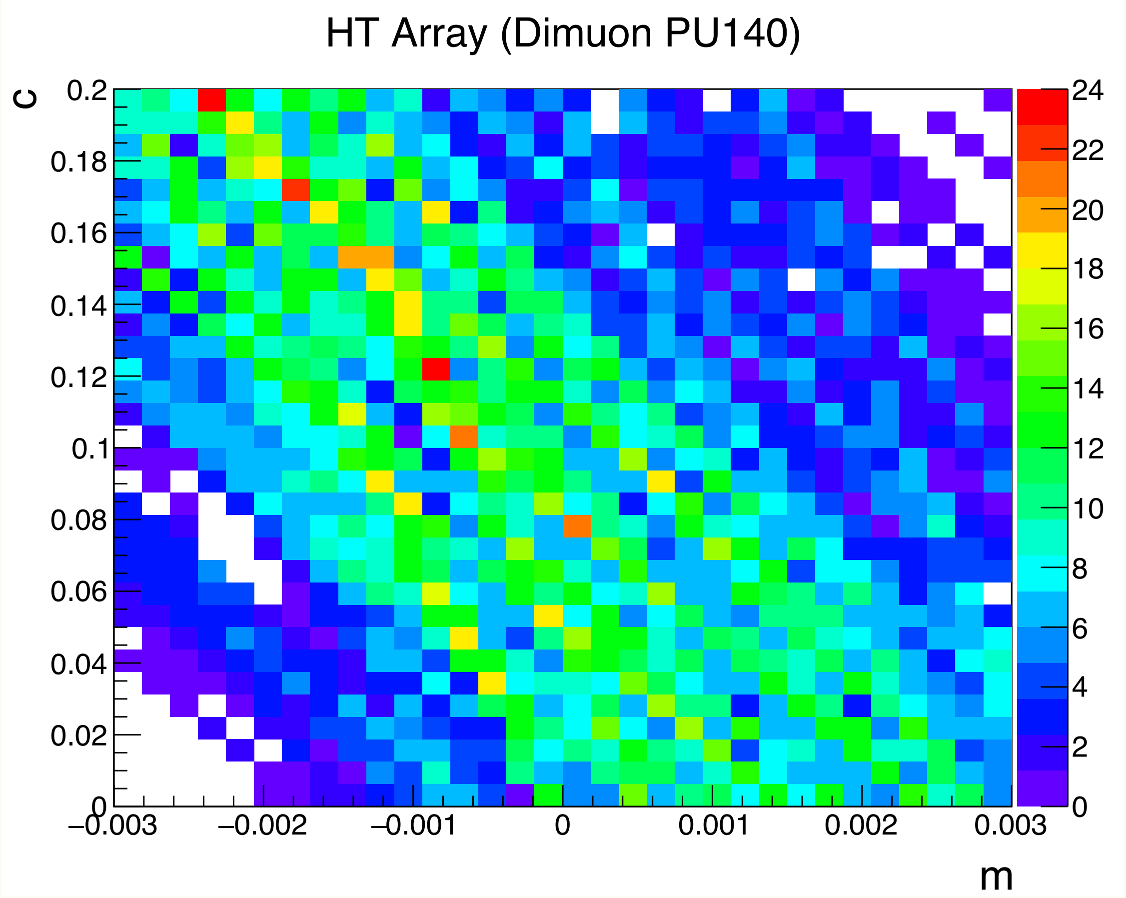




TRACK FINDING: HOUGH TRANSFORM

IMPLEMENTATION

- Each trigger region subdivided in 64 0.2 rad **β sectors**
- Hough Transform applied to each sector
- Bin stub in (m, c) space
- Arrays are filled following a **β ordering**
  - Currently evaluating alternative sorting (Φ, mixed Φ-β)



A typical filled array for one slice in β has

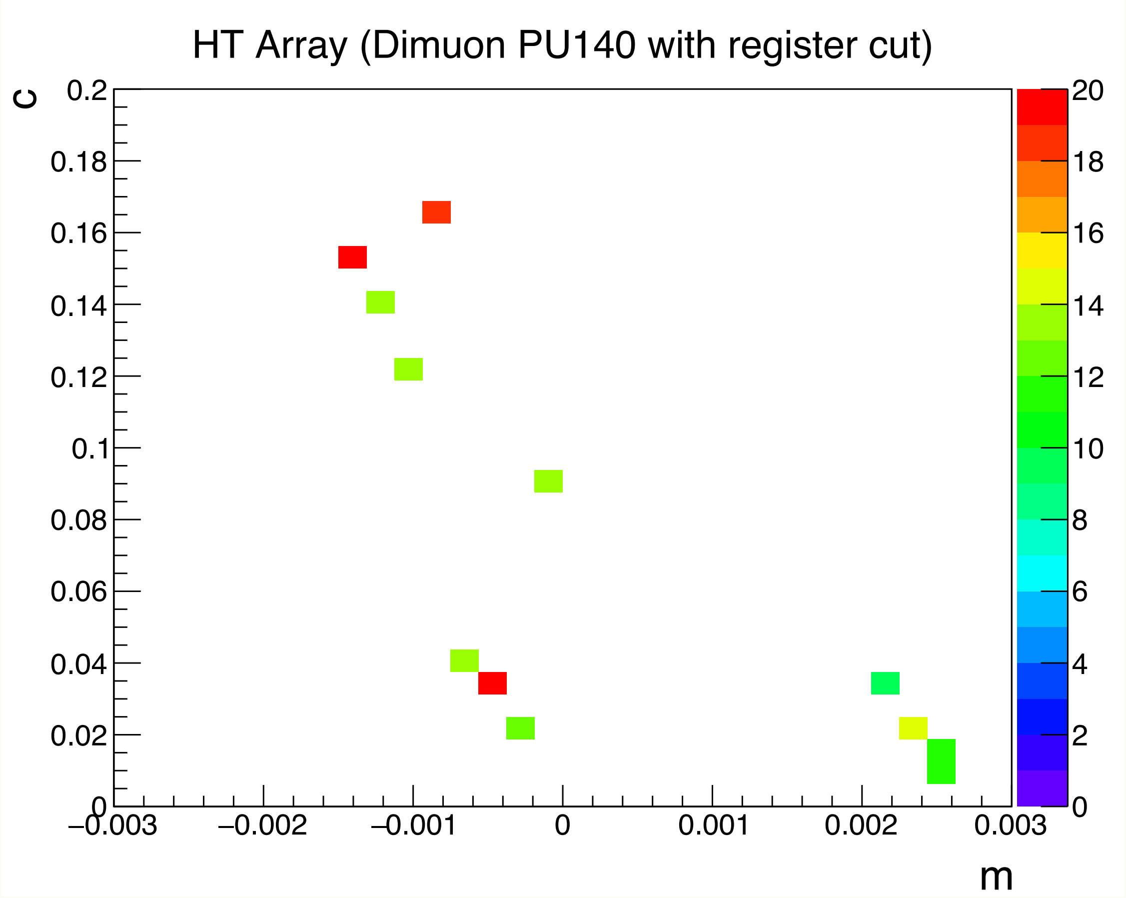
- ~ 120 stubs, each giving multiple entries
- 90% occupied cells
- 3 entries on average per cells

How can we find our tracks?

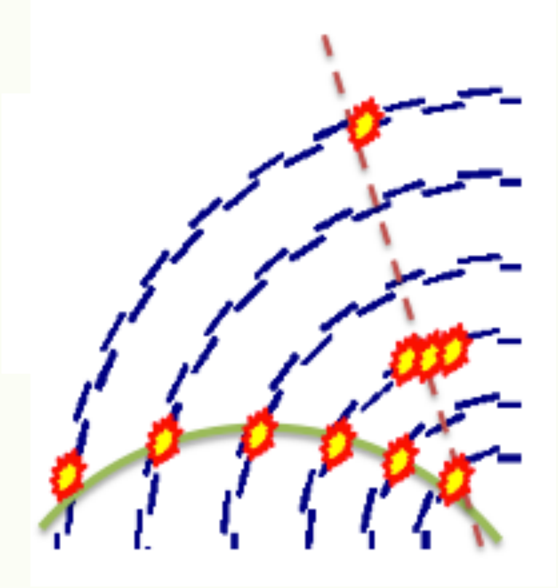
TRACK FINDING: HOUGH TRANSFORM

BACKGROUND SOURCES

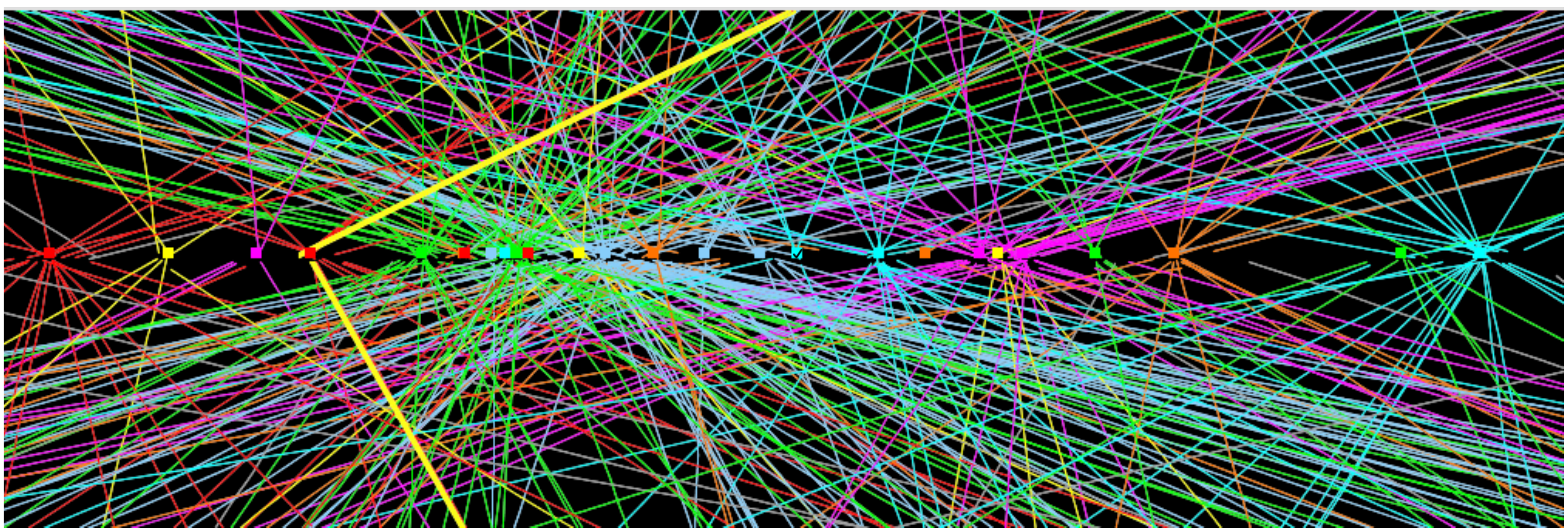
- Real tracks from PU events and secondary vertices ("secondary tracks") ➔ irreducible
- Random stub combinations, not lines in r-z projection ➔ remove in filter
  - Currently we apply two main stage of filtering, using R and η coordinates
- Correlation of PU tracks with high-p_T tracks ➔ remove in fitter



We require at least one hit in 5+ different layers/disks

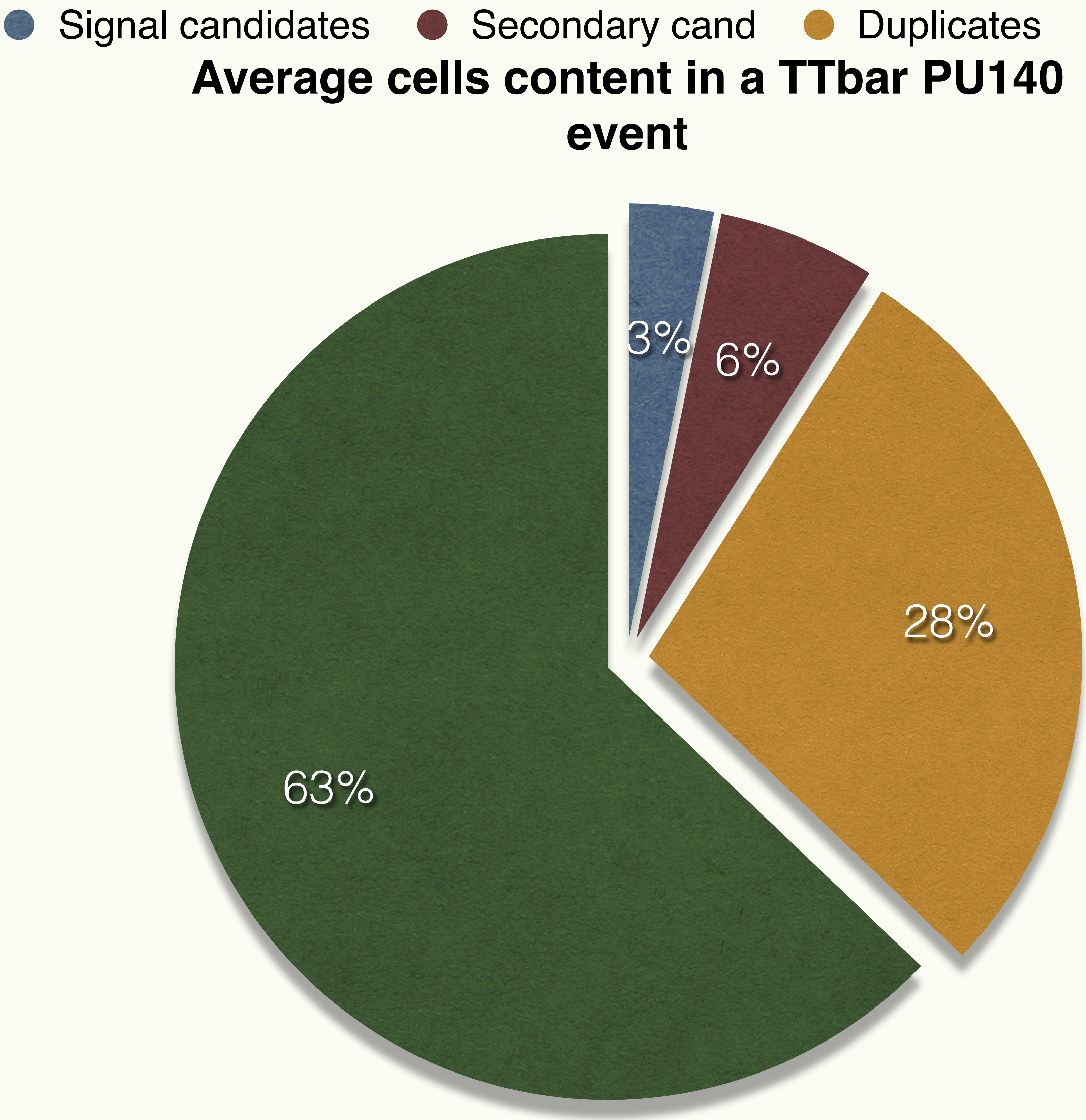


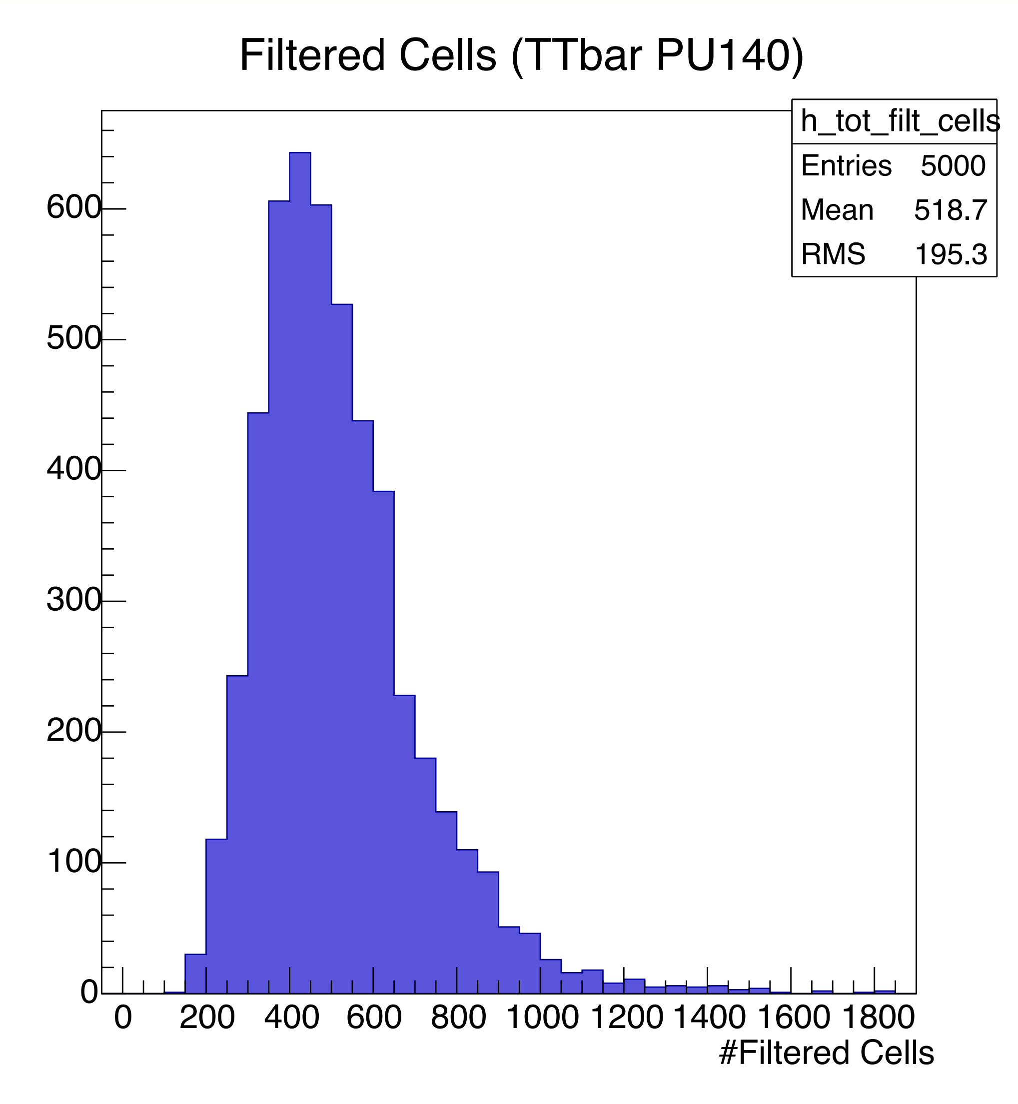
TRACK FINDING: PILE-UP



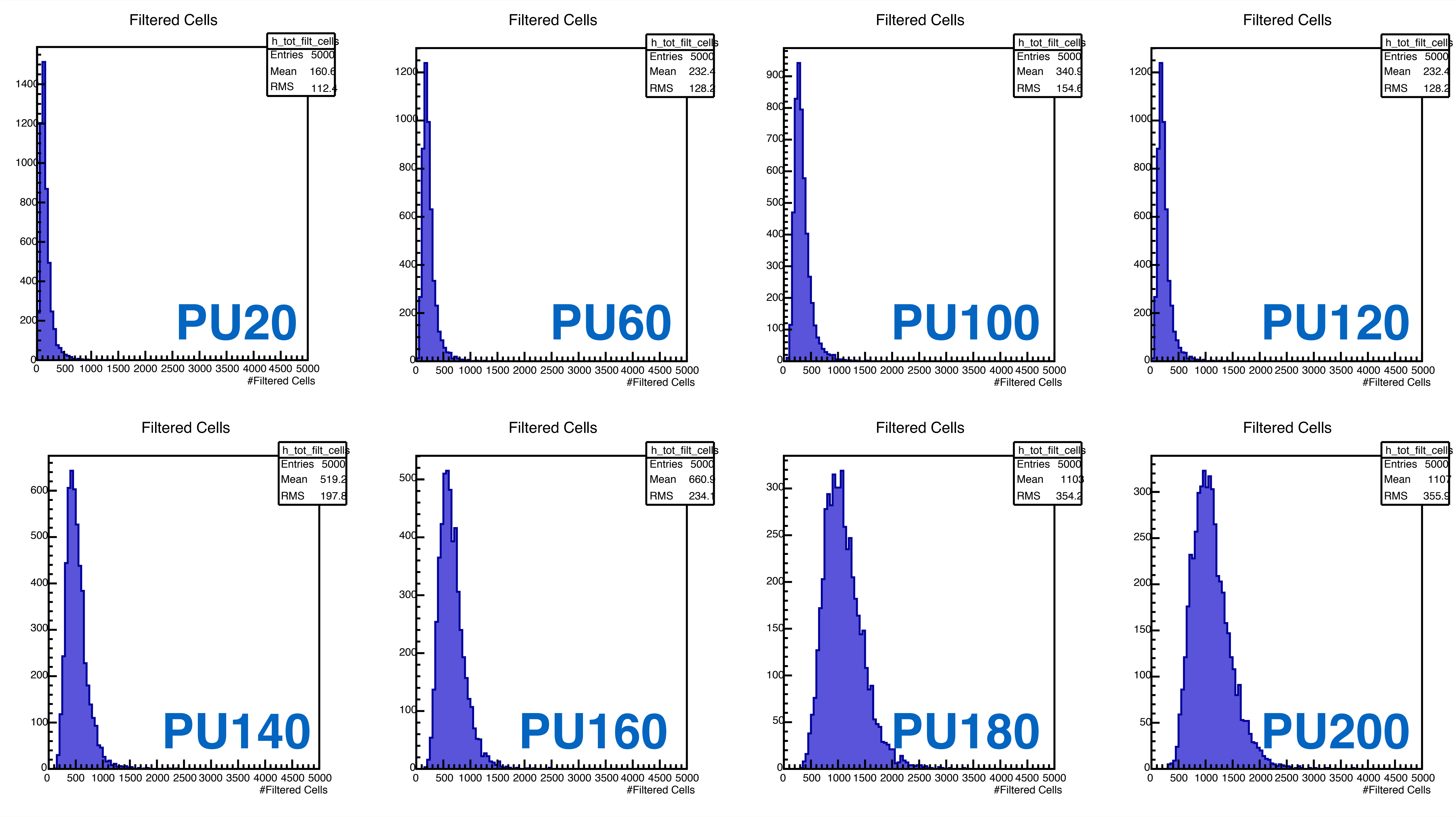
- At the High Luminosity LHC we will need to be able to work with an average of **140 pile-up** events per bunch-crossing
- The algorithm has been tested using samples with different pile-up content
- Crucial parameters are **n. filtered cells, fake rate and tracking efficiency**

TRACK FINDING: #FILTERED CELLS

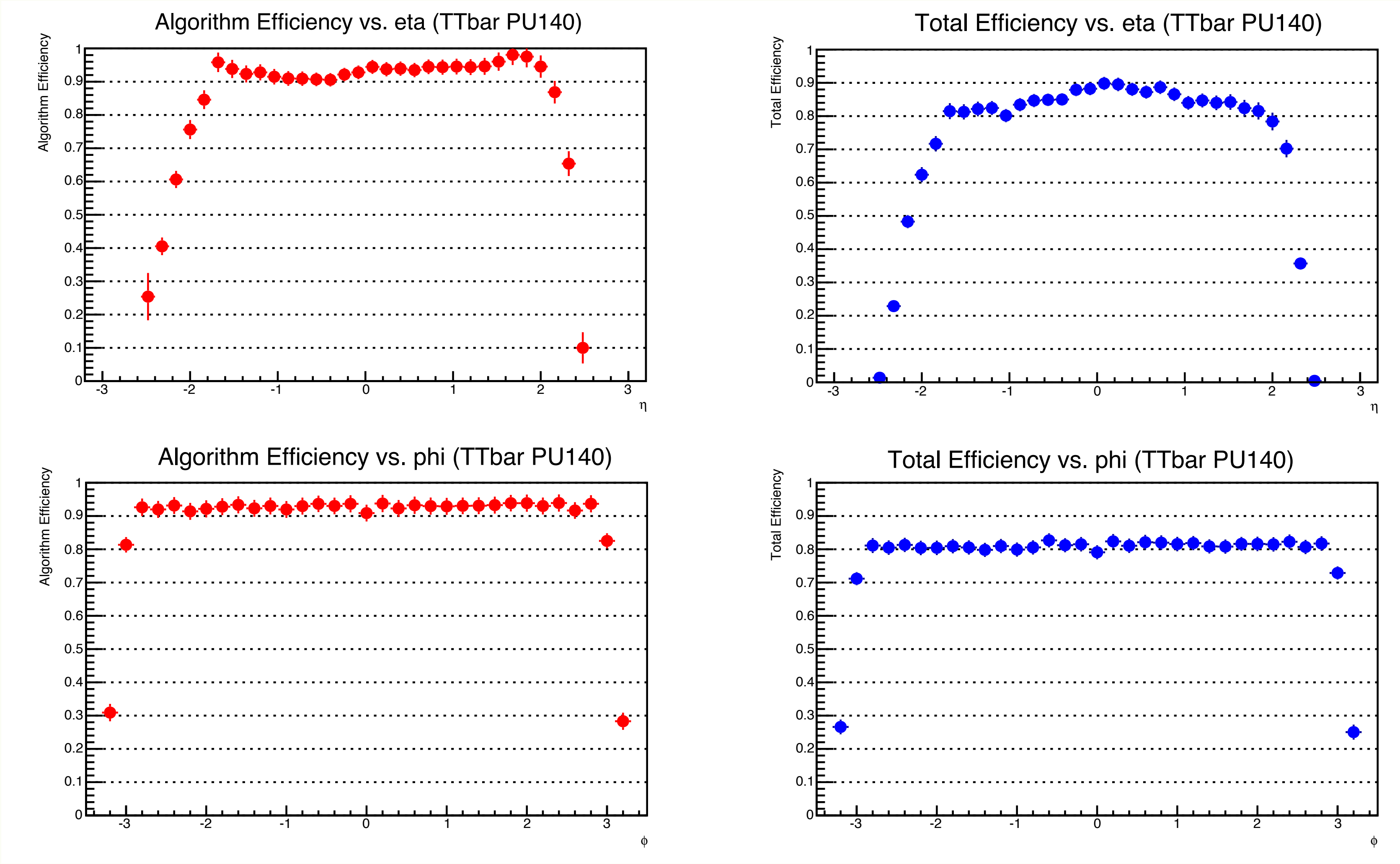




TRACK FINDING: #FILTERED CELLS VS. PU



TRACK FINDING: EFFICIENCY



- Known issues exist with **endcap-barrel** region and with ϕ boundaries
- **Improved filtering** could compensate this loss
- ϕ boundaries issue due to a coarse beta segment size definition (not submultiple of π)

ALGORITHM EFFICIENCY

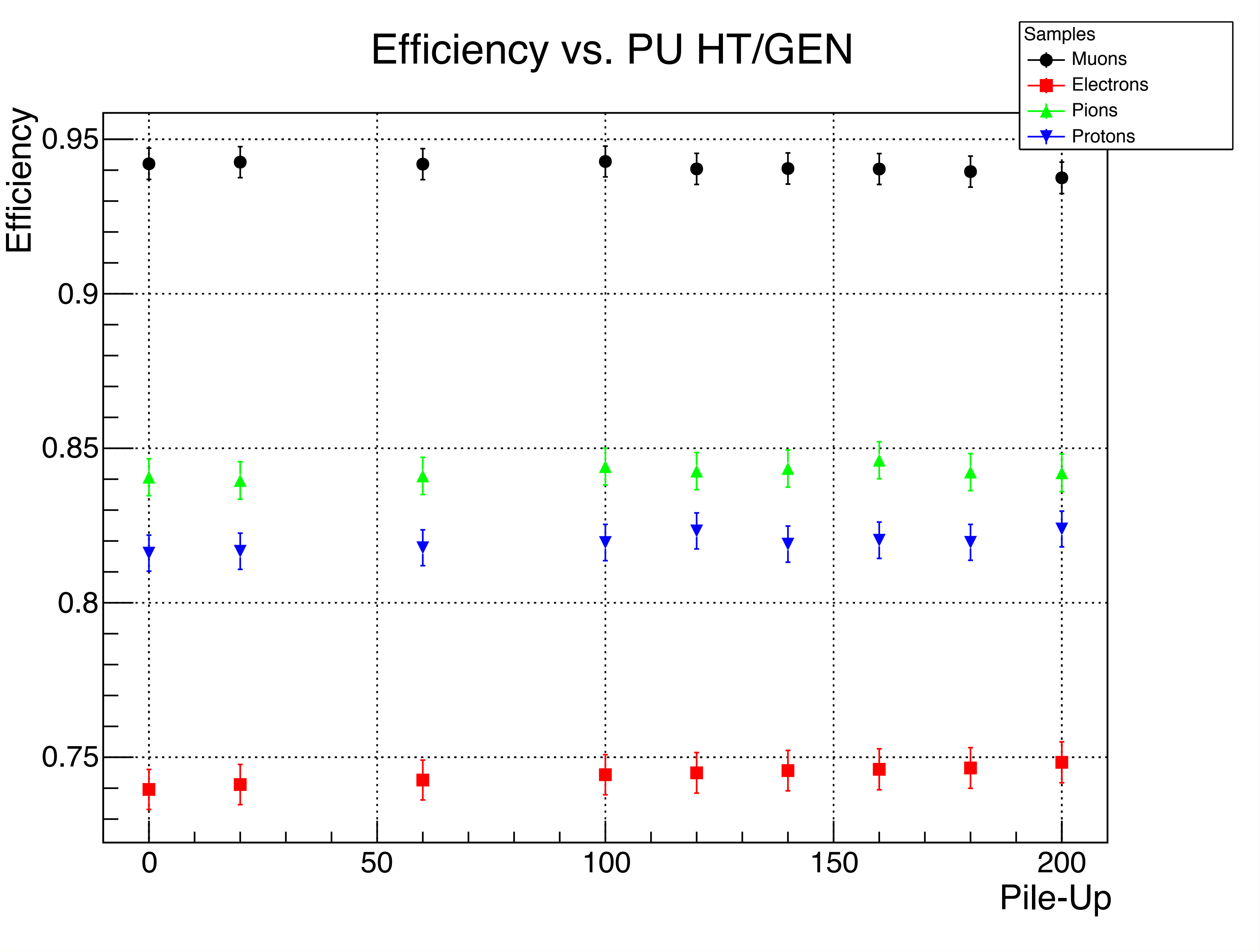
$$\varepsilon_{\text{algo}} = \frac{\text{“stable” signal tracks found by HT}}{\text{generated “stable” signal tracks passing filtering}}$$

TOTAL EFFICIENCY

$$\varepsilon_{\text{tot}} = \frac{\text{“stable” signal tracks found by HT}}{\text{total generated “stable” signal tracks}}$$

* Charged particles that can pass through the whole tracker before decaying are considered “**stable**” (K, p, e, μ, π)

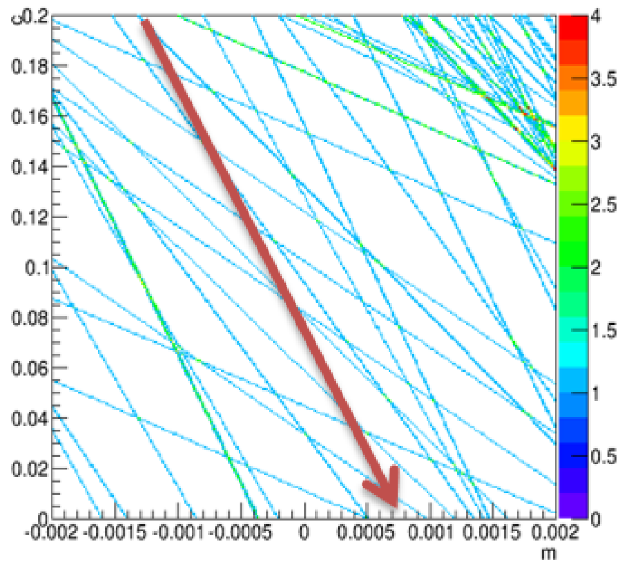
TRACK FINDING: EFFICIENCY VS. PILE-UP



- Algorithm **not strongly** affected by PU
- Low electrons efficiency mainly due to **Bremsstrahlung**
- May be a possibility to recover this by special binning for very high pt stubs

$$\varepsilon_{tot} = \frac{\text{“stable” signal tracks found by HT}}{\text{total generated “stable” signal tracks}}$$

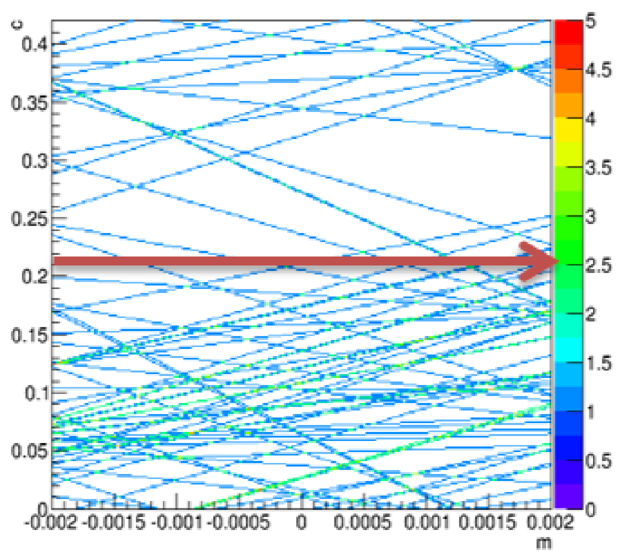
IMPLEMENTATION: DATA FLOW OPTIMISATION



Old Hough Transform

$c = -m*r + \phi$

← average direction of dataflow



New Hough Transform

$c = m*(r - 65) + \phi$

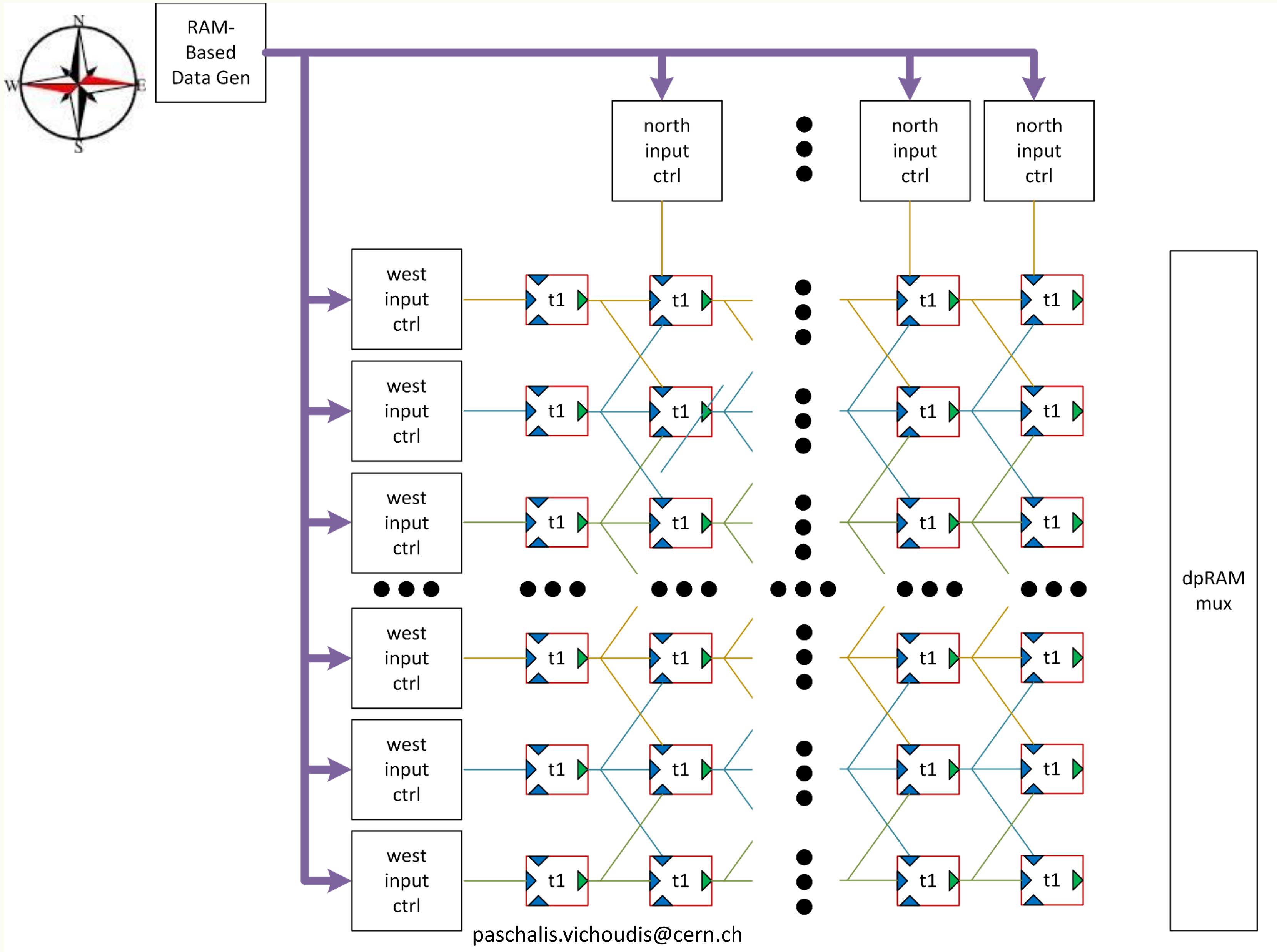
minus not important (flips m axis about 0), and we only care about intersection

equivalent to transposing the detector 'axis' to r = 65cm

required to distribute the stubs uniformly over the array, and balance dataflow from left to right

Other optimisations are currently under investigation

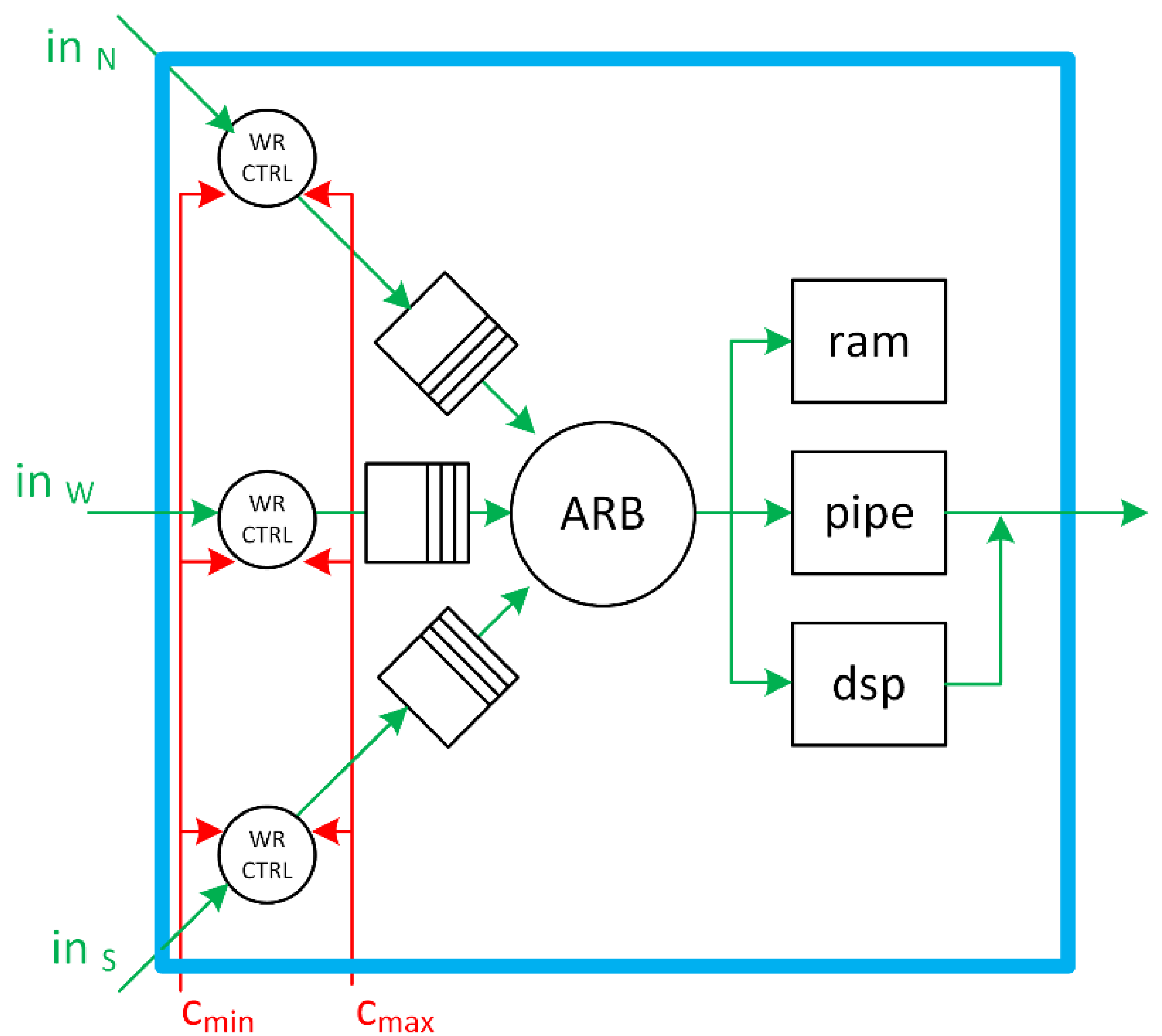
ARRAY IMPLEMENTATION



ARRAY CONCEPT:

- **eastbound traffic**: the stubs move towards east
- **two entry points:** west and north (sorting mechanisms)
- **cell readout condition:** when stub entries with at least 4 (or 5) different r values (corresponding to different detector layers)

CELL IMPLEMENTATION



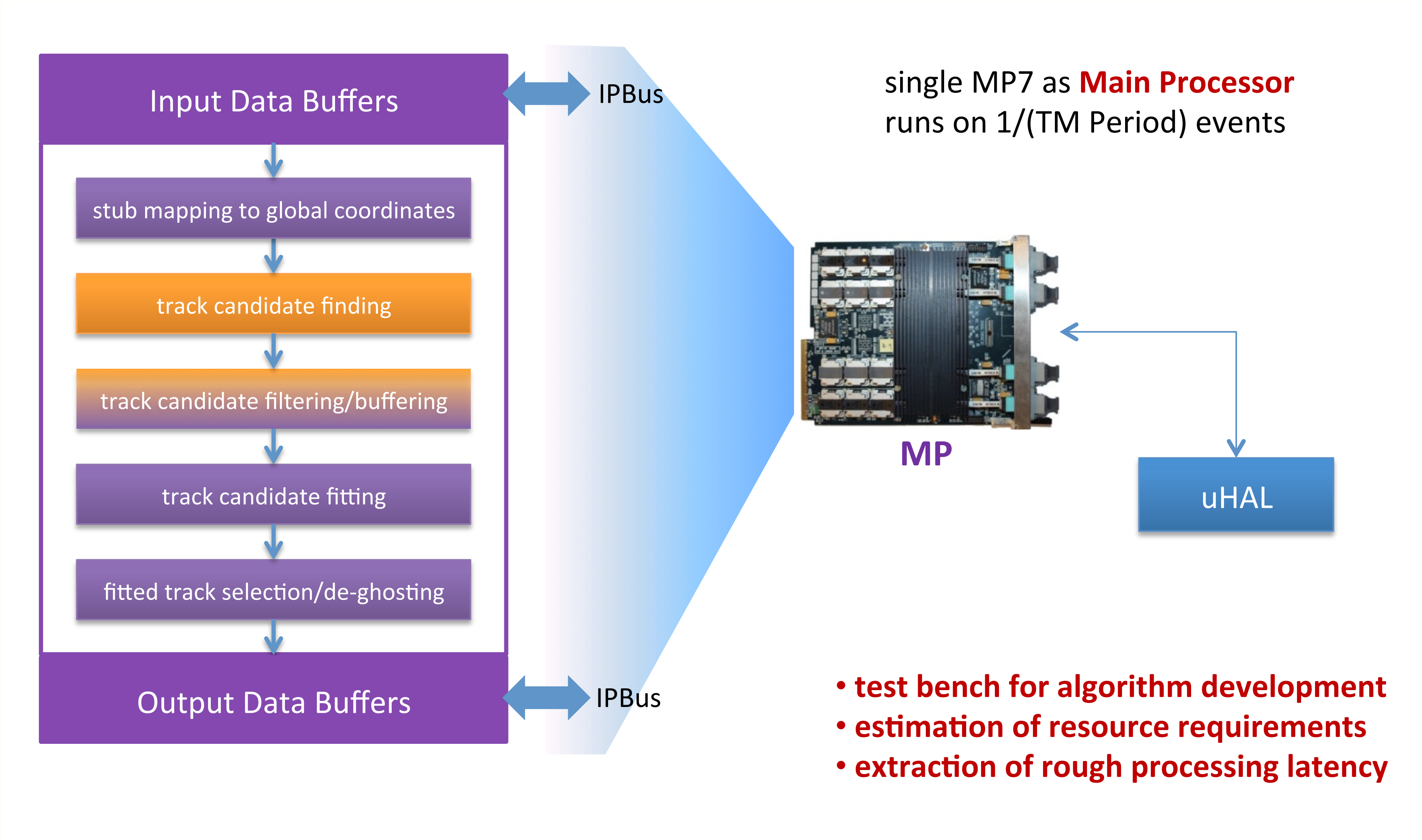
SYSTOLIC ARRAY FUNCTION

- Stubs enter at N, S and W sides
- Stubs automatically propagate eastwards through the matrix
- Various ‘routing methods’ under study

IMPLEMENTATION STATUS

- 25x25 array implemented in MP7
- Splitting across multiple FPGAs is straightforward to reach 32x32
  - Intrinsic strength of architecture
  - Future devices likely to be be multi-die

DEMONSTRATOR: SHORT TERM PLAN

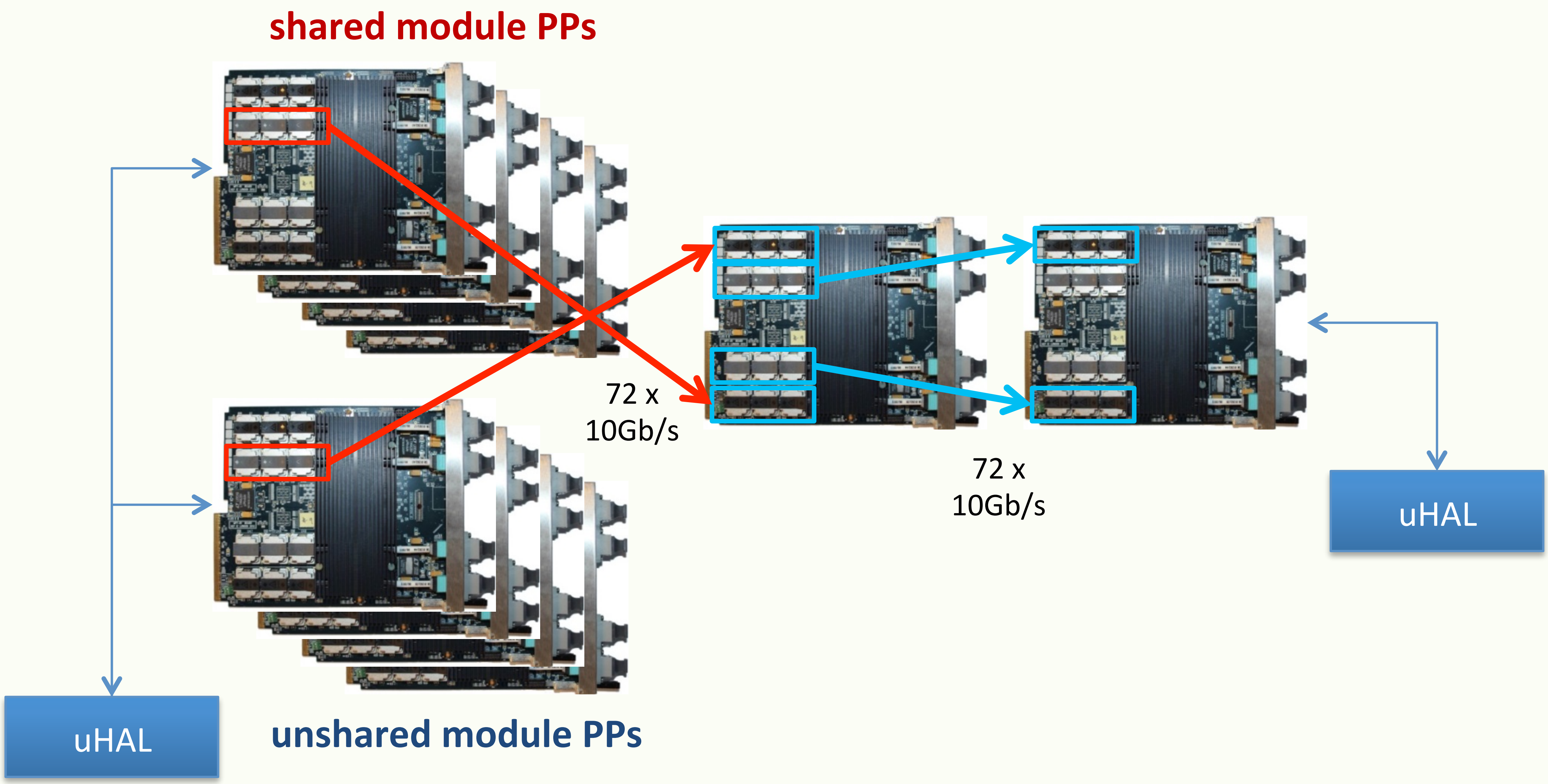


Working operation of a single MP (aka one subsegment) will be tested

- Including interface to PP (10~12.5 Gbps protocol block)
- Time-schedule: July 2015 for single board, September for multi-board

More technical details on the demonstrator in Aaron's talk

DEMONSTRATOR: LONG TERM PLAN



Expanded system for track filter/fitter testing

- Emulate a whole trigger segment, planned for late 2015

More technical details on the demonstrator in Aaron's talk

THE FUTURE

SIMULATION

- Continue **tuning** and optimisation of **Hough transform** algorithm
- Develop r-η **track filter** algorithm and specify interface to **track fitter**
- Look further into **electron/hadron** efficiencies
- Code is currently rewritten to have a more **modular structure**

IMPLEMENTATION

- Complete 32x32 array demonstrator
- Develop CMSSW **emulator** for TMT track finder
- Three way comparison: **CMSSW** ⟷ **VHDL simulation** ⟷ **hardware test**

DEMONSTRATION

- **Single board** testing expected during the Summer
- Full **multi-board** demonstrator data by September 2015
- Bring in **filter and fitter** for complete slice test by end of 2015

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THANKS!

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