Development of the ATLAS Insertable B-Layer and New Pixel Developments

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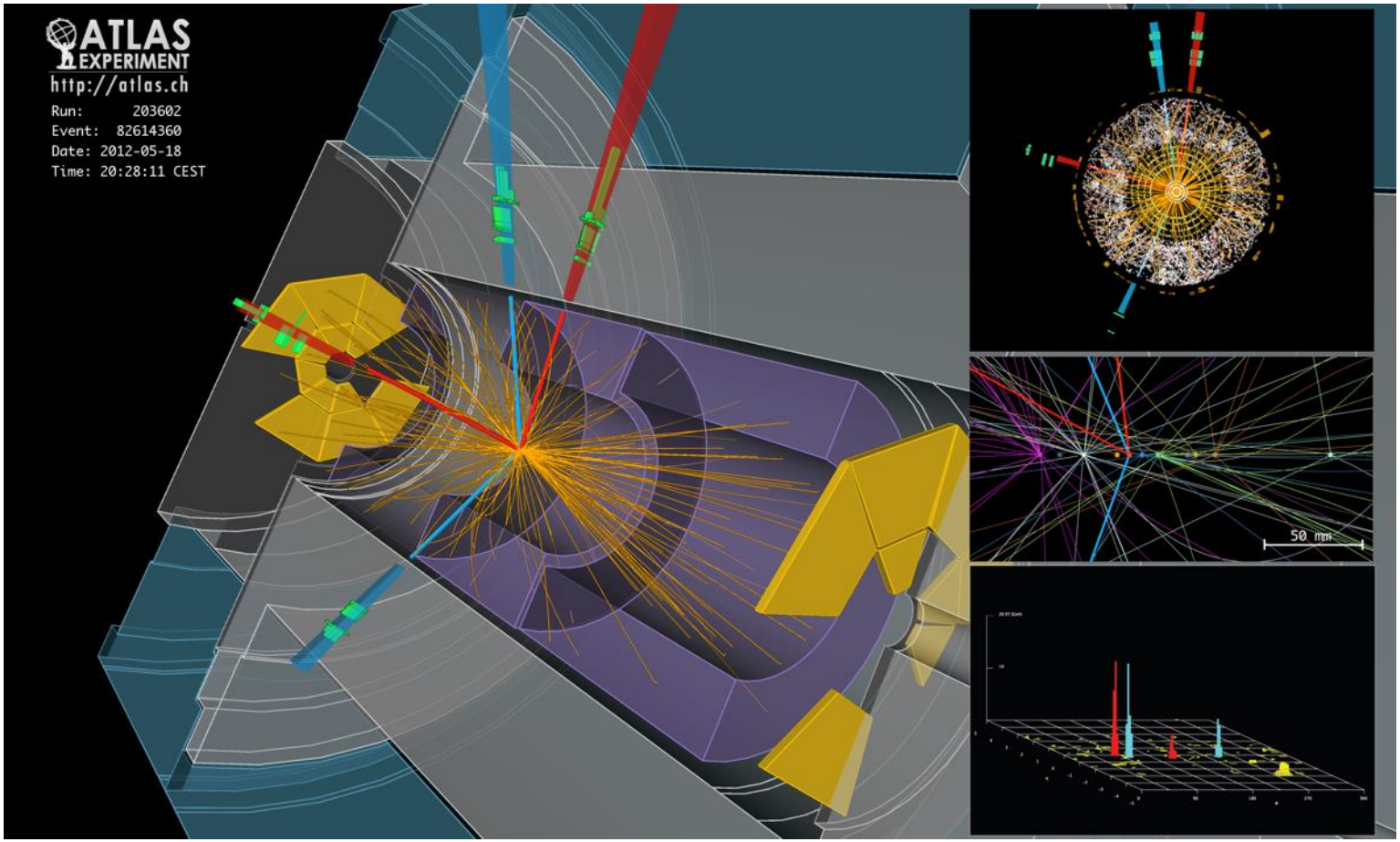
Outline

- State-of-the-art Pixel Detectors
  - what they do and how they do it
  - From design to development
- The new ATLAS 4-Layer pixel detector
  - What are the key technologies
  - Experience in the construction of the new detectors
  - Ready for the next LHC Run
- What are the future trends

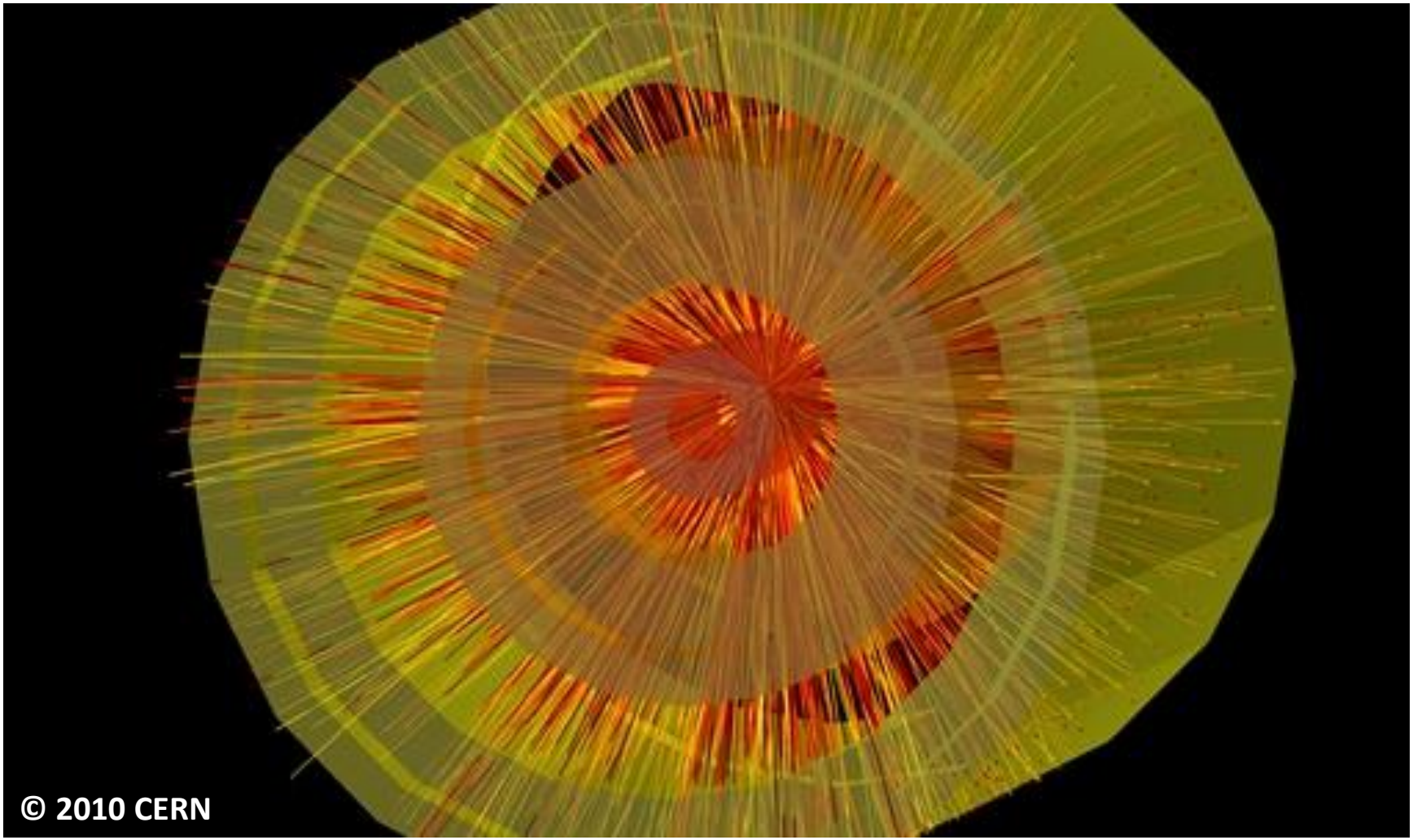
Reconstruct Tracks in pp collisions



ATLAS Experiment © 2012 CERN

Event display of a H -> 4e candidate event

… or lead-lead collisions at LHC

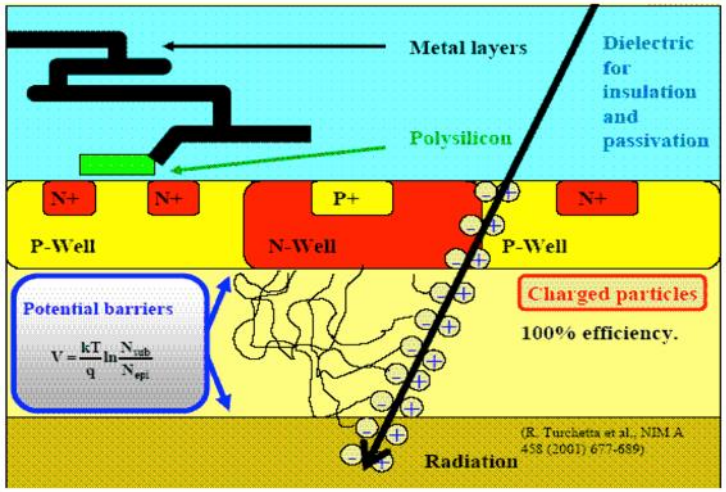


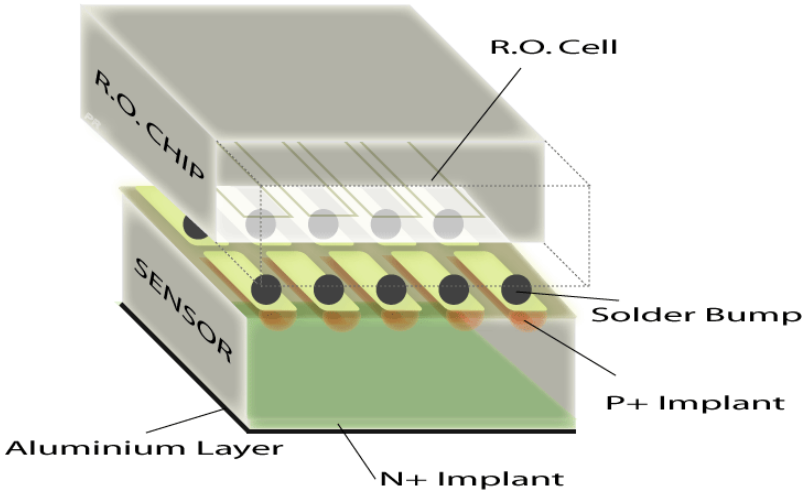
Events recorded by the ALICE experiment from the first lead ion collisions, at a centre-of-mass energy of 2.76 TeV per nucleon pair.

…and do this well!

- Pixel detectors are the first measurement layers after the beam pipe
- Their goal is
  - Reconstruct charged particle tracks & provide momentum resolution
  - To reconstruct primary and secondary vertices
  - Identify individual collisions through reconstruction of multiple primary vertices
  - Provide b-tagging
  - Reconstruct tracks in jets
- Used in ATLAS, CMS, ALICE and soon in LHCb

The "World of Pixels" …





Monolithic Pixels

- Charge generation volume integrated into the ASIC

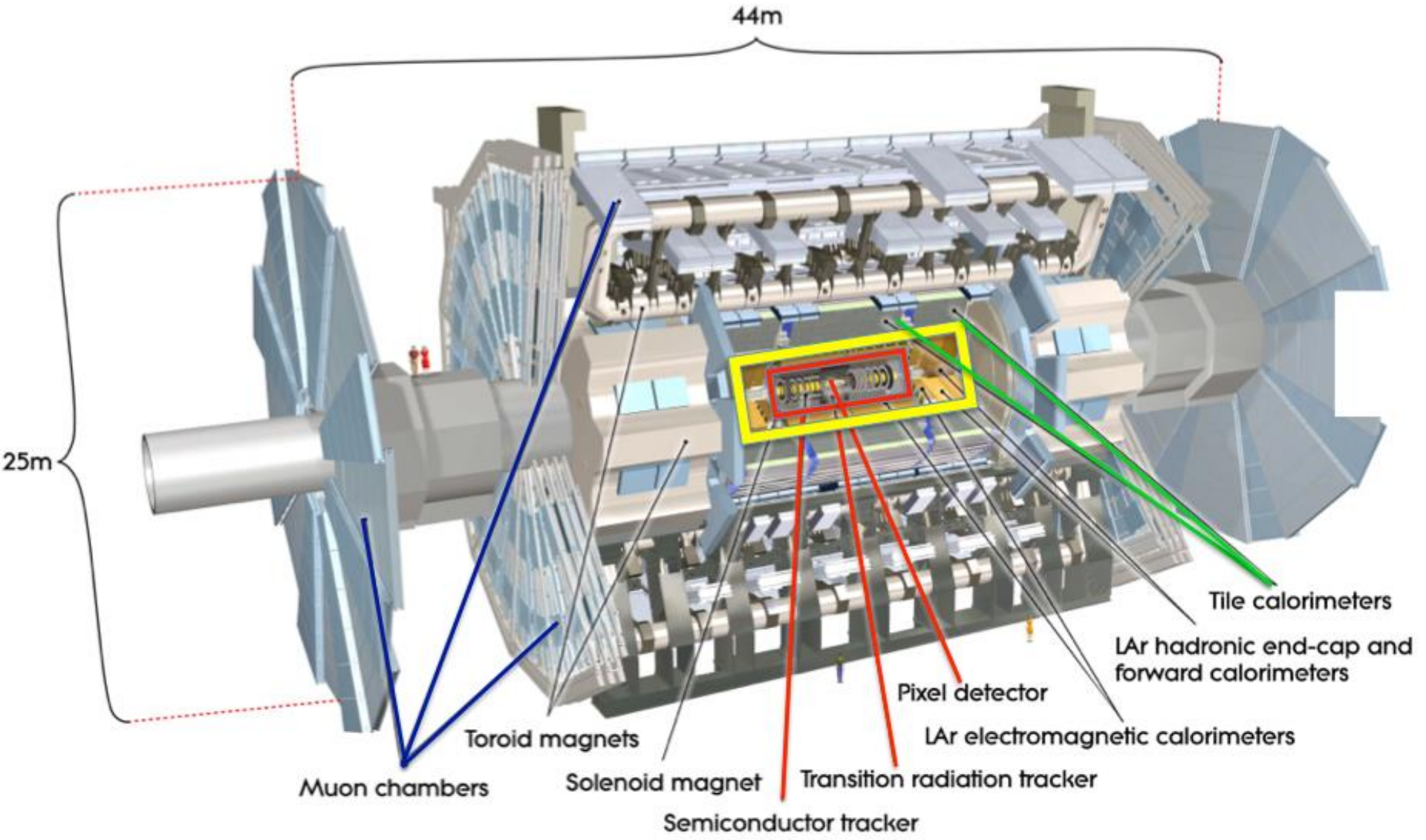
- **Used in ALICE ITS upgrade**
- Thin, sensor+FE in 1 chip, high resolution, not radiation hard

Hybrid Pixels

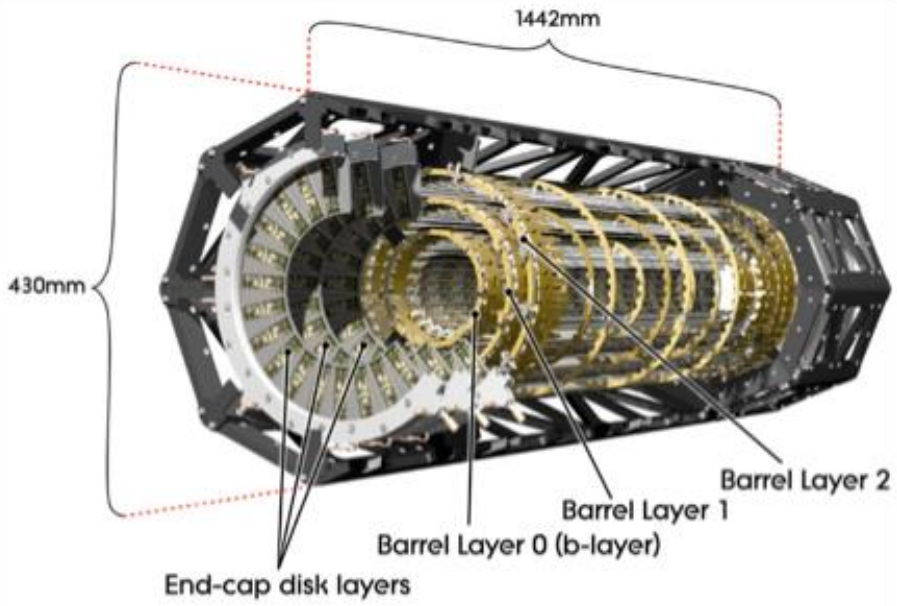
- Sensor and ASIC are independent units

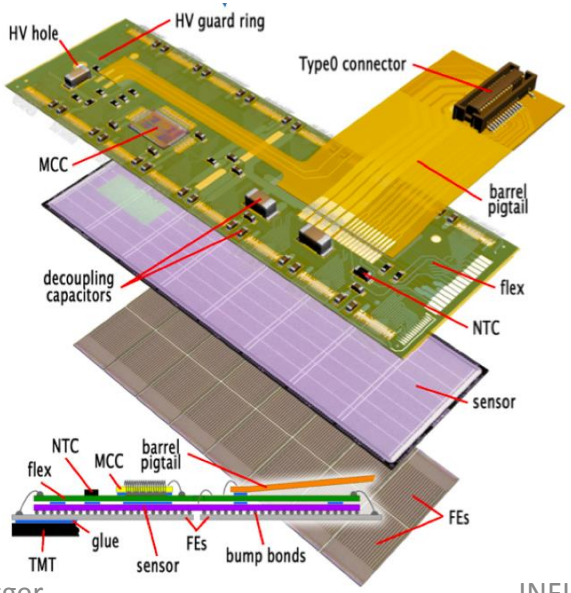
- **Used in ATLAS and CMS pixel detectors**
- Fast, radiation hard, fast readout but thicker and complex assembly

The ATLAS Detector



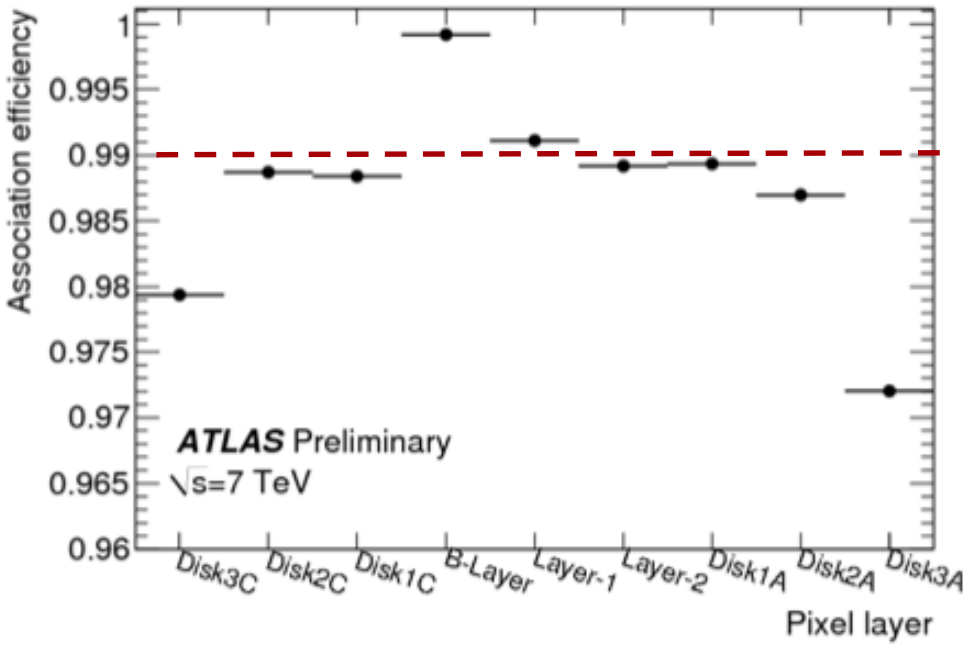
ATLAS Pixel Detector in Run 1





- The ATLAS Pixel Detector in a glance
  - 1744 modules and 80M readout channels
  - 1456 in three layers of barrel region 288 in three layers of end-cap regions
- High resolution
  - 8 μm in Rφ
  - 75 μm in z
- Module operation at -13 °C
  - Evaporative C3F8 cooling
- The ATLAS Pixel Module
  - Sensor is 250 μm thick n-in-n silicon sensor
  - 47232 pixels (typical size 50x400 μm2)
  - Active area of 16.4x60.8 mm2
- Module controller chip (MCC)
- Readout by 16 FEI3 chips (2880 pixels each) for each sensor - Data transfer 40-160 MHz depending on layer

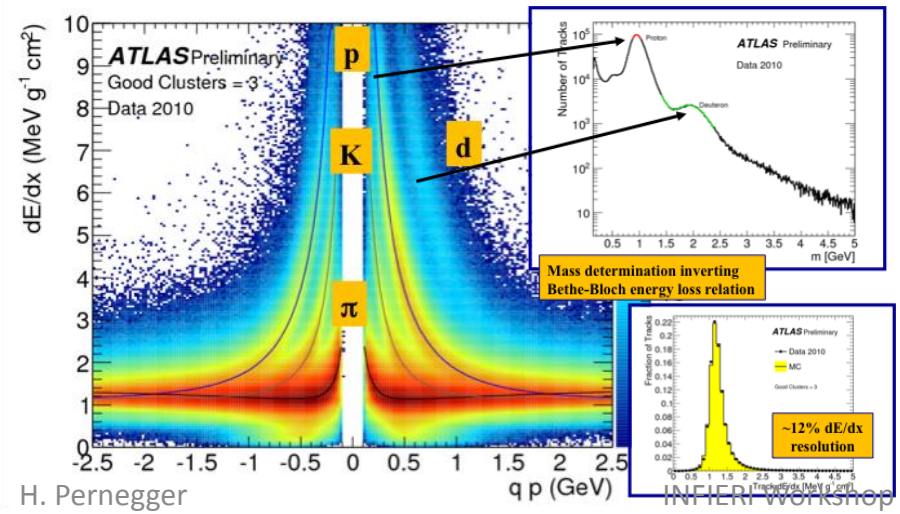
Pixel detector efficiency



Hit-to-track association efficiency for the different parts of the detector.

Disabled modules have been excluded, dead regions not (Full efficiency of the B-layer due to track selection).

Efficiency ~99% for nearly all parts
Slightly lower efficiency in the outermost discs due to inefficient regions on some modules.



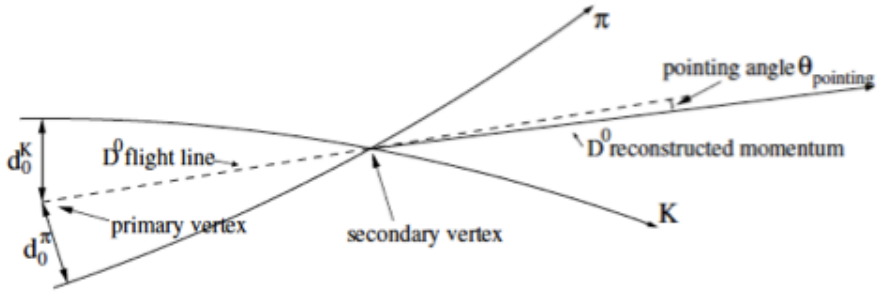
Bi-directional distribution of dE/dx and momentum.

The charge collected in each pixel is measured using the TimeOverThreshold information.

Thanks to the stability of the detection process, it allows the identification for non relativistic particles.

Impact parameter

- Secondary vertices reconstruction strongly depends on impact parameter resolution
  - d0 in r/phi (bending plane)
  - Z0 alone beam direction



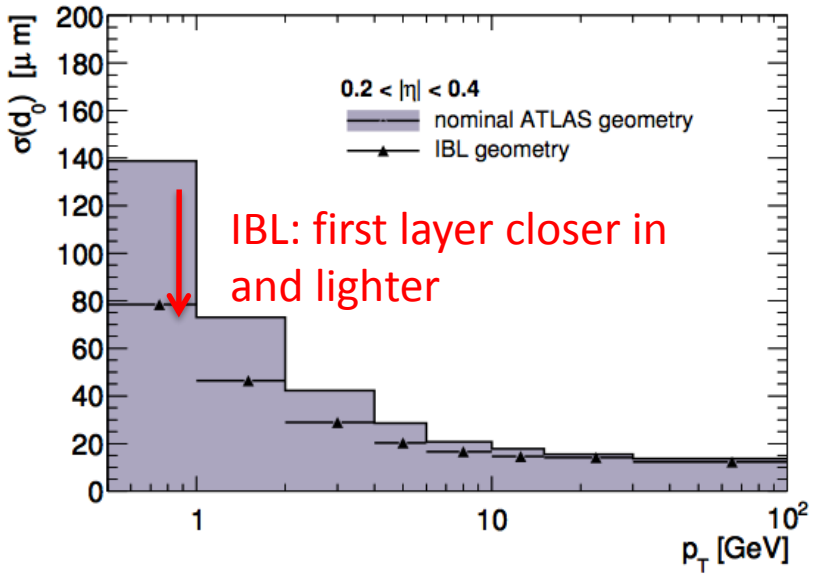
- Impact parameter resolution is strongly effected by
  - Intrinsic point resolution and alignment at higher momentum
  - Multiple scattering in detector material (in particular for low pt tracks)

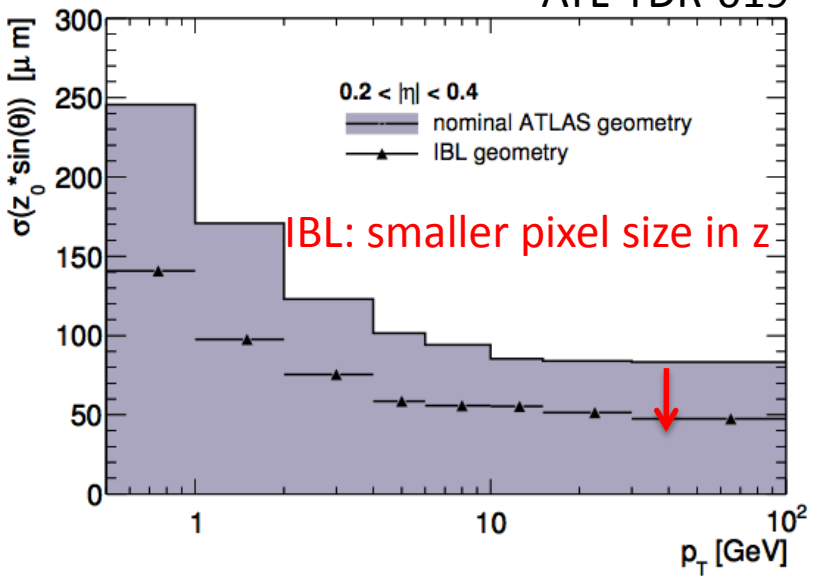
- Excellent impact parameter resolution is mandatory for reconstruction of heavy flavor vertex (c and b vertex)

How to improve the system for the future?

- Vertex reconstruction is very sensitive to the first layer – therefore make the first layer
  - Light ! (low multiple scattering using light supports and thin detectors)
  - High resolution ! (smaller pixel size)
  - Bring it close to the collision point -> minimal beam pipe diameter and highly integrated system
- ATLAS has done this in the last 4 years with the construction of the **"Insertable B-Layer (IBL)"** which now makes the ATLAS Pixel detector a 4 Layer system - Significant improvement in impact parameter resolution:

ATL-TDR-019



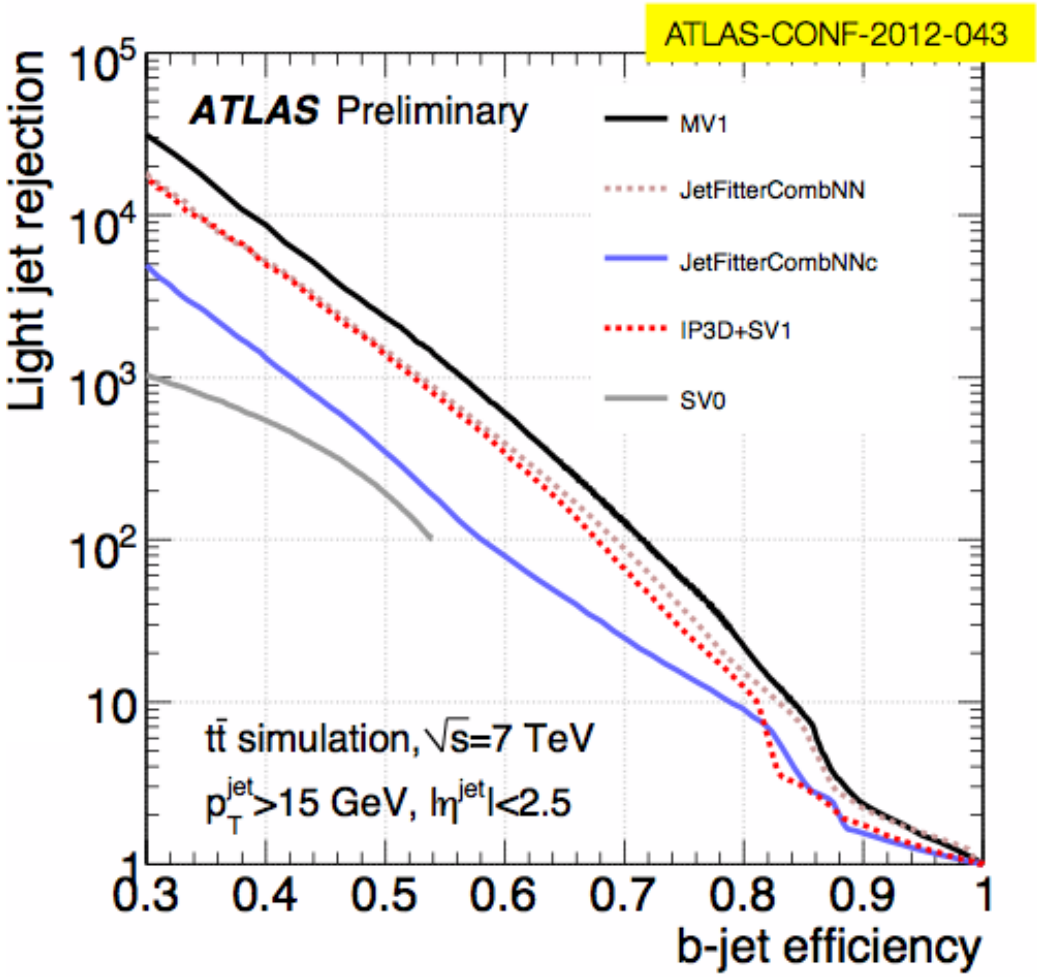


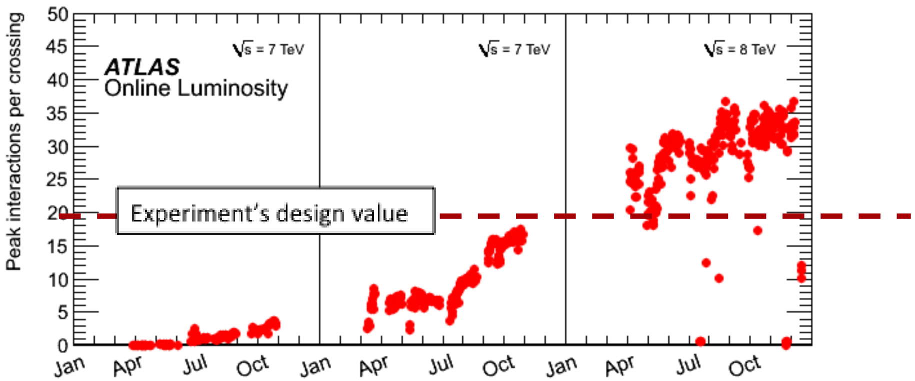
B-tagging

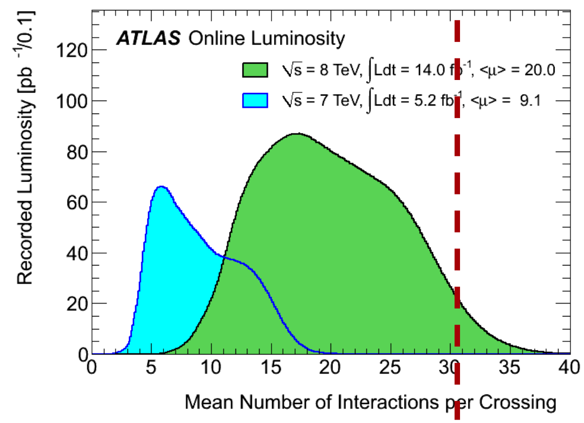
- Tagging b-jets is important for many analysis like Higgs (H->bb), top(t->Wb), SUSY/Exotics ($\chi 1 \rightarrow \chi_2 b$)

- B-tagging efficiency measures the efficiency with which a jet originating from a b-quark is identified AND an algorithm rejects jets from lighter quarks

- BUT…

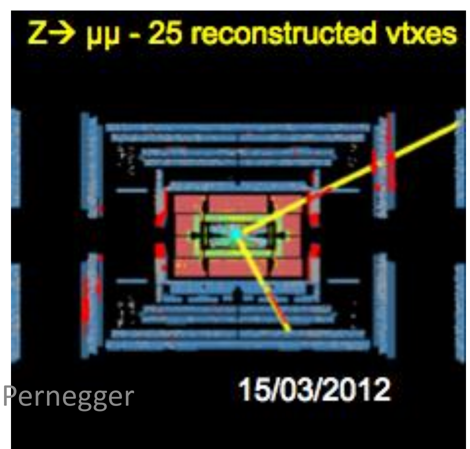


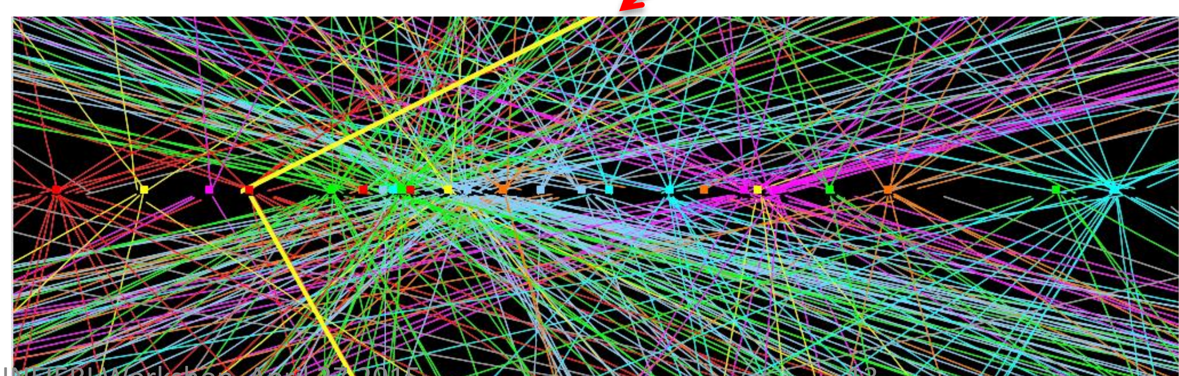




LHC reached design luminosity and will exceed it in cooling years up to instantaneous luminosity of 3×10^{34} $cm^{-2}s^{-1}$. Currently >30 collisions are superimposed in each bunch crossing every 25ns. For the next years this will reach 80-100 and at HL-LHC up to 200. **At HL-LHC this means that collisions are spaced at <1mm from each other**

You need a pixel detector with really good pattern recognition to disentangle that! Get more layers!

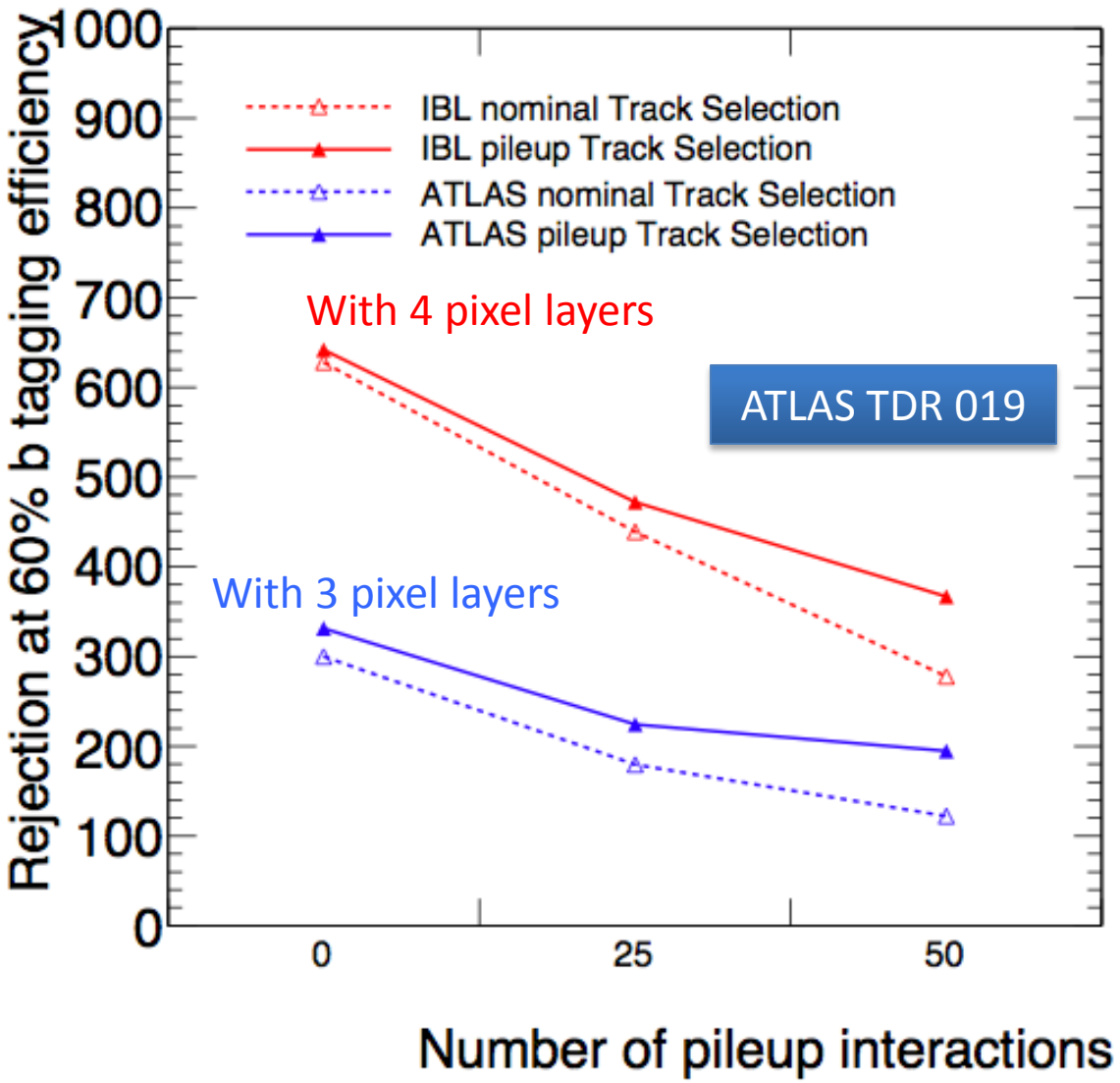




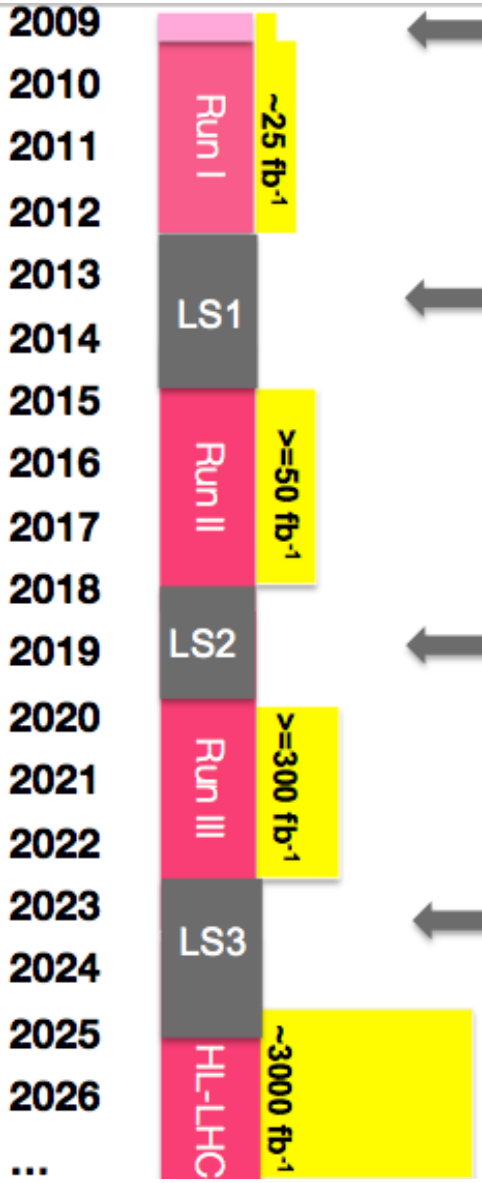
Z → μμ event with 25 reconstructed vertices.

B-tagging with pileup

- Light jet rejection at 60% b-tagging efficiency as function of pile-up events
  - Up to ~2 x 10^{34} $cm^{-2}s^{-1}$
- IBL improves rejection substantially at high pile-up



LHC time line



LHC startup, $\sqrt{s}$= 900 GeV
$\sqrt{s}$=7~8 TeV, L=6×10^{33} cm^{-2} s^{-1}, bunch spacing 50 ns, μ<40

Go to design energy, nominal luminosity
$\sqrt{s}$ = 13~14 TeV, L ~ 1×10^{34} cm^{-2} s^{-1}, bunch spacing 25 ns
μ<40 **Phase-0**

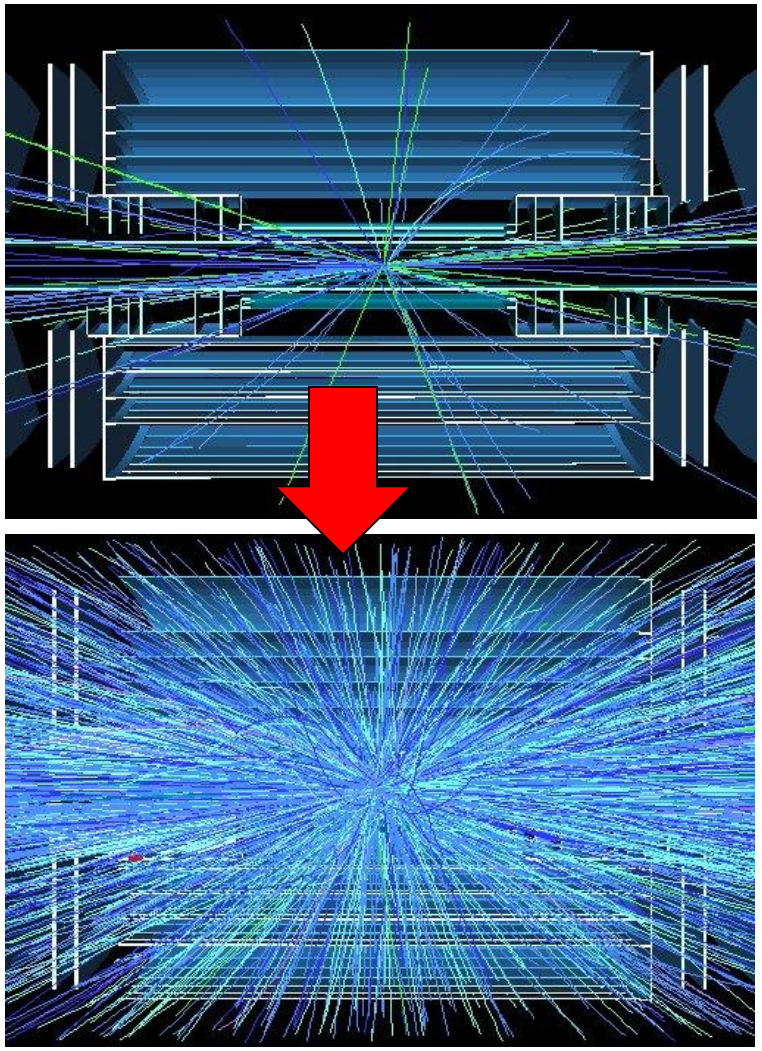
Injector and LHC Phase-1 upgrade to full design luminosity
$\sqrt{s}$ = 14 TeV, L ~ 2×10^{34} cm^{-2} s^{-1}, bunch spacing 25 ns, μ<80
Phase-I

HL-LHC Phase-2 upgrade, IR, crab cavities
$\sqrt{s}$ = 14 TeV, L = 5×10^{34} cm^{-2} s^{-1}, luminosity leveling,
μ~140, μ<200
Phase-II

Challenges for the future

- Increased luminosity requires
  - Higher hit-rate capability
  - Higher segmentation
  - Higher radiation hardness
  - Lighter detectors
  - Low noise & power

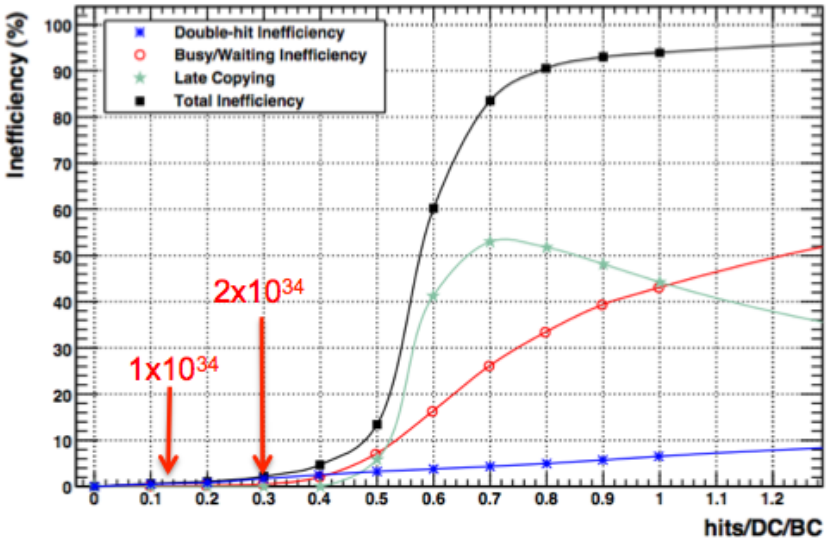
- Radiation hardness improvement compared to now
  - IBL approx. factor 5 (~300Mrad & $5x10^{15}/cm^2$ 1MeV neutron equivalent NIEL)
  - Phase-2 approx. factor 10 (~Grad & $10^{16}/cm^2$ 1MeV neutron equivalent NIEL on the innermost layer)



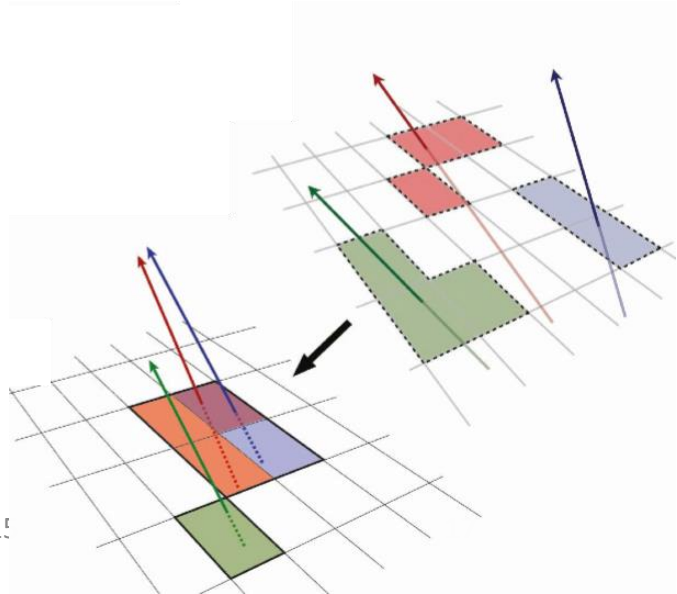
High hit rates & densities

- On the FE chip
  - High hit rates (>>MHz/mm2) fill buffers quickly which leads to inefficiencies
  - Developed FEI4 in 130nm technology with complex readout structure and improved radiation hardness

"old" FEI3 readout chip



- On sensors
  - High track density can lead to cluster merging
  - Particular critical for track reconstruction in high pT jets
  - Make sensor pixels smaller and sensors thinner to limit charge spread



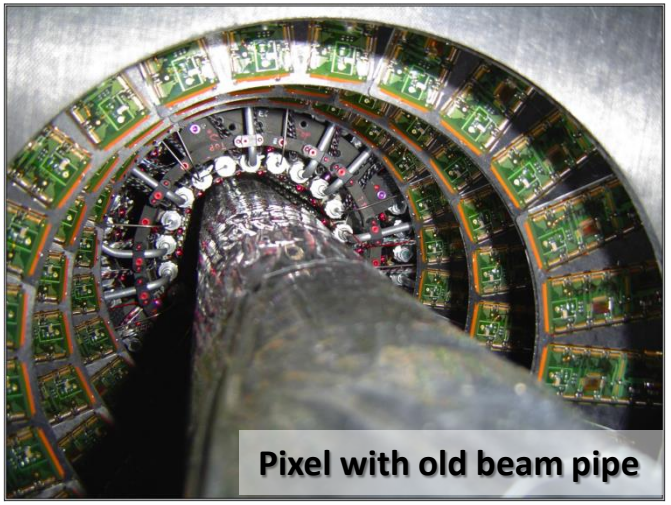
Major upgrade for ATLAS Pixel now ready

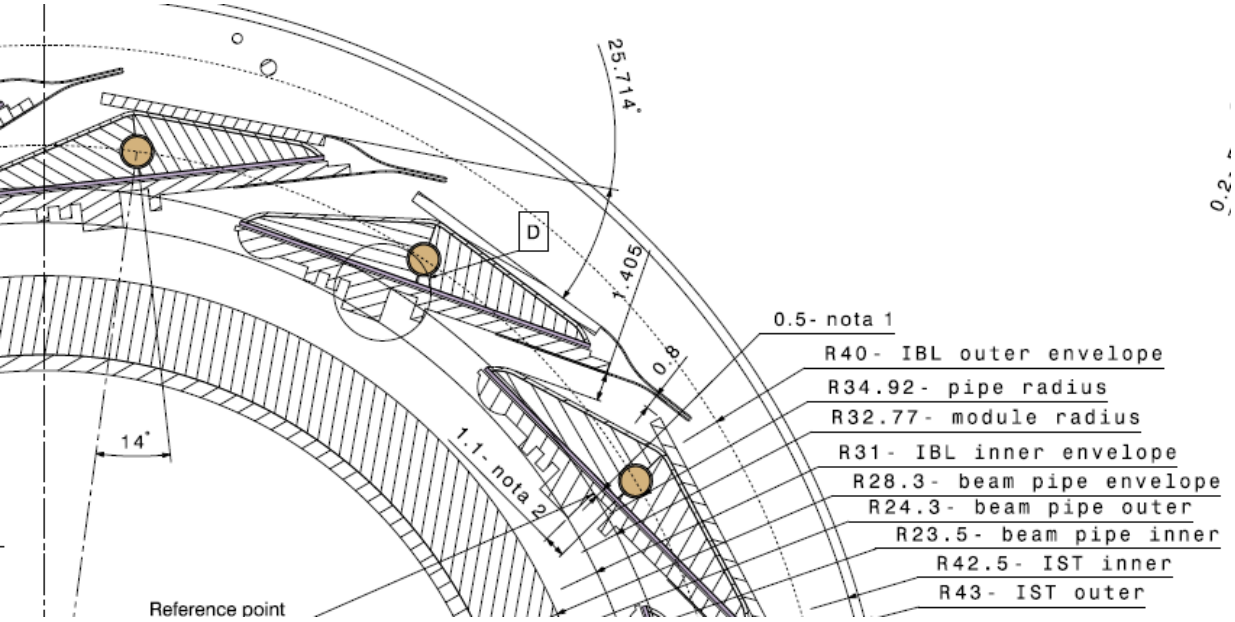
- It worked well but we can do better: **The ATLAS Pixel Detector for Run 2**
- Refurbish Run-1 Pixel detector: **New Service Quarter Panels (nSQP) and readout chain**
  - Keep the pixel detector assembled but rebuild all on-detector services
  - Repair all accessible failures
  - Move opto electronics to off-detector location for improved accessibility
  - Increase data bandwidth from modules to back-end electronics to be ready for luminosities in Run 2 and beyond (2-3 10^{34})
- **Insertable B-Layer (IBL)**
  - Extend the Pixel detector to a 4-Layer pixel system to improve pattern recognition and b-tagging, track reconstruction and additional redundancy for the future
  - New sensors, FE chips and light detector in center of existing detector
- **All those additions have been built before and during LS1 for installation in ATLAS during LS1**
- **The installation, connection and commisioning is done**
- **The new 4-layer Pixel Detector is ready for beam in LHC Run 2**

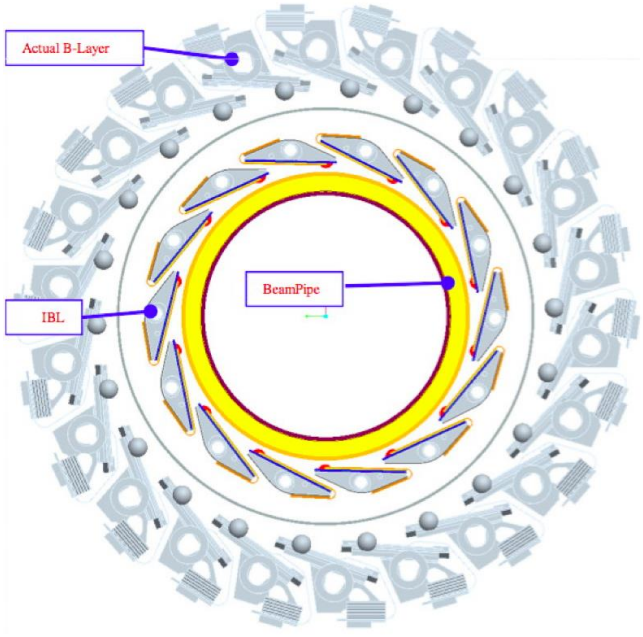
The ATLAS IBL

The ATLAS Insertable B-Layer:

- ✓4th Pixel layer (instead of b-layer replacement)
- ✓ Closer interaction point (5.05 → 3.27cm)
- ✓ Smaller pixels (50 x 250 μm2)
- ✓ Better sensors, better R/O chip
- ✓ Significantly reduced X0/Layer

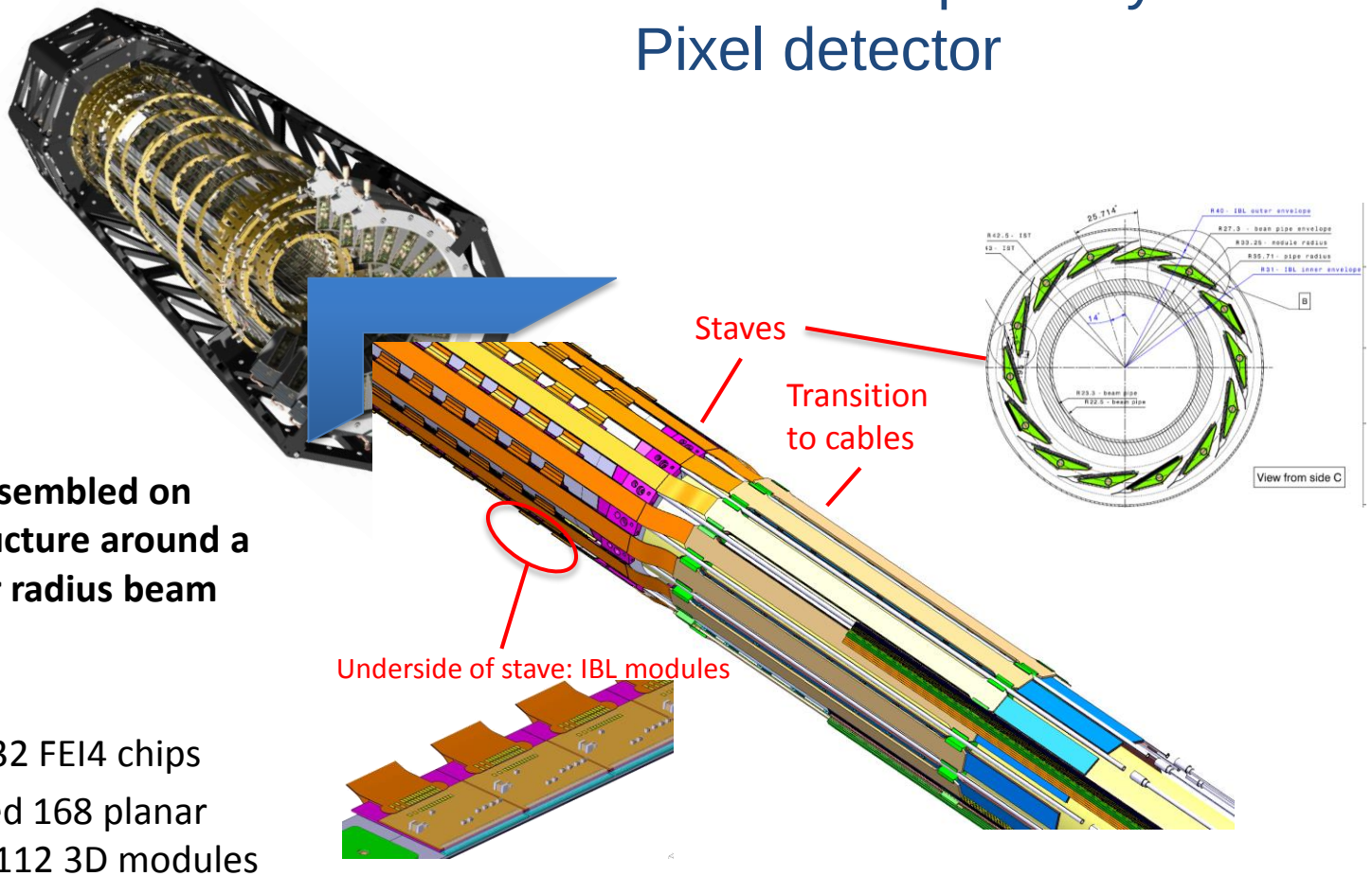






The Insertable B-Layer (IBL)

- Insert a 4th pixel layer existing Pixel detector



- **14 staves assembled on support structure around a new smaller radius beam pipe**

- Each stave: 32 FEI4 chips
- Total installed 168 planar modules or 112 3D modules

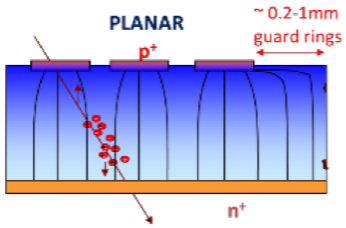
IBL new technologies

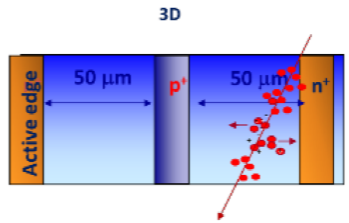
- For the IBL we have developed several new technologies to match the requirements for the IBL:

- New Sensors at smaller radius:
  - Radiation hard $5x10^{15}$ n_{eq}/cm^2
  - Geometrical acceptance >97%, Efficiency after irradiation >97%
  - Developed slim-edge planar and 3D silicon sensors
- New Front-end readout ASIC: FEI4 in IBM 130nm process
  - Improved data buffering/transfer architecture for higher hit-rate capability and eliminate readout inefficiency at higher luminosity and reduced radius.
  - Larger size (~4cm^2) for cost reduction and larger active area/physical size (FEI3:74% to FEI4:90%).
  - Thinned to 150 μm and solder bump-bonded to sensor
- New support structures and cooling
  - Reduce X0/Layer from ~3% to 1.9% including all supports
  - Cooled with CO_2 at $T_{coolant}$ = - 40C
- New readout system with higher bandwidth and processing power

IBL Sensors – planar & 3D silicon

Features	Planar	3D
Thickness (nominal) [µm]	200	230
Depletion voltage [V]	~35	10 - 25
Working voltage after LHC fluence ($5x10^{15}$ 1MeV n_{eq}/cm^2) [V]	~1000	~160
Pixel [FExRowxColumn]	2x336x80	1x336x80
Active size WxL [mm^2]	16.8 x 40.9	16.8 x 20.0



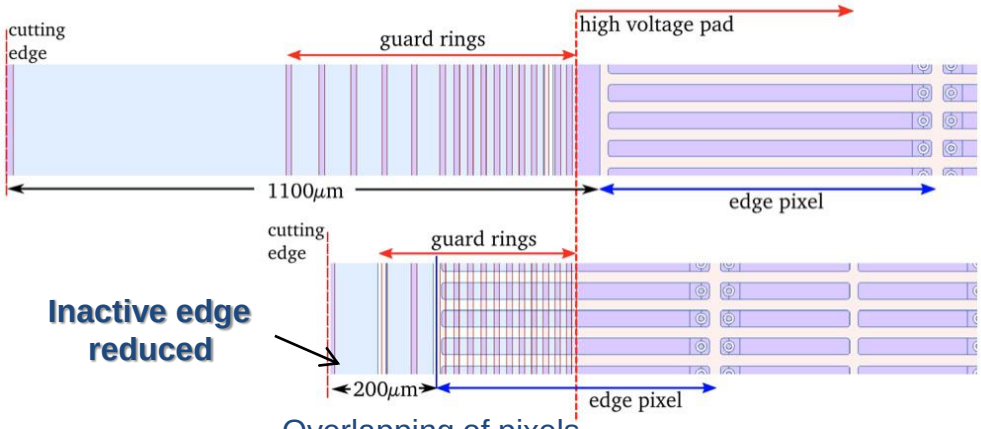


Planar features:

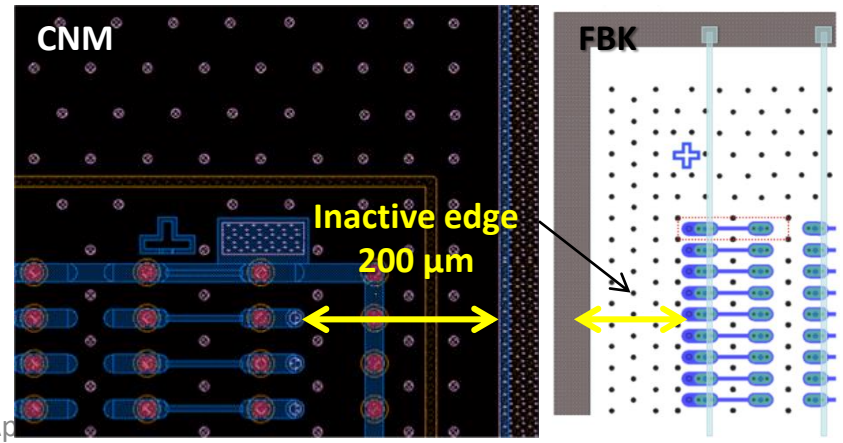
- **n-in-n** technology
- **Lower thickness** than Pixel
- **Inactive edge** minimized to 200 microns

3D features:

- **D**ouble-side **D**ouble **T**ype **C**olumns (DDTC) process
- **Guard ring fence:** 200 microns inactive area
- **CNM:** No full 3D columns (210 µm)
- **FBK:** Full 3D columns (230 µm)

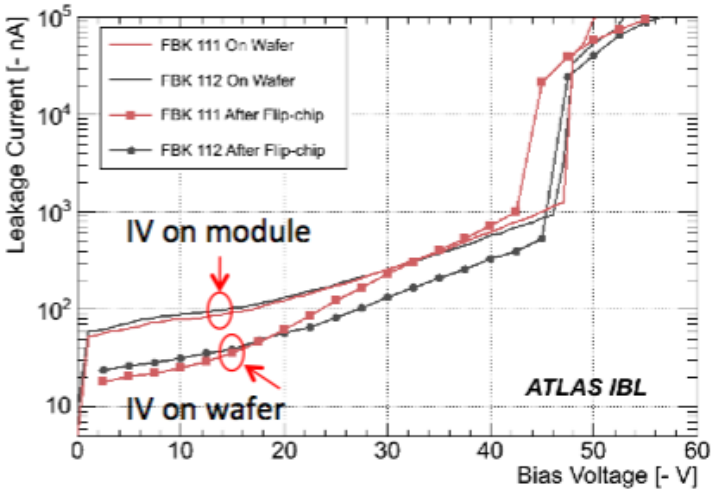


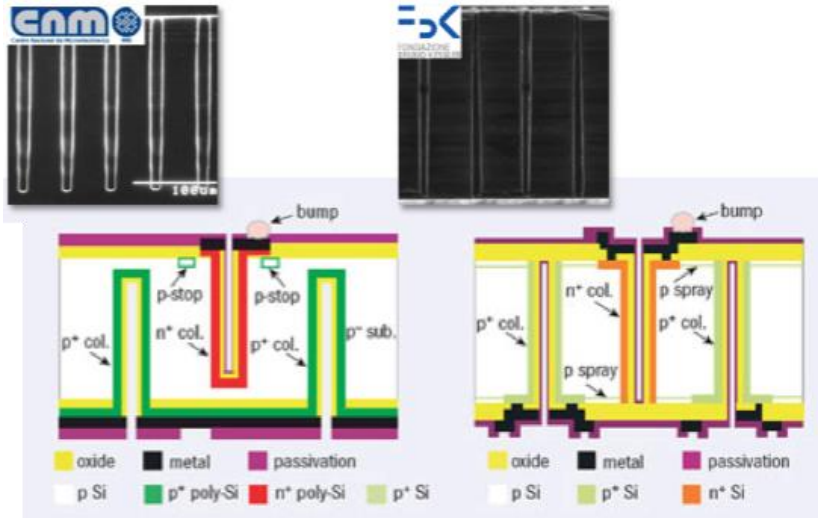
Overlapping of pixels and guard rings



IBL 3D silicon sensors

- Invented ~10 years ago (S. Parker/SLAC)
- Advantages : fast signal collection and low operation voltage for improved radiation hardness
- We developed 3D sensors for IBL use with FBK/Italy and CNM/Barcelona
- The IBL is the first use of silicon 3D detectors in a collider experiment
  - Gained first real production experience and will now get many years of operation experience
  - A very important setting stone for future use





New Front-end FEI4 chip

FEI4 main features:

- IBM (130 nm)
- 70 Million transistors
- 26880 pixels (50 x 250 μm2)
- Lower noise than FE-I3 (~150e- with sensor)
- Lower threshold operation (down to 1500 e-)
- Higher rate compatibility
- Radiation hard to >250Mrad
- In use for pixel R&D and towards Upgrade phase2

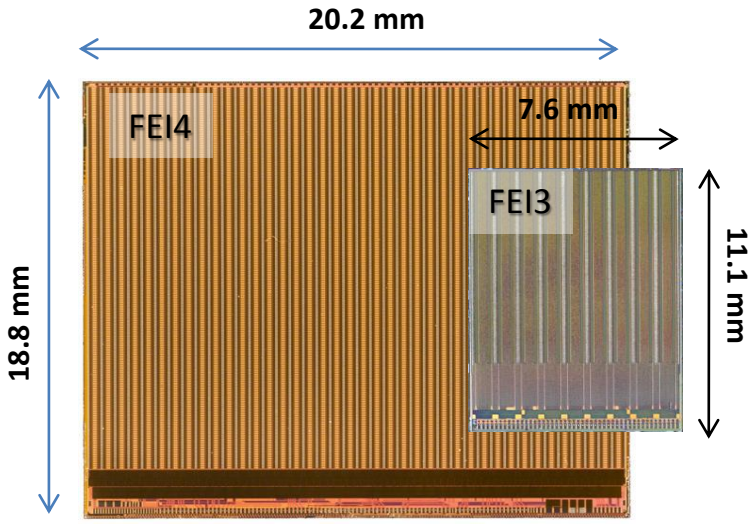
Through the FEI4 history:

➢ First version FEI4a for validation and IBL prototypes (32 FE-I4A wafers received in 2010/11)

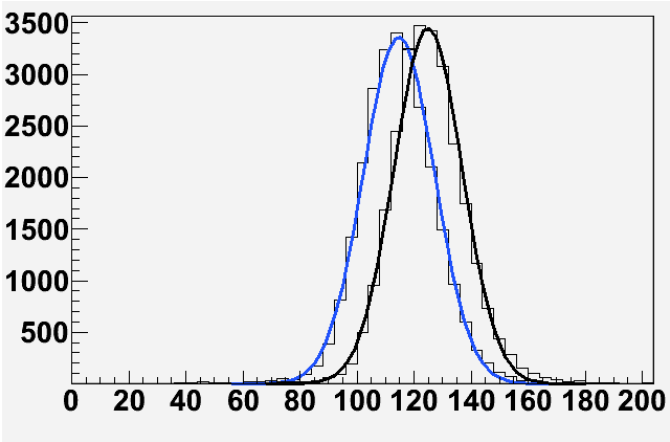
➢ FEI4b features: minor fixes + r/o functionalities + uniform pixel matrix + Power functionality

➢ First FEI4b delivery in Dec. 2011

➢ FEI4b production (30 wafers) and wafer probing is completed for IBL needs (yield ~60%)



FEI4b noise before and after irradiation (250 Mrad):
114e → 124e (both tuned)



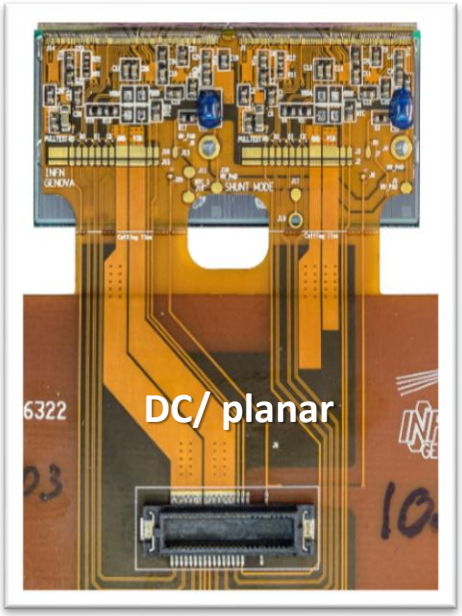
IBL Modules

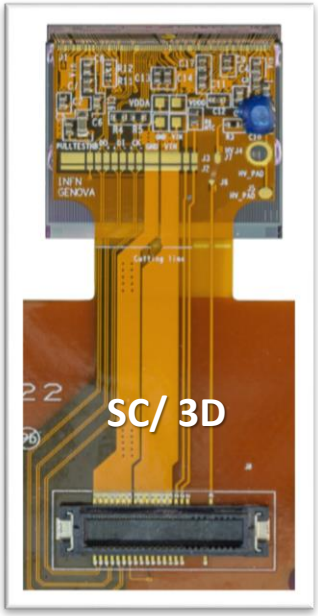
Thin module process steps:

① FE-I4 wafers thinned (150μm thick FE)
② Glued on glass support wafer
③ Bump deposition
④ Dicing wafer & substrate
⑤ Flip-chip & reflow
⑥ Substrate wafer removal by power laser.

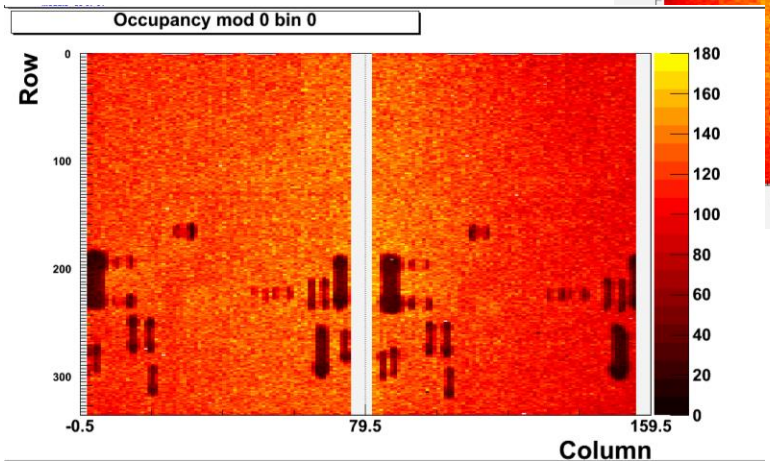
Final module assembly and QA
(at Bonn & Genova)

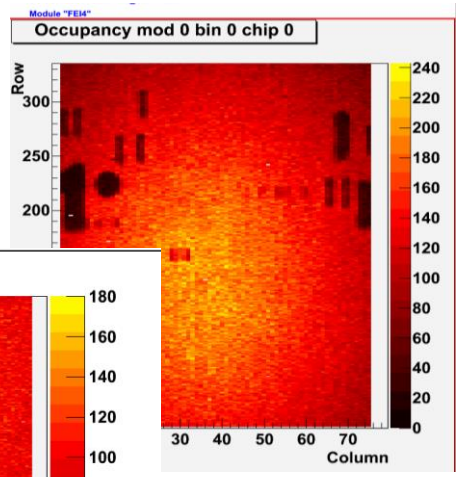
- Module dressing: DC module with flex
- Wire bonding
- Electrical QA and TC (including debug)





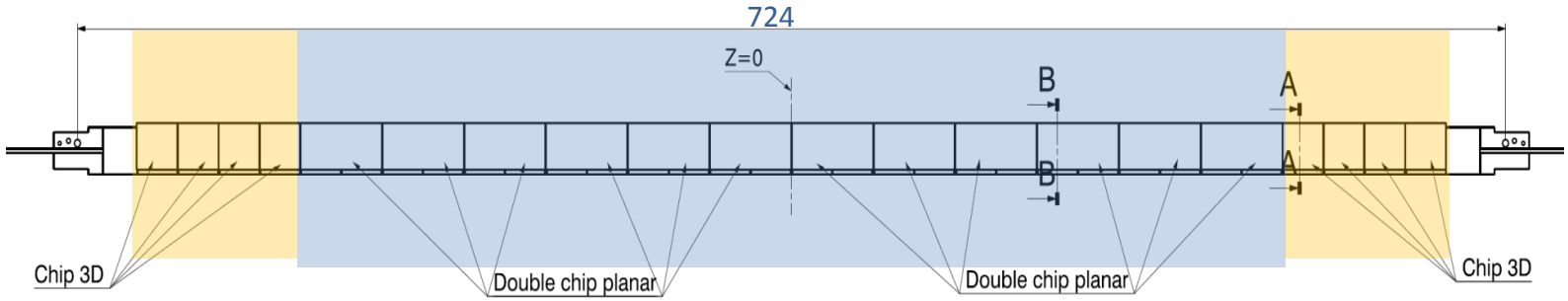
241 Am source scan during Module QA

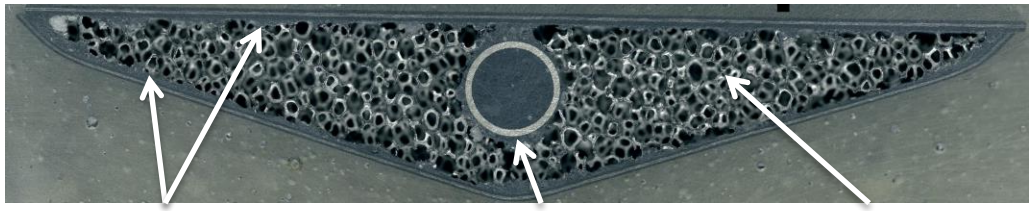




IBL Stave Layout

- 14 staves overlapping in phi mounted on inner positioning tube (IPT)
- 7m long assembly when integrated with services on both sides
- Very tight clearances between staves, IPT and outer IBL support tube (IST) due to tight space constraints
- IBL stave consists of 12 Double-chip modules using planar sensors and 8 single-chip modules using 3D sensors on ends (32 FEI4 chips/stave)
- Powered and readout from both ends (“half stave”) using Al/Cu flex circuits glue to support
- Cooling by 1.5mm diameter Ti pipe along stave length which is integrated in CF support

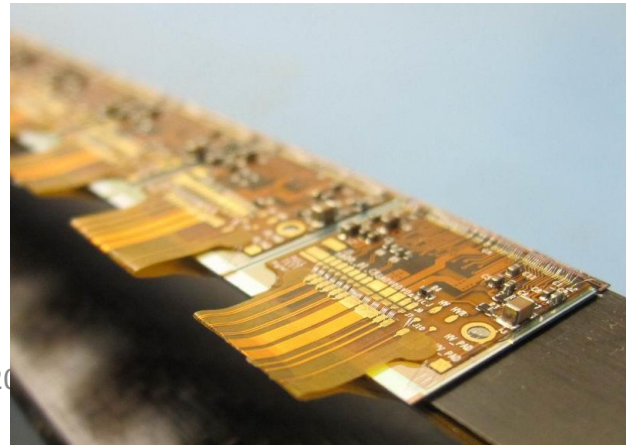




CF (K13C) 3 Layer Shell and face plate

Ti cooling pipe 1.5mm diameter (0.11 wall thickness)

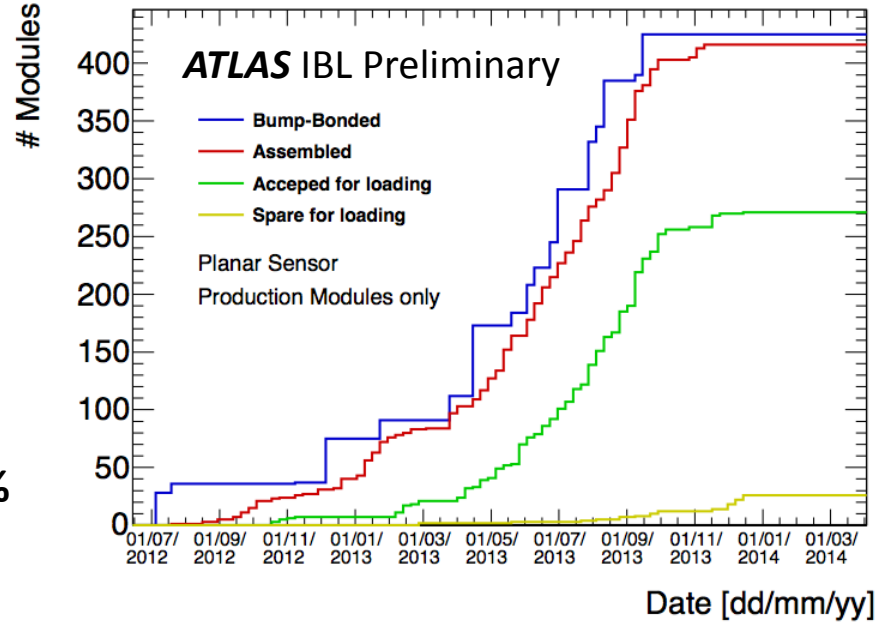
Carbon Foam filler



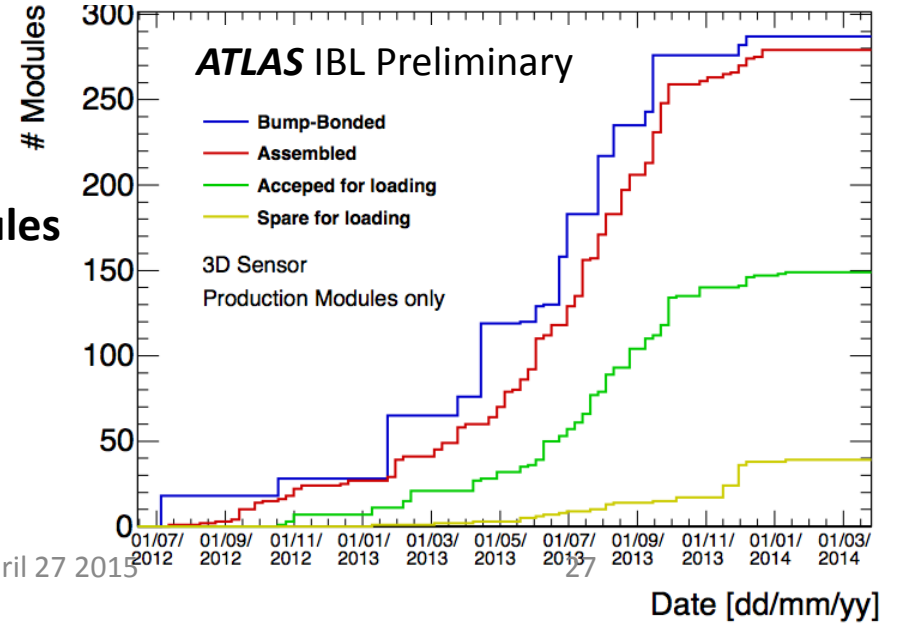
Module Production Experience

- Most IBL module produced during Jan-Oct 2013
- Module yields slightly lower than anticipated due to bump-bonding problems in first batches
  - Open bumps due to excessive flux in flip-chip
  - Shorts between pixels
  - Both problems disappeared when we moved to flux-free flip-chip process

DC planar modules
Yield ~ 75%



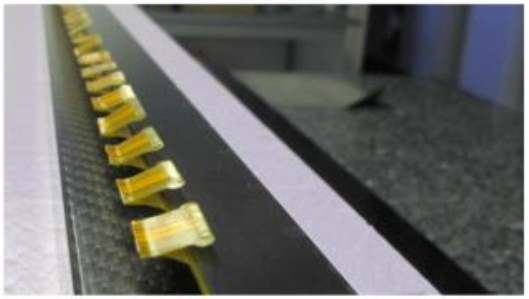
SC 3D modules
Yield ~ 62%



From Modules to Staves

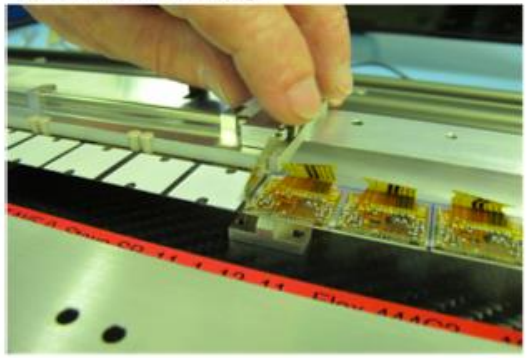
- Produced a total of 20 staves and selected best 14 for final detector

Bare stave with flex

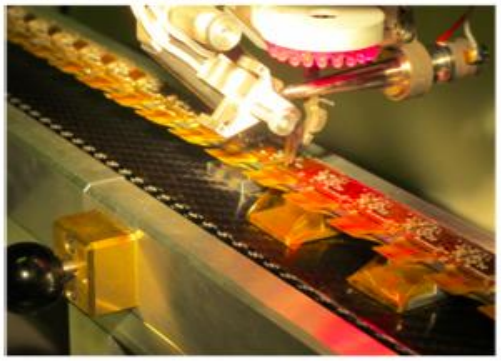


Thermal grease and glue

Module loading



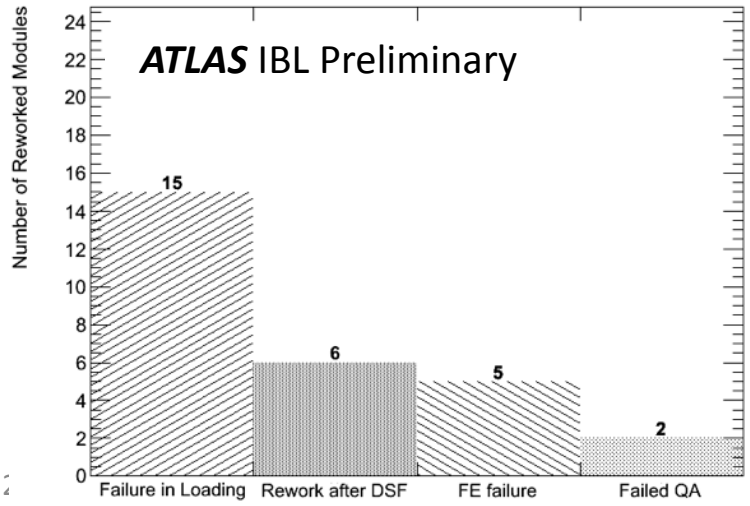
Wire bonding



428 Modules loaded

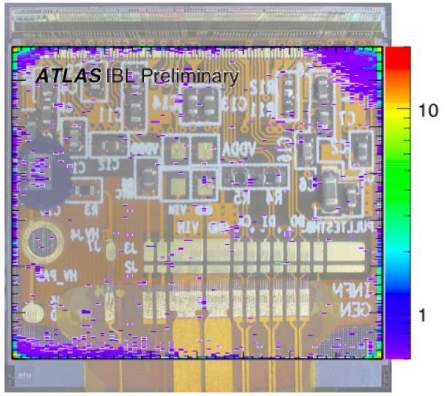
28 reworked on stave

Reason for rework

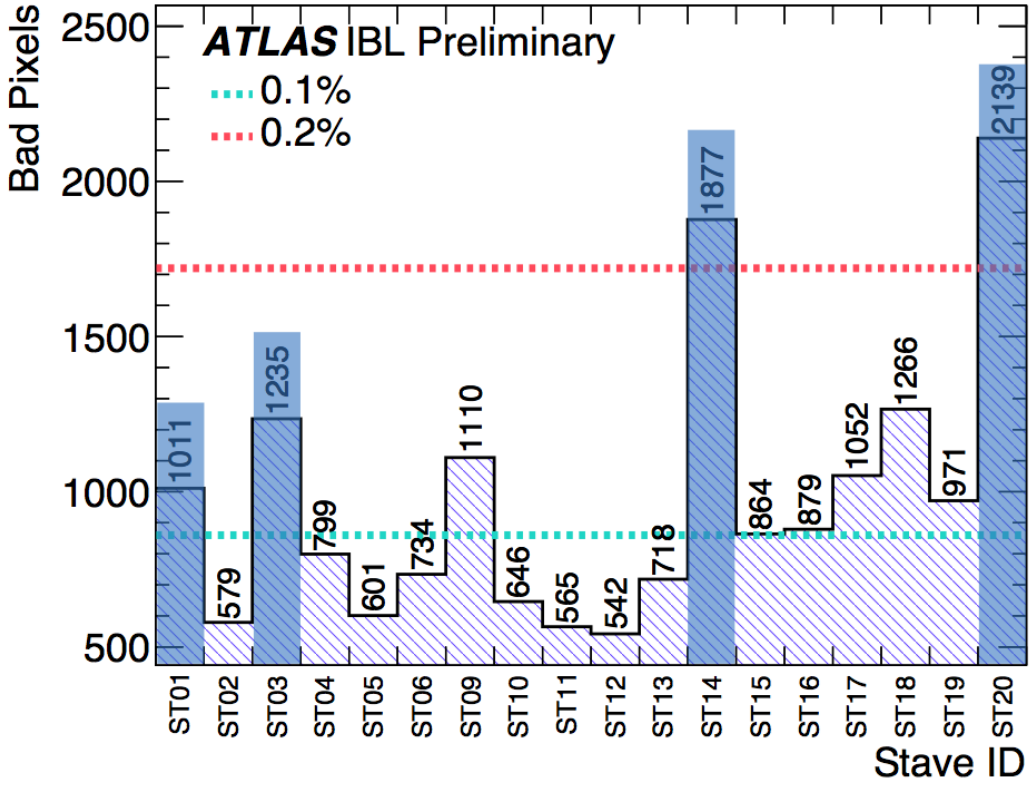


Overall Stave Quality (Stave QA)

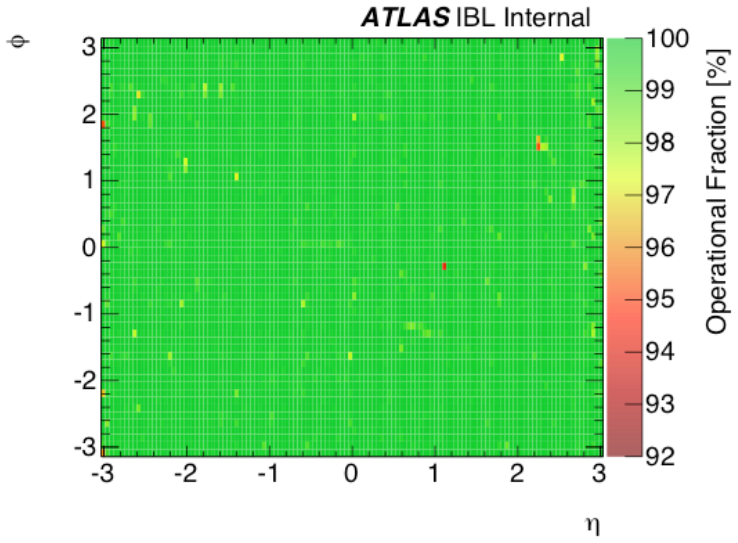
- Aim to have less than 1% dead pixels
- Actual detector has ~0.1 % dead pixels!
  - Disconnected pixels usually on sensor edges



1 Stave has 860 kpixels



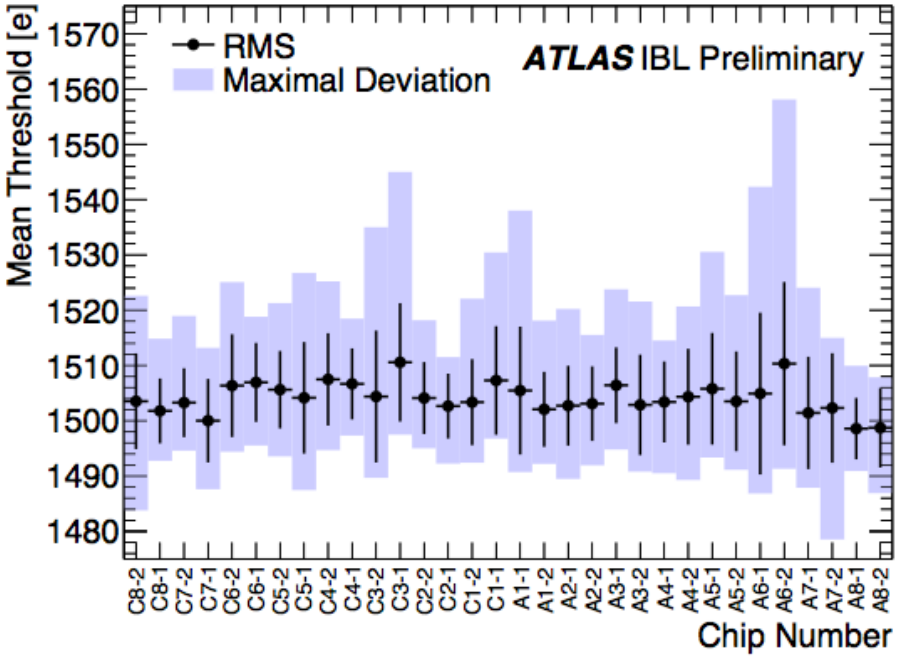
Arranged modules & staves in final IBL for uniform low $\eta-\phi$ distirbution of dead pixels for $\eta<2$



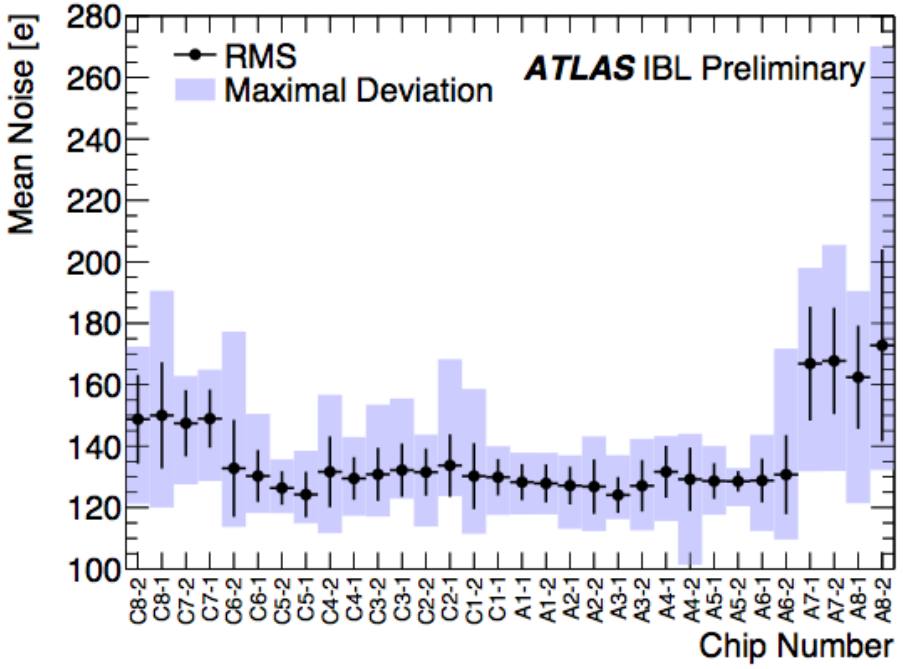
Stave Performance (Stave QA)

- Staves operate well at 1500e- threshold
  - Important for operation after radiation damage!
- Noise is ~130e- for planar and ~150/170e- for 3D CNM/FBK modules

Mean Threshold versus chip position



Mean Noise versus chip position



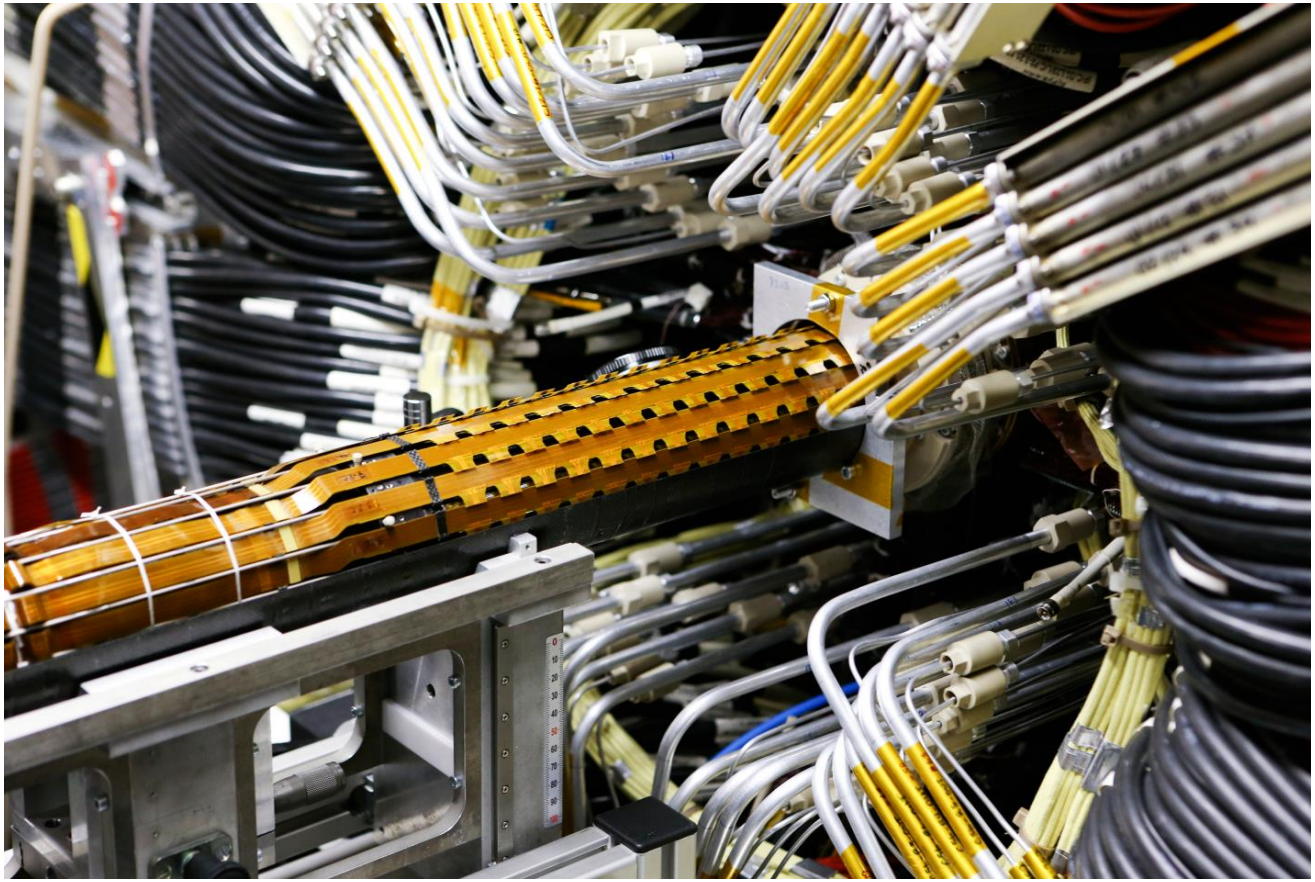
IBL integrated on IPT

The last stave goes on - March 26th

- Integrated all 14 stave around the beam pipe within one month
- Tested electrical function of all modules after integration -> no dead chip ~ 100% of all chips functional
- “Connectivity test” checks analog and digital function of modules as well as sensor’s IV and modules DCS info
- The test confirmed the results measured during stave QA
  - No deterioration after final integration with services and support pipes

The IBL is installed!

- May 7th: The ATLAS IBL is completed and installed!



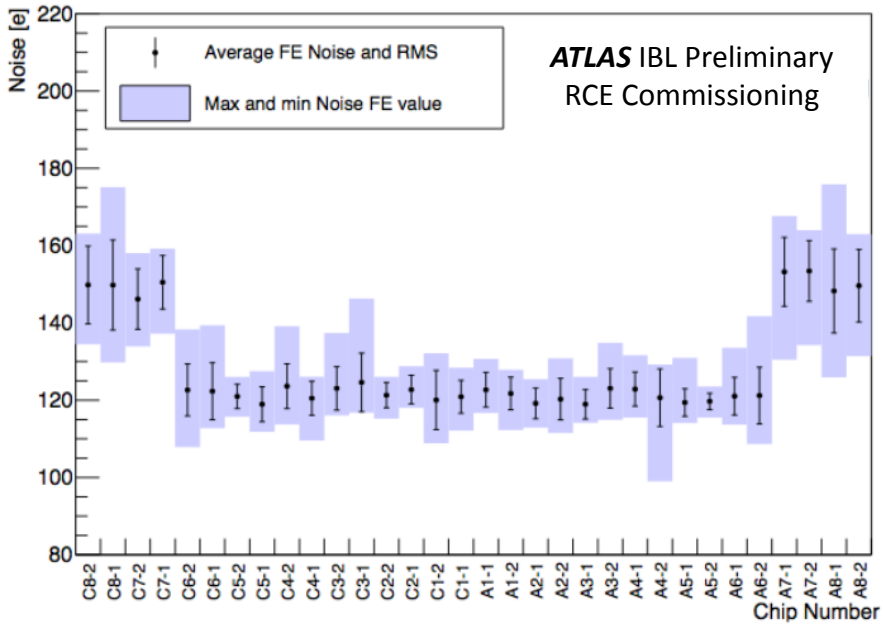
Initial commissioning

- The Pixel Detector + IBL commissioning has started beginning of July to check and adjust the detector
- The IBL's performance was re-measured again for analog and digital performance in its final configuration in the pit
- 100% of IBL chips are functional, the detector operated very stable at room temperature and -5C coolant, go cold now.
- Comparison to the stave QA data and integration tests confirmed that noise and module operation are identical

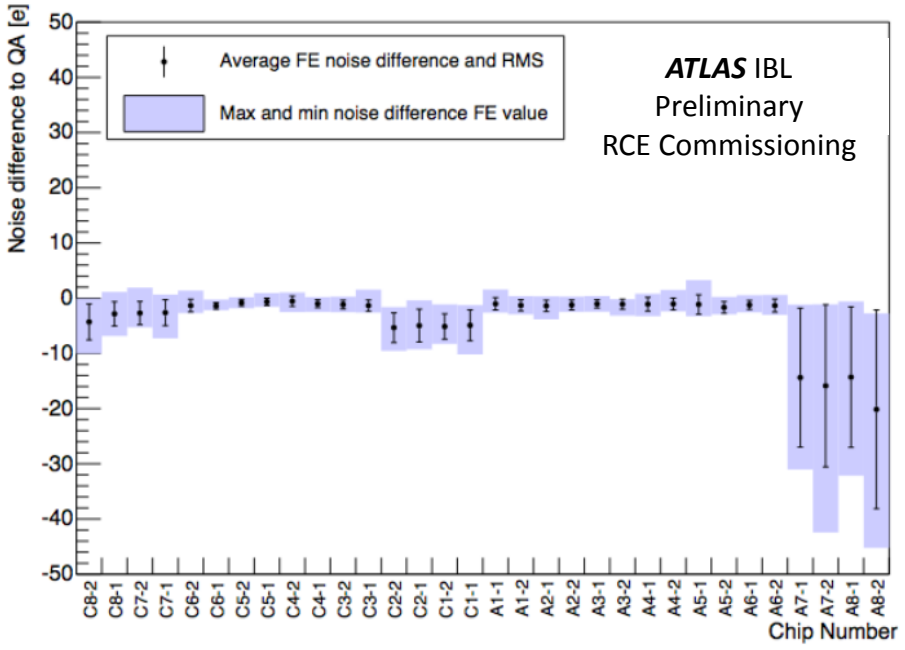
IBL : Finally in pit – Stave QA

- First preliminary comparison of IBL stave noise, threshold in pit to IBL Stave QA

Mean noise in pit – Preliminary!



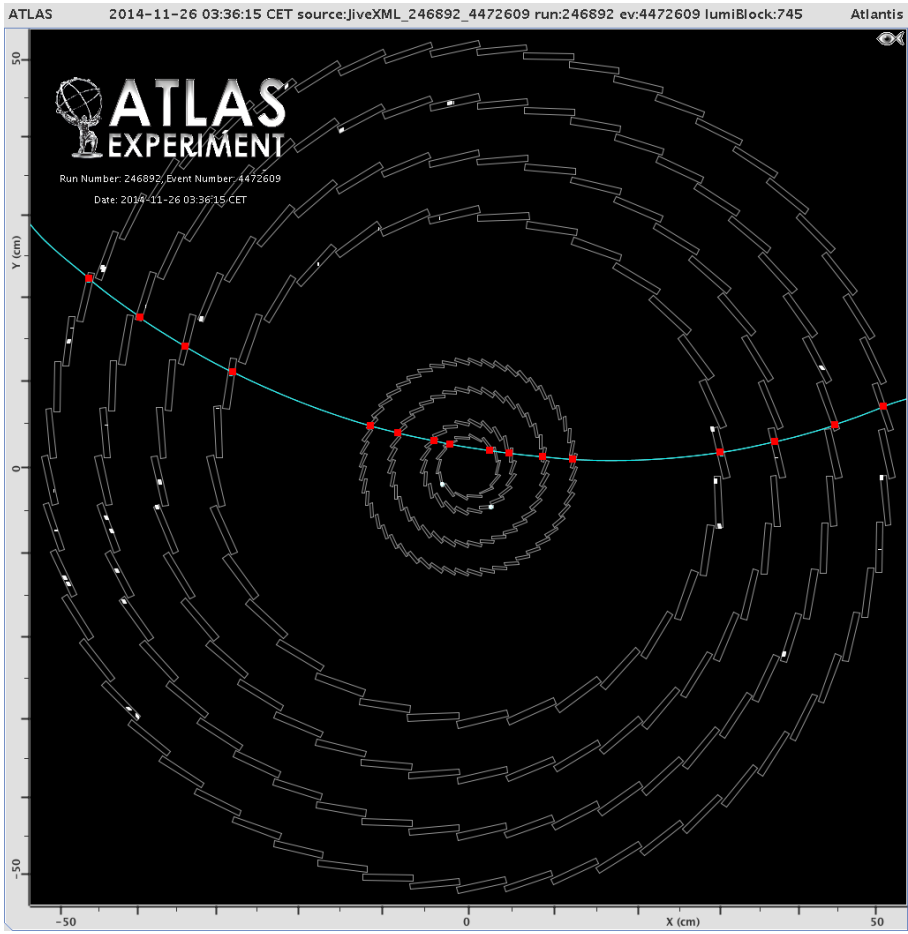
Difference Noise in Pit minus Noise in Stave QA



- The next major steps are the commissioning of the combined Pxel+IBL system, tuning of detector and integration to ATLAS data taking system

Cosmic commissioning

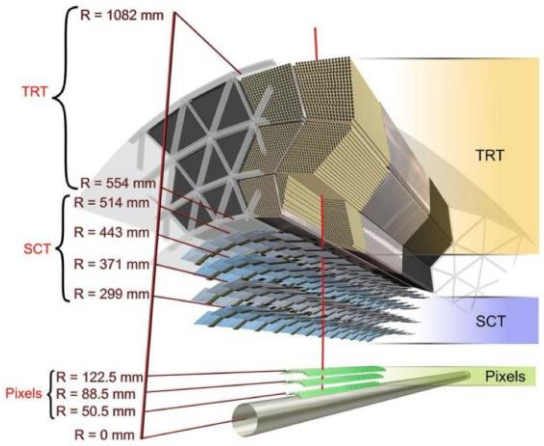
- 4 Layer Pixel system now ready to run
- Integrated in ATLAS controls, readout and reconstruction software
- Made a first round of signal and alignment measurements using cosmic tracks
- First stable colliding beam expected for June 1

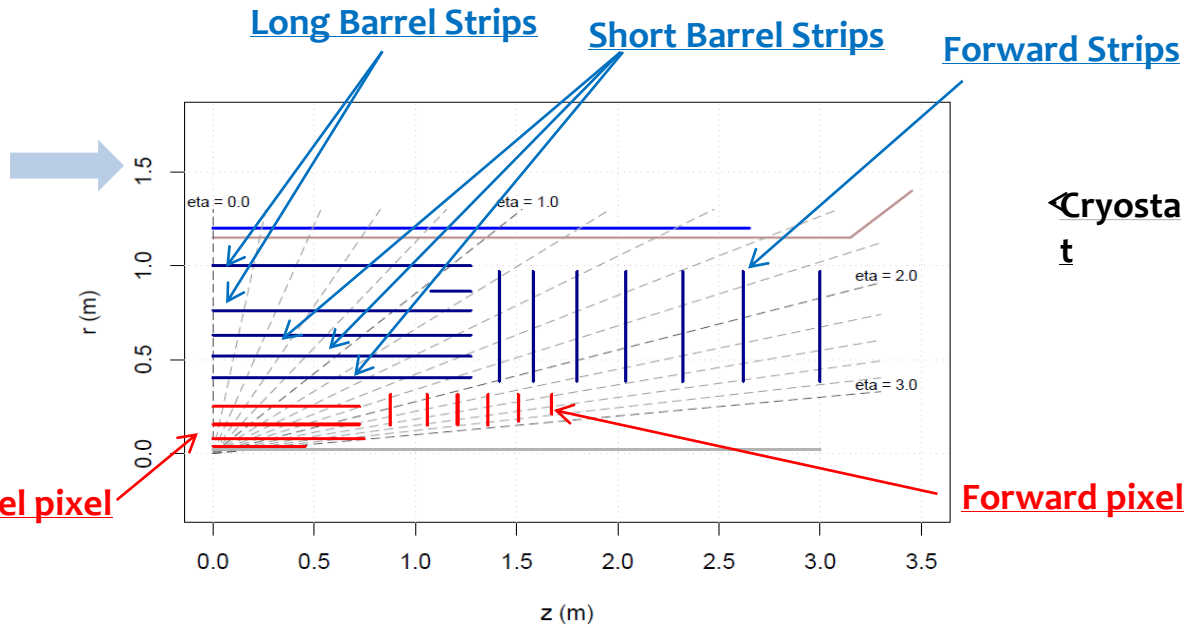


The future of pixel detectors at LHC

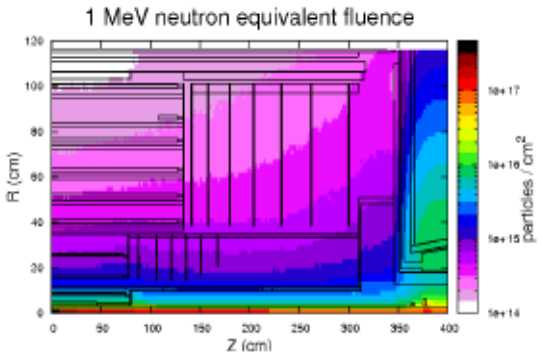
- Several new Pixel detectors are planned / under construction for the future at LHC
  - CMS 4 –layer pixel detector for installation 2017
  - ALICE ITS pixel detector for installation in 2019
  - LHCb Velo Pixel for installation in 2019 (see Paula's talk)
  - ATLAS and CMS new pixel tracker for operation in HL-LHC beyond 2025
- Many new developments ongoing to cope with the enormous hit rate, track densities, radiation levels, precision requirements
- Detector size and costs are substantial, hence strong push for potentially cheaper technologies and optimized layouts
- Two examples : ITK pixel for ATLAS and ITS for ALICE

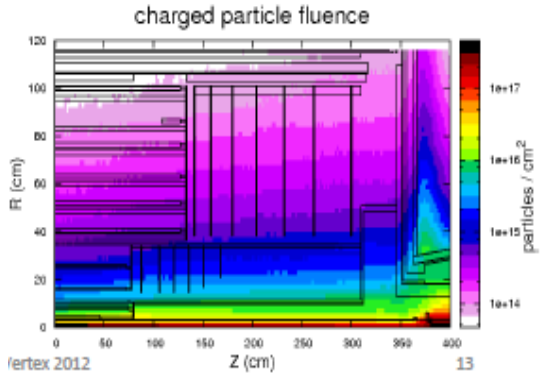
What's next ? ATLAS HL-LHC





All Silicon tracker for Phase 2 (TRT would not cope with occupancy)
Baseline layout of the new ATLAS inner tracker for HL-LHC
Aim to have at least 14 silicon hits everywhere (robust tracking)





14 TeV collisions; integrated luminosity = 3000fb⁻¹

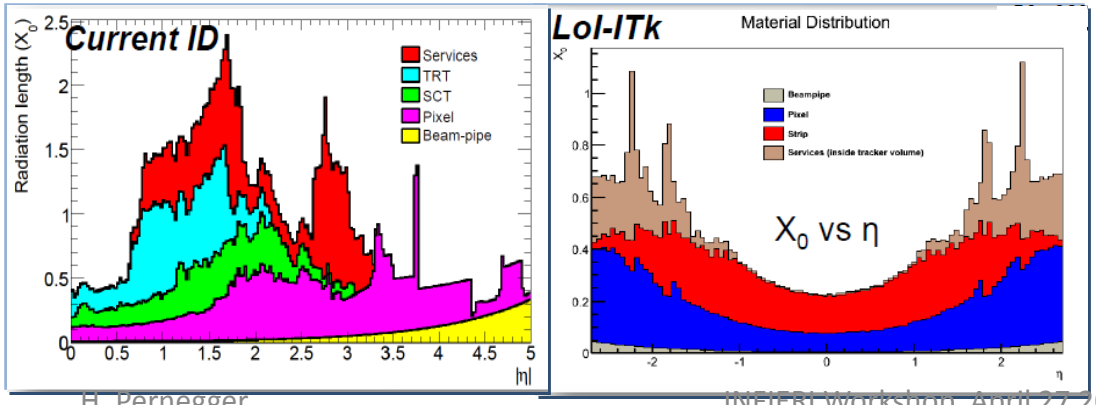
ITK - Tracker performance

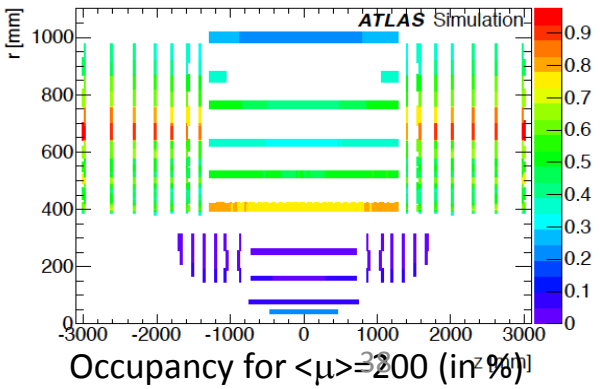
- New Inner Detector Improved granularity
  (Smaller pixels and 4.9cm and 9.8cm strips (74.5µm pitch)
  - ➢Improved radiation hardness
  - ➢Reduced material
  - ➢Extended forward coverage
  - ➢Robust tracking (14 layers)
  - ➢Exact distribution of layers (how many pixel & strips under study, extension to eta <4?))

Basic numbers of baseline (LoI):

Detector:	Silicon area [m^2]	Channels [10^6]
Pixel barrel	5.1	445
Pixel end-cap	3.1	193
Pixel total	**8.2**	**638**
Strip barrel	122	47
Strip end-cap	71	27
Strip total	**193**	**74**

Tracker - now and then:

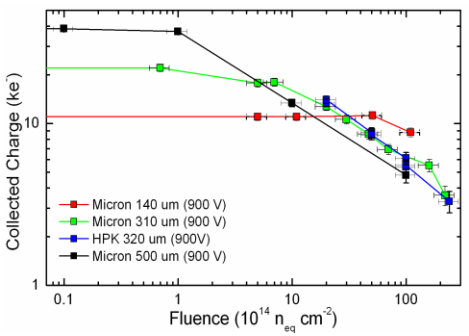




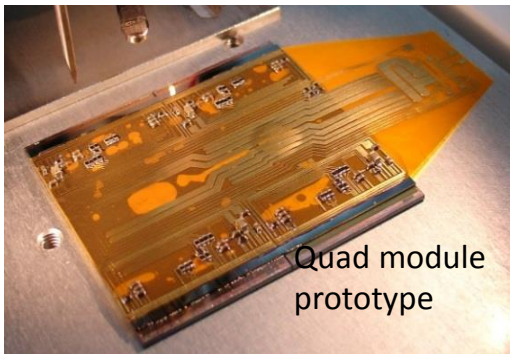
Occupancy for <µ>=200 (in %)

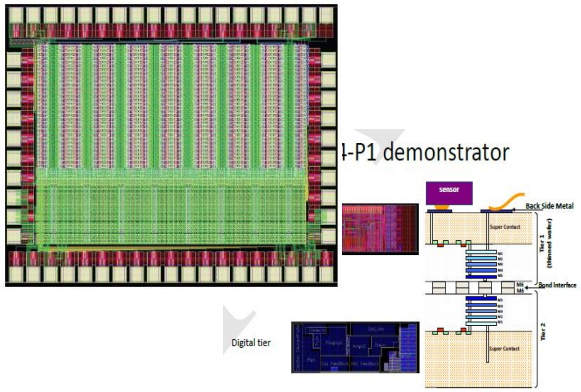
ATLAS ITK pixels

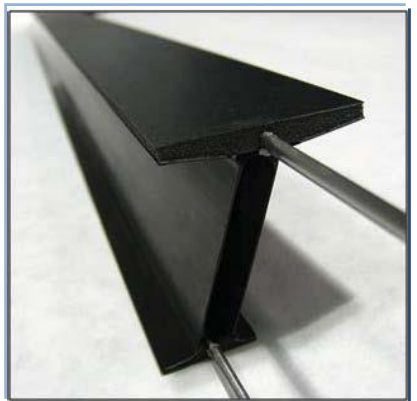
Pixel Detector



- Pixel sensors in several technologies proved to high doses (planar/3D/diamond shown to $2\times10^{16}n_{eq}/cm^2$)
- Next front end chip has to deal with 1Gbps per chip scheme, go down to 25µm×125µm pixels with 65 nm CMOS
- Common effort to develop pixel chip at 65nm (RD-53)
- Larger area sensors quads produced on 150mm diameter wafers with several foundries
- Quad pixel module produced, being tested and results look promising
- Prototyping of local supports for various concepts has been carried out

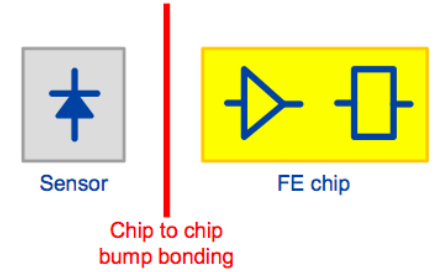




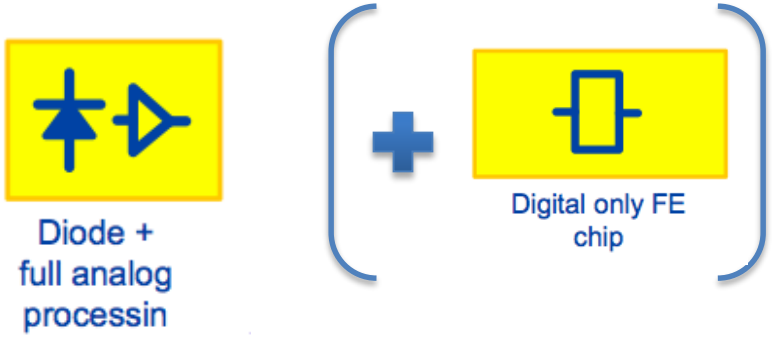


Development of CMOS sensors for LHC

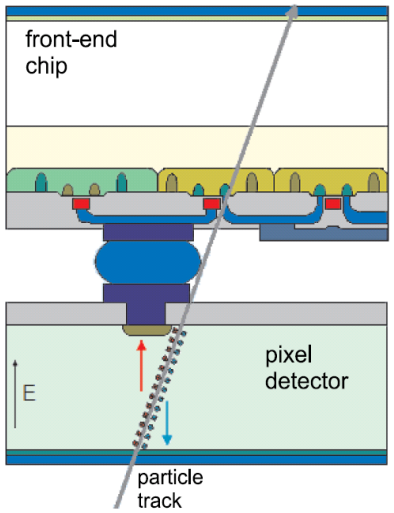
Compared to hybrid pixel detectors, the **sensitive volume and part or the full readout circuitry is combined in one piece of silicon**. The generated charge is collected on a dedicated collection electrode.



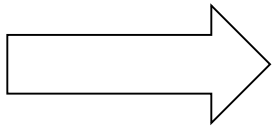
Hybrid Pixel Detector

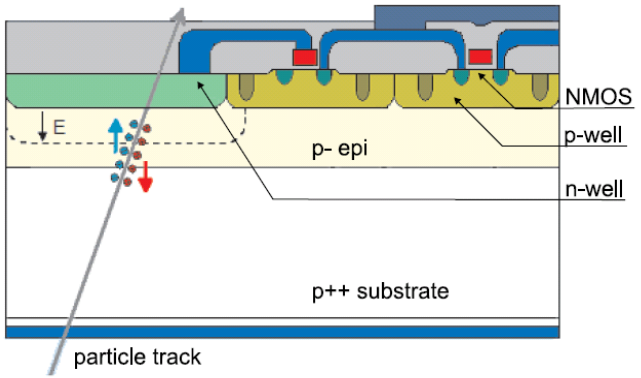


Integrate first level electronics into CMOS sensor



N. Wermers/Univ. of Bonn





P. Riedler FCC workshop April 2015

ALICE Inner Tracking System Upgrade at LHC

Based on high resistivity epi layer MAPS

3 Inner Barrel layers (IB)
4 Outer Barrel layers (OB)

Radial coverage: 21-400 mm

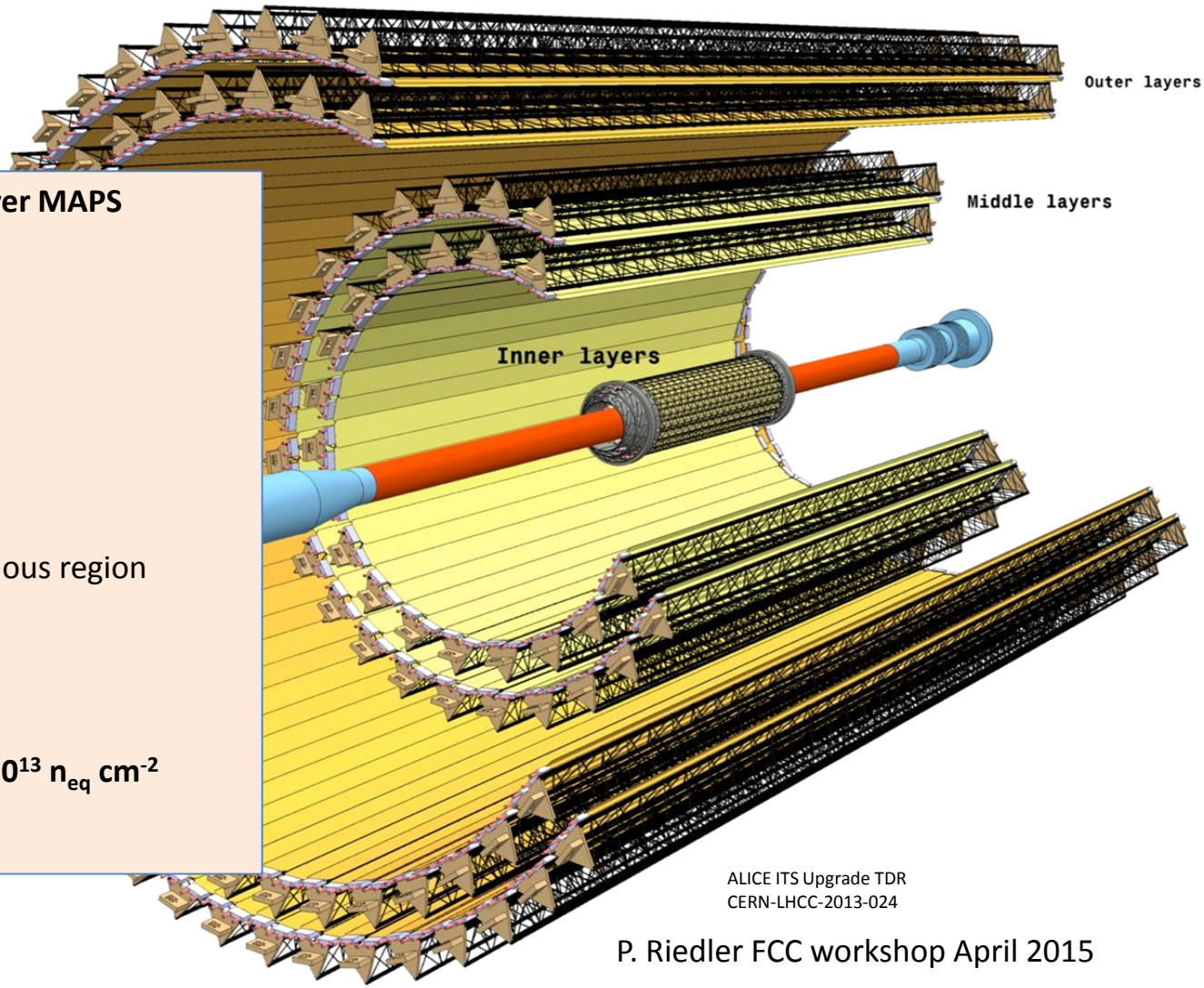
~ 10 m^2

$|\eta|<1.22$ over 90% of the luminous region

0.3% X_0/layer (IB)
0.8 % X_0/layer (OB)

Radiation level (L0): 700 krad/10^{13} n_{eq} cm^{-2}

Installation during LS2



ALICE ITS Upgrade TDR
CERN-LHCC-2013-024

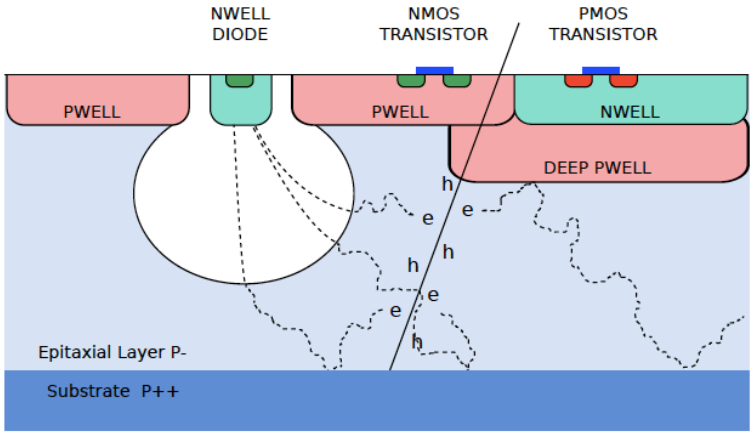
P. Riedler FCC workshop April 2015

ALICE ITS Upgrade: High res epi layer MAPS

N-well collection electrode in high resistivity epitaxial layer (>1kohmcm)

TowerJazz 0.18 um CMOS Imaging Process

- Special deep p-well for full CMOS within matrix (based on experience of RAL)
- 6 metal layers -> suited for high density, low power circuitry
- Small n-well diode (2-3 µm diameter), ~ 100 times smaller than pixel → low capacitance
- 3 nm gate oxide -> TID tolerant
- Epi thicknesses 20-40 µm tested → higher cluster signal
- Partial depletion of the epi layer (limited by circuitry)



Schematic cross-section of CMOS pixel sensor (*ALICE ITS Upgrade TDR*)

NWELL diode output signal:

$$V \sim Q/C$$

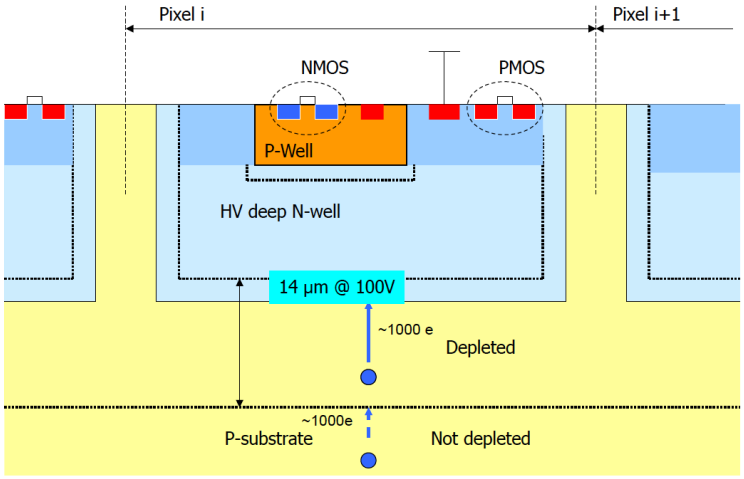
- Increase charge collected by the central pixel
- Minimize capacitance:
  - diode surface
  - depletion volume

→ (reverse substrate) bias

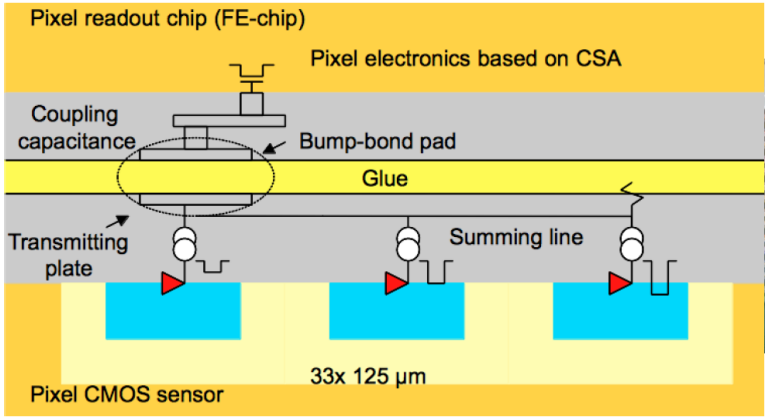
ALICE ITS TDR

Radiation hard HV CMOS in ATLAS

- ATLAS requires very radiation hard sensors, which present CMOS cannot do (>10 to 100 Mrad range)
- Started RD to develop commercial CMOS processes to radiation hard sensors through optimized designs, high voltage processes (>100V on chip) and higher resistivity (kOhm?)
- Commercial processes can give big cost savings and simplify assembly
- This allows to deplete the sensing volume deep into the substrate and collect charge by drift (rather then diffusion)
- Sensors becomes “functional” and can improve spatial resolution through finer segmentation into sub pixels
- We have produced test structure in several different foundries to study their performance

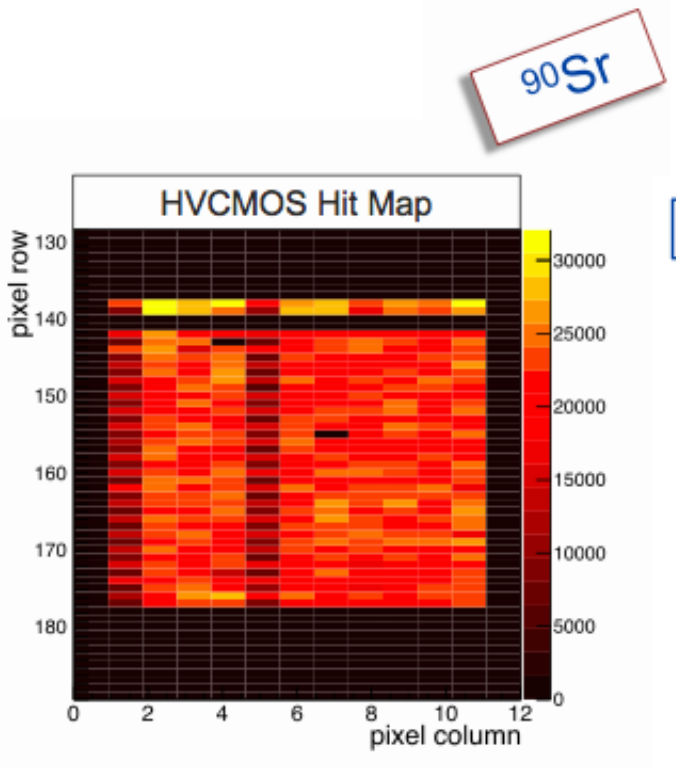


CMOS electronics placed inside the diode (inside the n-well)



Rad hard CMOS tests

- Test in Lab and testbeam are encouraging but a lot remains to be done to qualify them as radiation had for use in the ITK



CCPD AMS 180nm

M. Backhaus / PSD 2014

The outlook

- **ATLAS has now a 4-layer pixel detector system in the center of the experiment and our commissioning efforts started to ensure the best possible tracking performance ready for Run 2**

- **The construction of the IBL is complete and it is installed in the pit**
  - Module and stave QA showed 99.9% functional channels on the modules
  - It operates well at 1500e- threshold and shows good noise performance
  - It is the first large scale application of 3D sensors as well as the new ATLAS FEI4 pixel chip

- Pixel detector specifications and their performance keep increasing and LHC experiments constantly push the limits of many technologies
  - Sensors, FE electronics, mechanics, integration,…)
  - Their performance parameters are improved by factors (not %) from each generation to the next

- Pixel detectors are fascinating devices and they get more and more important in collider experiments