

**AIDA** 2020

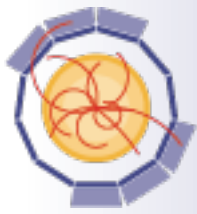
Advanced European Infrastructures  
for Detectors at Accelerators

# Introduction to hardware tasks

Data Synchronization



*This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 654168.*



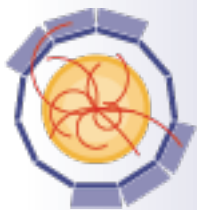
- Synchronize the data:
  - First step of any DAQ with multiple detectors
  - Use triggers and/or common clock
- Aim of WP5 hardware tasks:
  - Provide hardware standards
    - Clock/Synchronization/Trigger
    - Support existing standards
  - Provide hardware tools
    - Trigger Logic Unit (TLU)
      - Development of AIDA TLU
  - Provide support





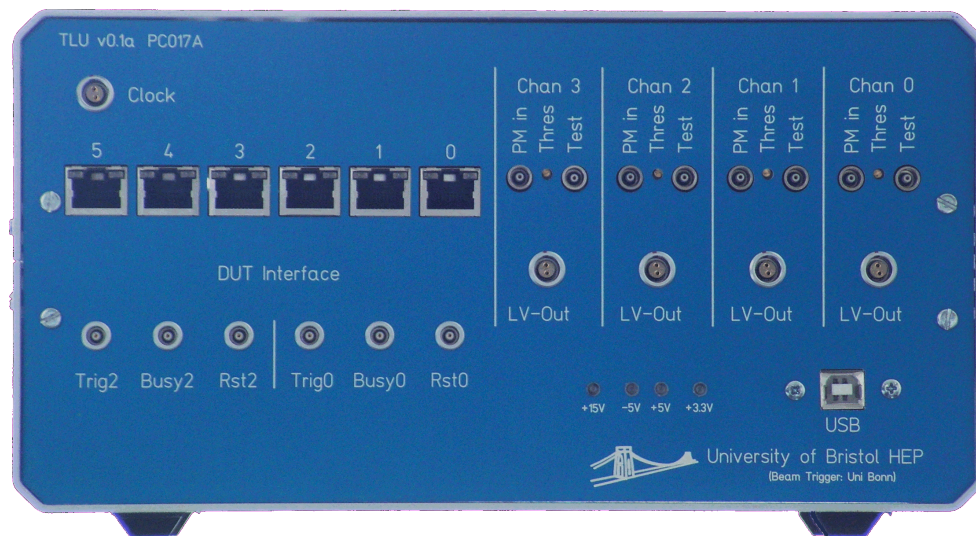
### • **Task 5.2 Interface, synchronisation and control of multiple-detector systems**

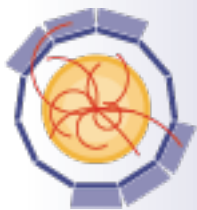
- Specification of interfaces for the common DAQ; this should incorporate compatibility with trigger logic unit (TLU) and Clock and Control Card (CCC) but also have a clear definition for other DAQ systems and detectors to plug in to
- Timing and synchronisation signals to be harmonised so that signals from different detectors can be correlated
  - Ensure compatibility with and between TLU and CCC, the two principal synchronisation and control systems used by Linear Collider detectors
- Development of TLU (and CCC) firmware to cater for new detectors and combined beam tests.
- Provide TLUs for combined beam tests
- Set up of different beam tests and aid integration to common DAQ
- Expert support during beam tests
- Successful completion of beam tests with multiple detectors



### • EUDET TLU

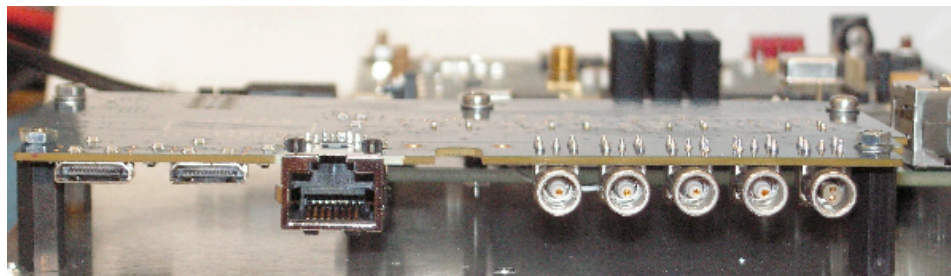
- Designed for Linear Collider Vertex detector beam tests
- Low rate (  $\sim 100$  kHz maximum )
- No common clock
  - Trigger/Busy
- Synchronization by triggers
  - (Optional) check synchronization by reading out trigger number.
- $\sim 30$  units made



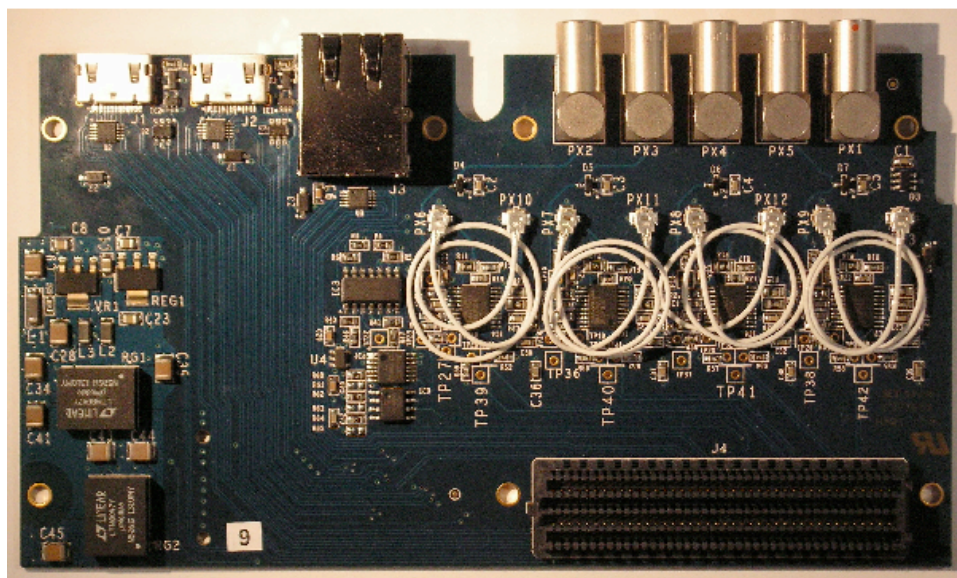


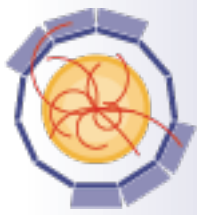
### • AIDA TLU

- Backwards compatible with EUDET interface
- New synchronous interface
  - Clock / Trigger / Busy / T0
  - Higher rate – 1MHz average , 10MHz burst
- More precise time-stamping ( <1ns cf. ~3ns )
- Four scintillator inputs , three DUT i/face.

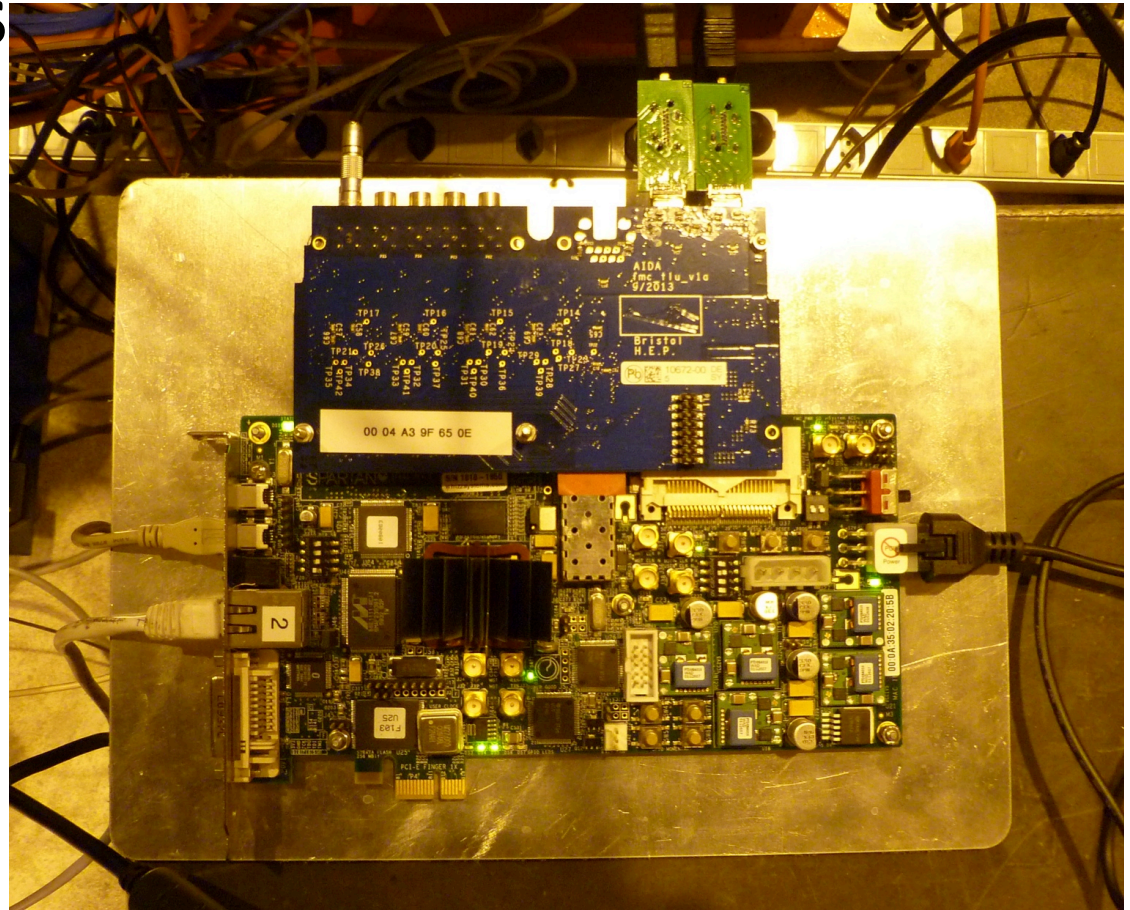


DUT0 (HDMI)   DUT1 (HDMI)   DUT2 (RJ45)   Trigger Inputs   Clock I/O





- **Implemented as FMC card**
  - COTS FPGA board
  - Easy to move to new FPGA
- **Ten modules exist. Seven in use.**
  - Bug in HDMI pin-out (fixable with “dongle”)





- **Development of AIDA TLU**

- Same interface definition

- **Open Hardware** (<http://www.ohwr.org/projects/fmc-mtlu> )

- **Two varieties**

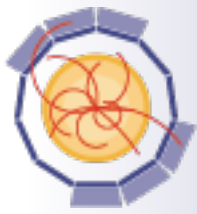
- Mini-TLU ( development of AIDA TLU ).

- Available for purchase, ~ Euro 1000.
- Q4 2015

- **Maxi-TLU.**

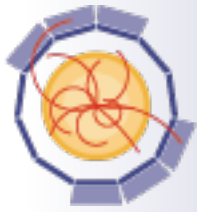
- More trigger inputs, more DUT interfaces.
- Supplied to beam lines for common beam-tests as part of WP5.
- Final versions Q4 2017 (M30) of AIDA-2020. Prototypes earlier.
- Firmware/software compatible with mini-TLU

- Integrate in home lab against Mini-TLU, easy integration at beam-line.

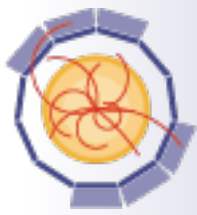


- **TLU interface physically compatible with CALICE CCC ( by design ).**
  - See CALICE talk later.
- **Preliminary agreement about interface specification**
  - Needs checking/ community approval.
- **Integration tests need to be defined and performed**
  - Worry about “jitter peaking” in chained PLLs ( though not observed so far with chained Xilinx FPGA PLLs )

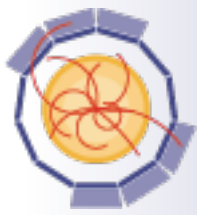




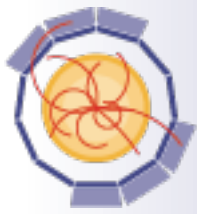
- **Passes information about beam ( from scintillator triggers ) to CALICE DAQ**
- **Send data with same data format as DIF→LDA link**
- **Can be same physical object as TLU**
  - One link to CCC for clock/synchronization
  - One link to LDA to pass beam information



- **AIDA-2020 TLU backward compatible with EUDET TLU**
- **Needs change to DAQ to allow multiple triggers per readout frame**
  - Work underway
  - At the moment at most one trigger per readout frame ( limits triggers to few kHz )
- **Will enable trigger rates  $O(\text{MHz})$**

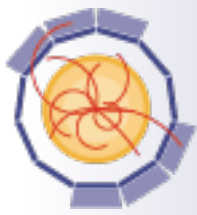


- **Current interface definition believed to be suitable for TPC**
- **AIDA TLU may be useful as basis for “Local TLU”**
  - Customize firmware

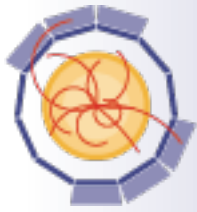


- **Common DAQ work-package can not succeed without partnership with other work-packages**

- Providing tools and standards for detectors wishing to work together.
- ( We can manufacture technical compliance with deliverables and milestones, but this isn't really success ).
- Your input vital.....

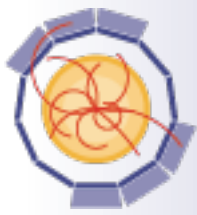


- **Freely available firmware and hardware blocks are starting to appear**
- **Worth considering when designing/modifying systems**
- **E.g. IPBus ( <http://cern.ch/cactus> )**
  - A32/D32 Wishbone-compatible bus in FPGA communicating with host over 1Gbit/s Ethernet
  - Used in TLU
  - Work in progress to offer 10Gbit/s link and “FIFO” interface as well as bus interface

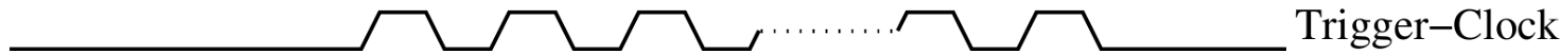
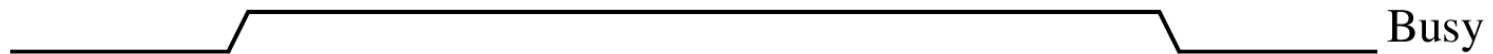
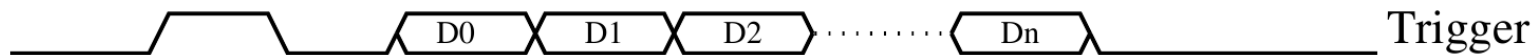
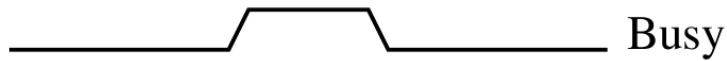


- **Support and develop EUDET/AIDA synchronization hardware (TLU)**
- **“Buy in” from detector groups vital.**
- **Designs , firmware, software easily accessible ( Open Hardware )**
- **More support effort available under AIDA-2020 than AIDA.**

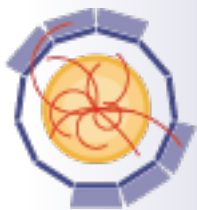
Backup



- **Different triggering modes:**
  - No handshake (trigger pulses high)
  - Trigger-Busy handshake
  - No system wide clock







### • System wide clock

- Allows higher trigger rate ( eliminates hand-shake latency)

