INFN-MIlano (65 nm CMOS)

Valentino Liberali

Department of Physics, Università degli Studi di Milano, and INFN
Via Celoria, 16 — 20133 Milano — Italy

valentino.liberali@unimi.it

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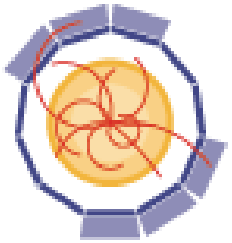
DI MILANO



AIDA 2020

AIDA-2020 Kick-Off Meeting, June 4, 2015

Outline

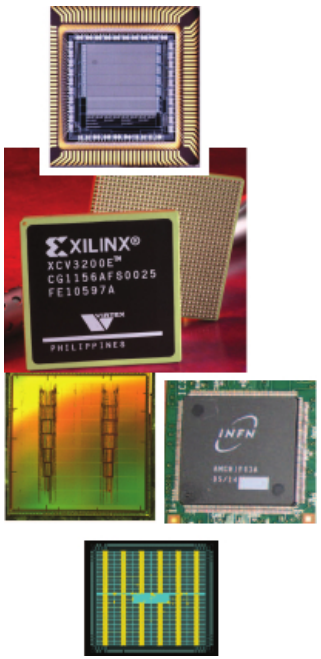
Previous Expertise

INFN-Milano design team:
Valentino Liberali, Alberto Stabile, Seyedruhollah Shojaii (chip design);
Mauro Citterio, Alessandro Andreani, Fabio Manca (PCB and chip assembling);
Alessandra Camplani (FPGA firmware and radiation tests)

Since 2010, **INFN-Milano in involved in the design of the Associative Memory chip for the Fast TracKer (FTK) project in ATLAS, using TSMC 65 nm CMOS technology**

The Associative Memory chip (AMchip) for FTK

Several versions of the AMchip:

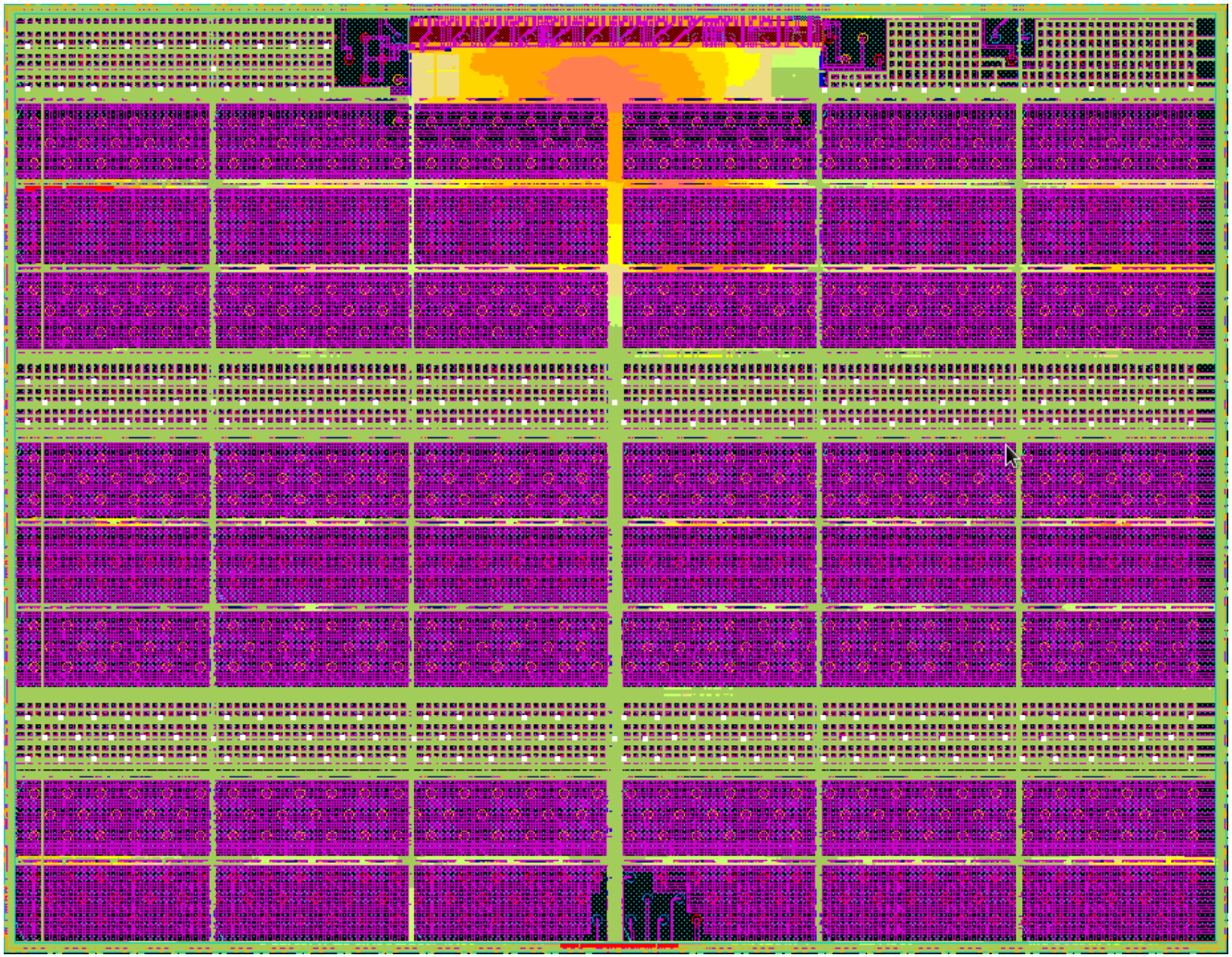


Vers.	*Design*	*Tech.*	*Area*	*Patterns*	*Package*
1	Full custom	700 nm		128	QFP
2	FPGA	350 nm		128	QFP
3	Std cells	180 nm	100 mm^2	5 k	QFP
4	Std cells + Full custom	65 nm	14 mm^2	8 k	QFP
mini-5	**Std cells + Full custom + SERDES IP blocks**	**65 nm**	**4 mm^2**	**0,5 k**	**QFP**
5			**12 mm^2**	**3 k**	**BGA**
6	**Std cells + Full custom + SERDES IP blocks**	**65 nm**	**160 mm^2**	**128 k**	**BGA**

blue = under design

AMchip06

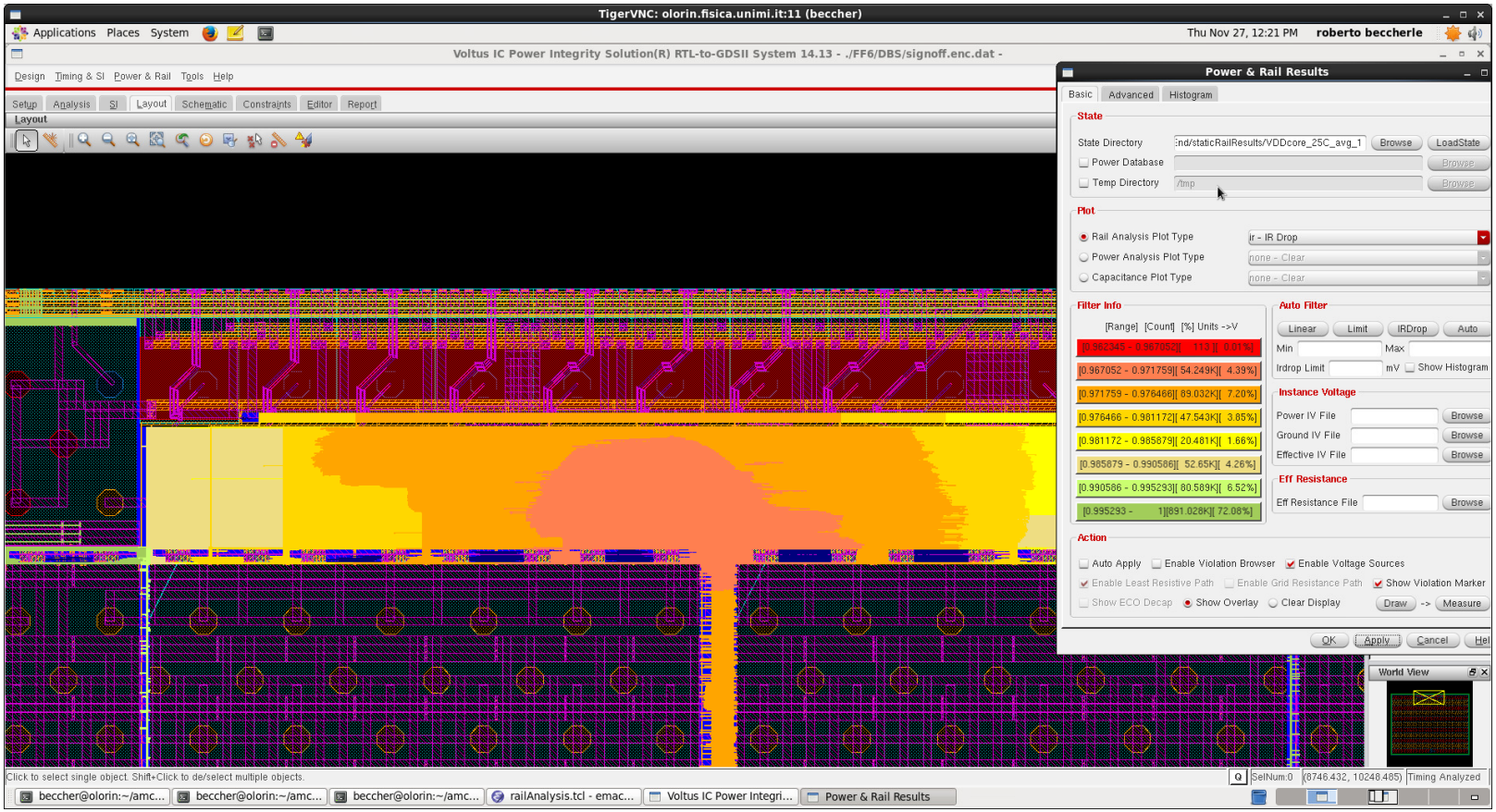
Last version: **AMchip06**
168 mm^2, 421 M transistors
Floorplan:



Expertise on Digital Design

Design of large IC's with Cadence Encounter
Mixed approach (full-custom, standard cells, IP blocks)
Use of timing analysis tools (Tempus) and *IR* drop analysis tools (Voltus)

Example: static *IR* drop for AMchip06 obtained from Voltus



Radiation Hardening Approach

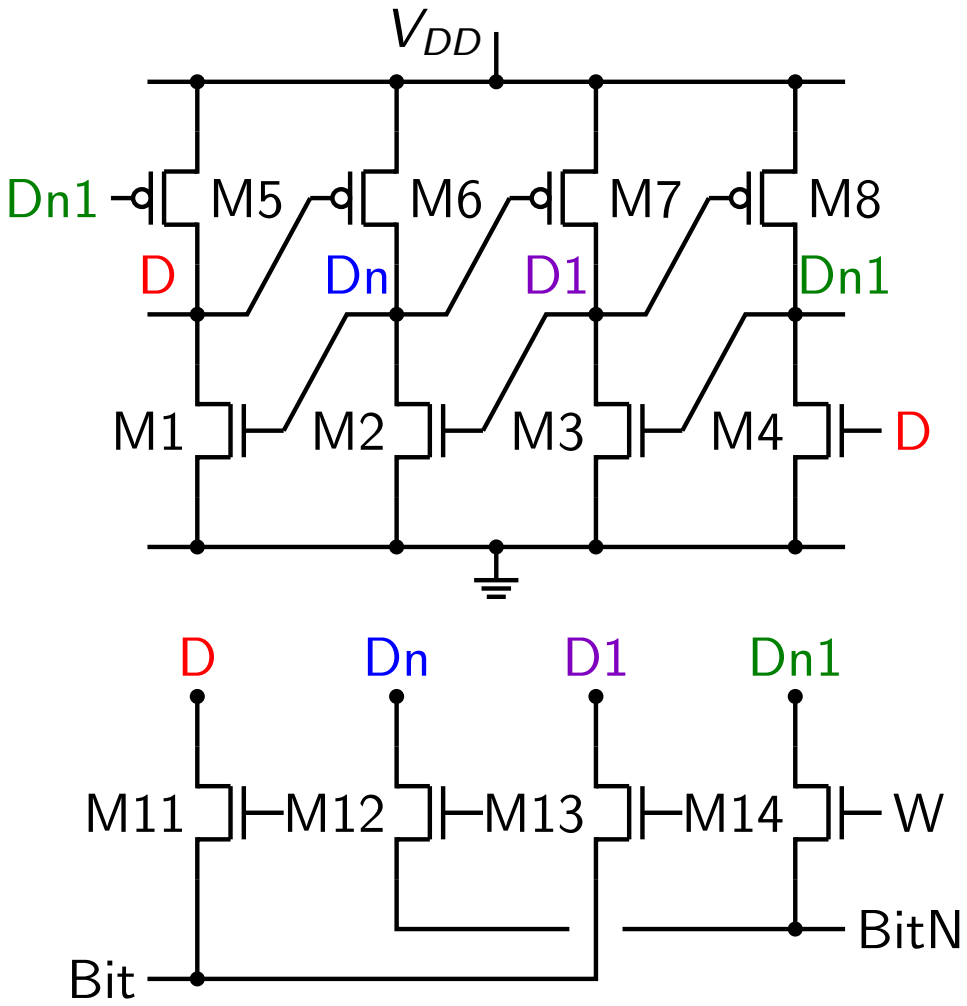
Within RD53/CHIPIX65:

Digital IP blocks designed in 65 nm CMOS technology (TSMC) using RHBD (Radiation Hardening By Design) techniques.

REDUNDANCY technique has been used for:

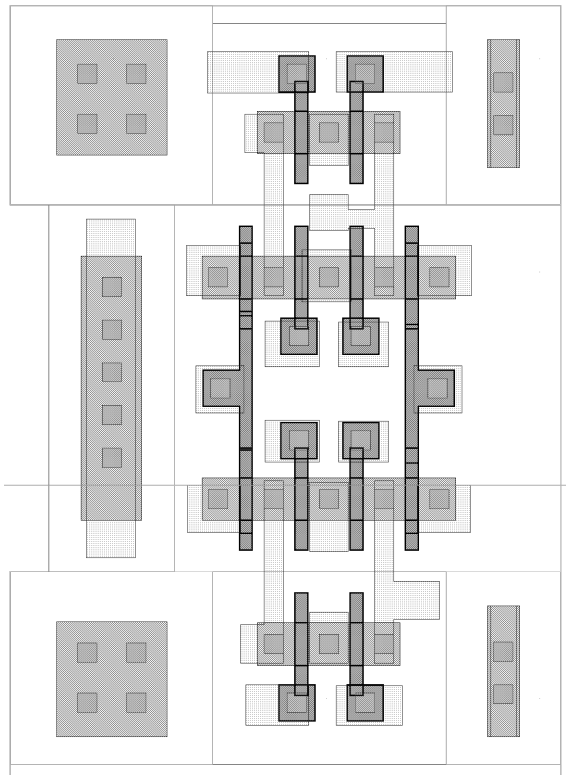
- DICE SRAM
  - Array of 256 $\times$ 256 cells designed with three different layouts
  - Prototypes available
  - Test board designed
  - Test firmware under development
  - Radiation test planned in July
- D2RA logic
  - New logic family based on redundancy: each signal is propagated on two wires (bit and inverted bit)
  - Cells designed
  - Test chip under design; MPW submitted in May

DICE (Dual Interlocked CEll) SRAM: schematic



T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology,", *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 2874-2878, Dec. 1996.

DICE (Dual Interlocked CEll) SRAM: layout

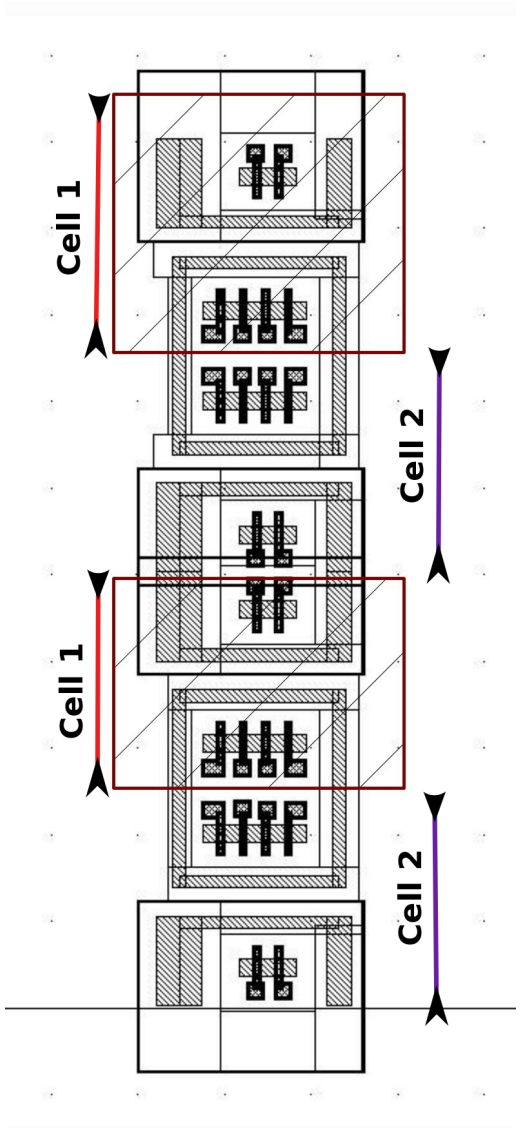


Simple layout

Minimum transistor size:
$W = 200$ nm, $L = 60$ nm

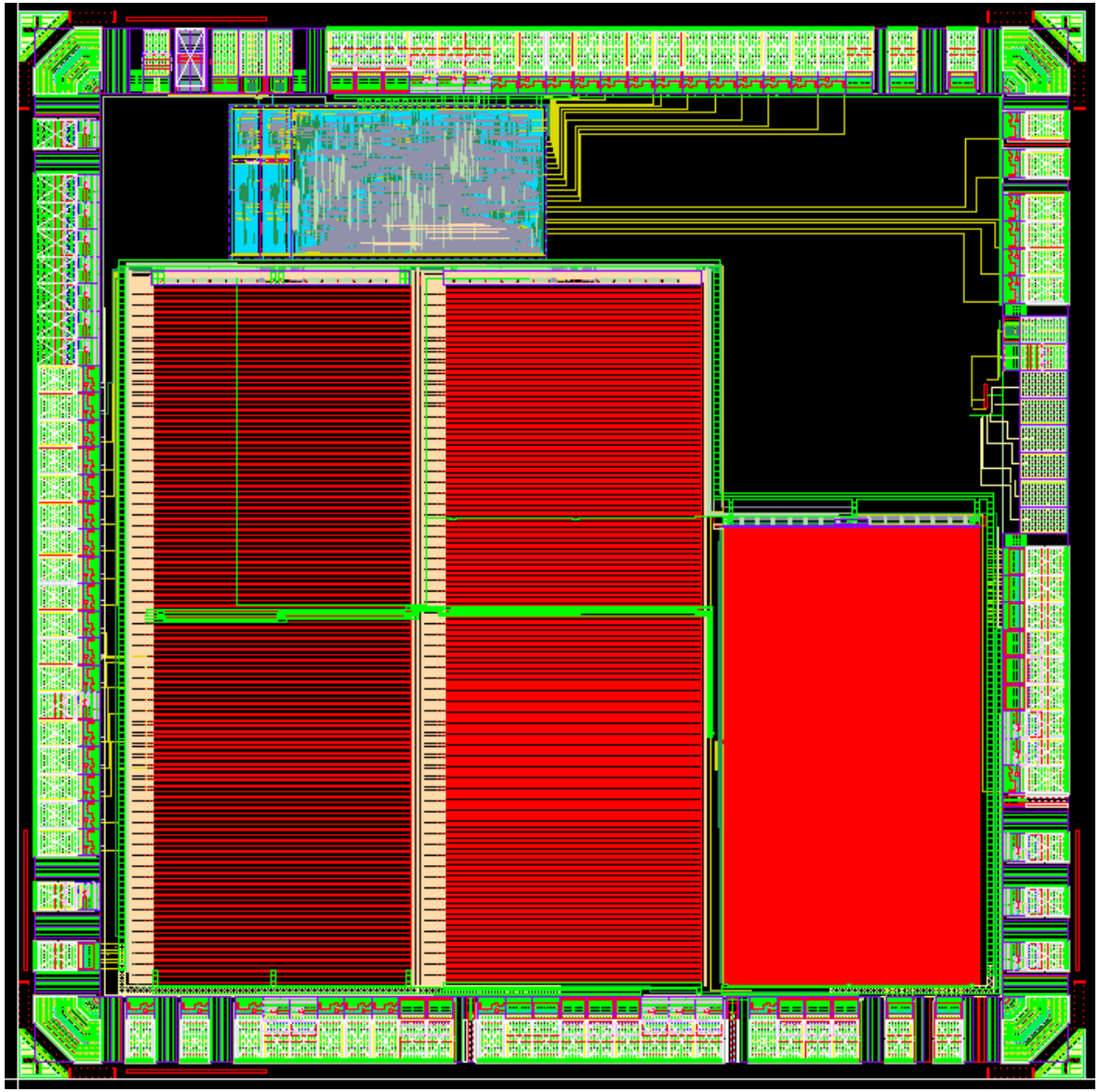
The cell has been designed in three different versions:

- "simple" layout
- with guard rings around transistors
- with both guard rings and interleaving



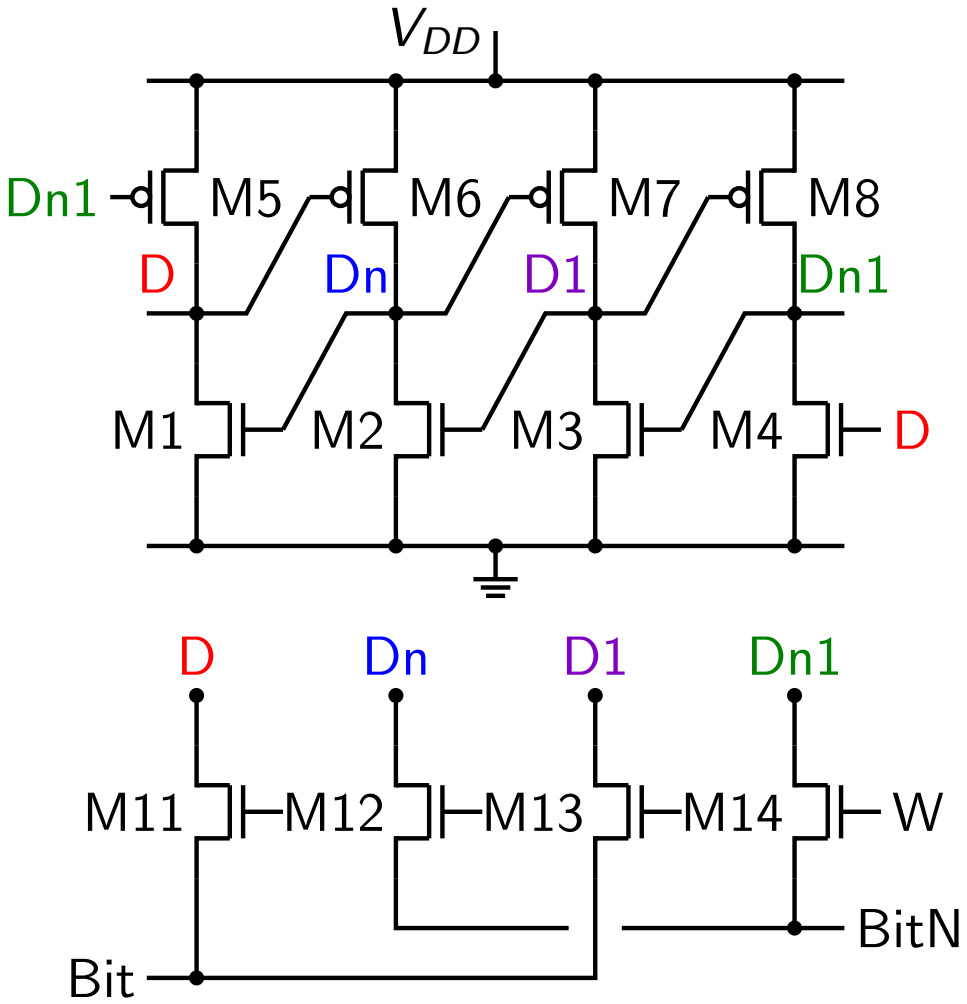
Interleaved layout

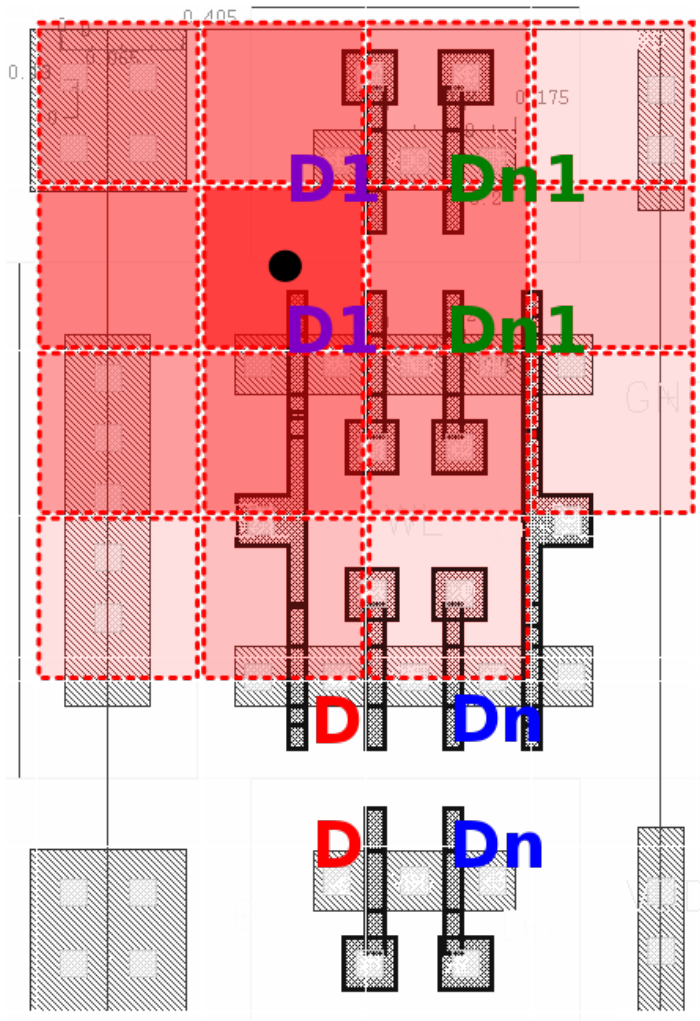
1st test chip: CHIPIX-SRAM-1



Layout:
3 256 $\times$ 256 SRAM arrays; SERDES; MOS transistors

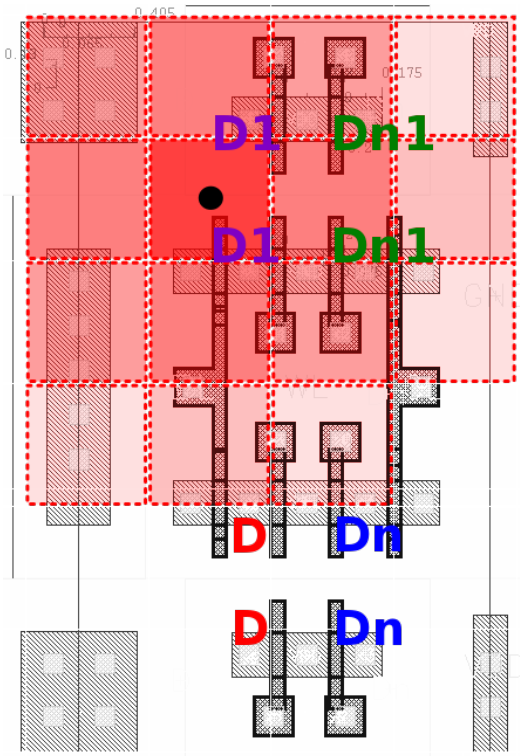
DICE Single Event Effect simulation

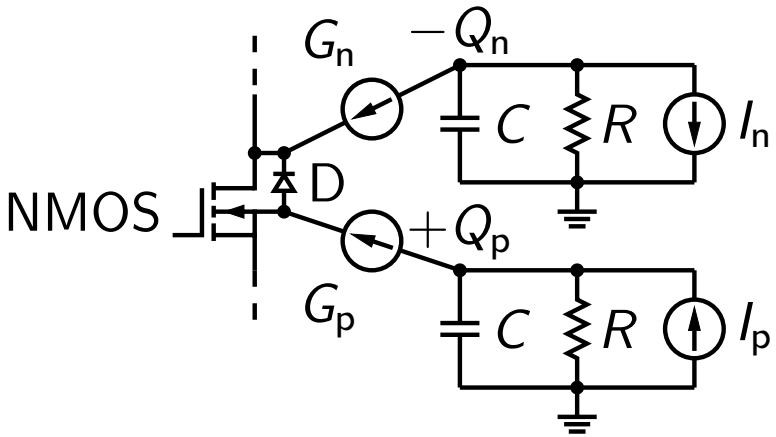




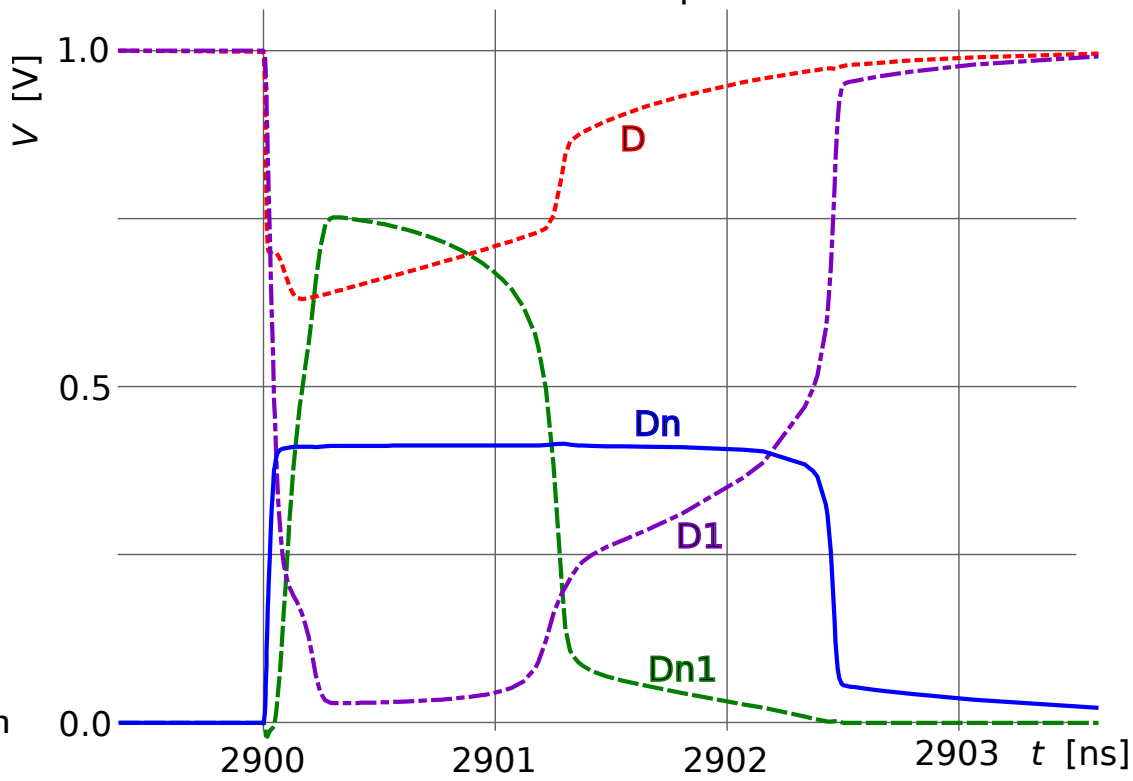
The area affected by a single particle is much larger than a single node!

DICE SEE simulation results





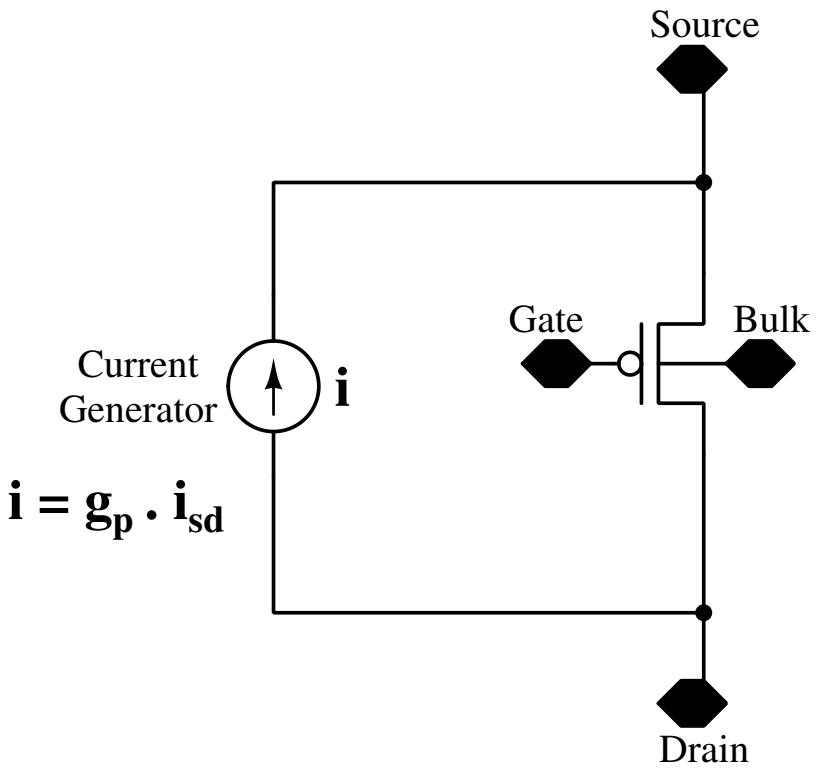
Total injected charge: $Q_p = Q_n = 1$ pC



After a 2.5 ns transient, the DICE memory reverts back to the correct value

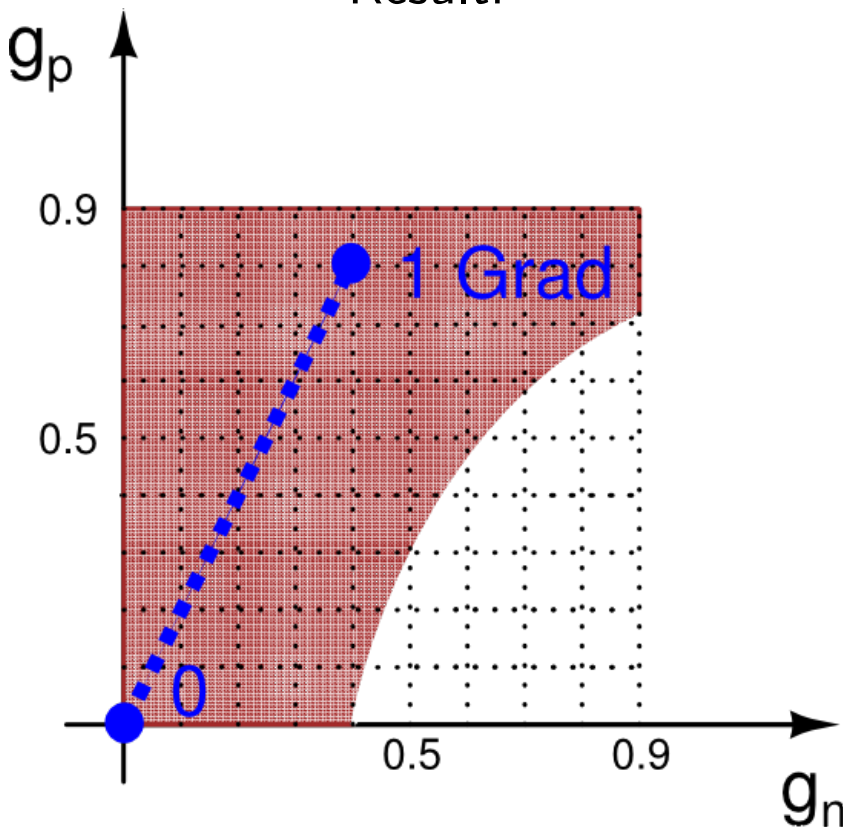
Total Dose simulation

Model:



The parameter g_p (g_n) accounts for the degradation of the PMOS (NMOS) transistor

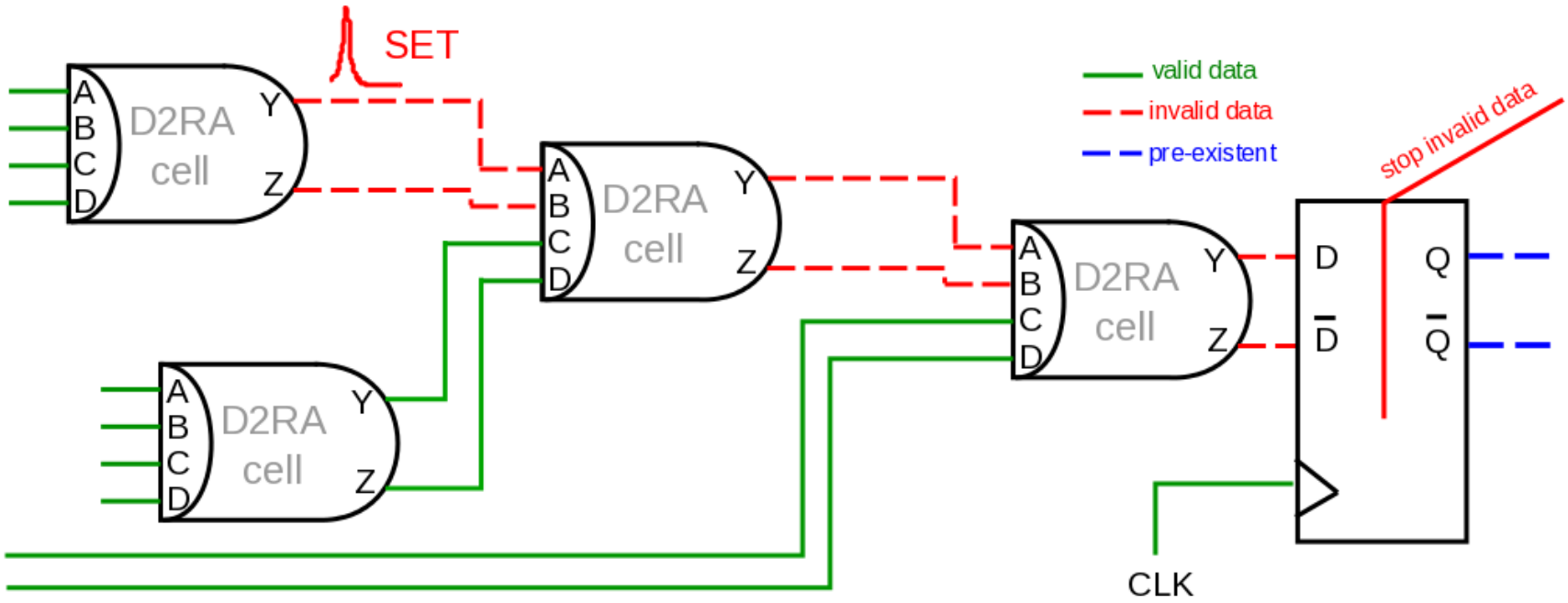
Result:



The DICE SRAM is less sensistive to PMOS conductance degradation

D2RA: Double-Rail Redundant Approach

Redundant logic which processes both the bit and the inverted bit
(01) and (10): valid data
(00) and (11): invalid data (Single Event Transient)



V. Ciriani, L. Frontini, V. Liberali, S. Shojaii, A. Stabile, and G. Trucco, "Radiation-tolerant standard cell synthesis using double-rail redundant approach," in *Proc. of Int. Conf. on Electronics, Circuits and Systems (ICECS)*, Sept. 2014, http://dx.doi.org/10.1109/ICECS.2014.7050063

D2RA Logic Gates

Combinational logic gates:

- AND / NAND
- OR / NOR (identical to AND / NAND with swapped inputs)
- XOR / XNOR (two identical "half-cells")
- MUX
- NOT (redundant inverter for single-ended signals)

Sequential logic gates:

- Edge-triggered delay flip-flop (D-FF)
- Clock edge detector

D2RA: Logic Constraints

Fully CMOS logic $\longrightarrow$ inverting logic gates

Correct points:
input valid data must give (**1**, **0**) or (**0**, **1**) at the outputs

Faulty points: **Invalid data** are represented by don't cares (-), which can be either (0, 0) or (1, 1)
Gravity points: 0000 and 1111 at the inputs must give (**1**, **1**) and (**0**, **0**) at the outputs, respectively

CD \ AB	00	01	11	10
00	**1**	-	-	-
01	-	**0**	-	**0**
11	-	-	**0**	-
10	-	**0**	-	**1**

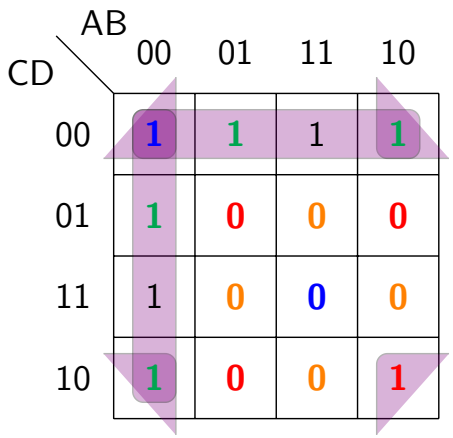
AND

CD \ AB	00	01	11	10
00	**1**	-	-	-
01	-	**1**	-	**1**
11	-	-	**0**	-
10	-	**1**	-	**0**

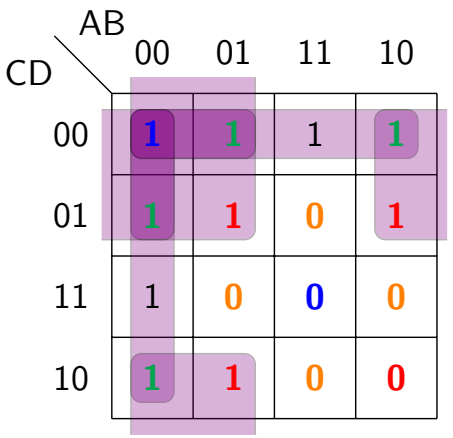
NAND

Synthesis of a 2-input D2RA AND-NAND

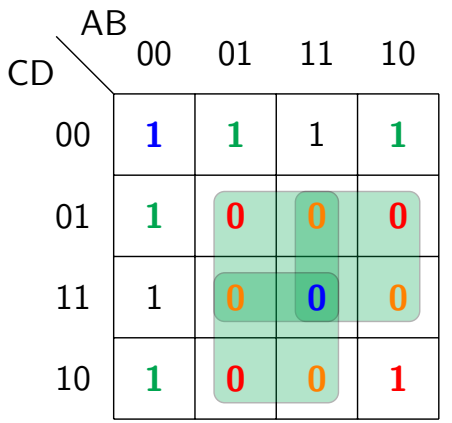
- For both gravity points find the square covers that include neighborhood
- Remaining don't care are filled with ones
- Find minimum covers



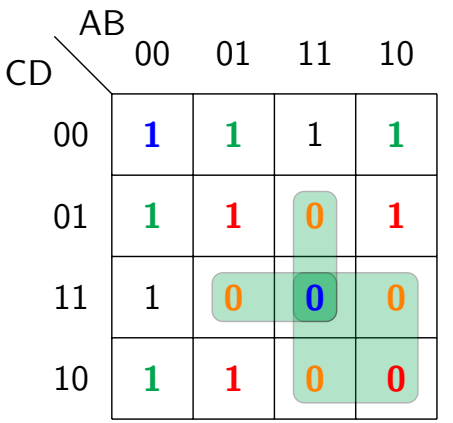
AND - Z output



NAND - Y output

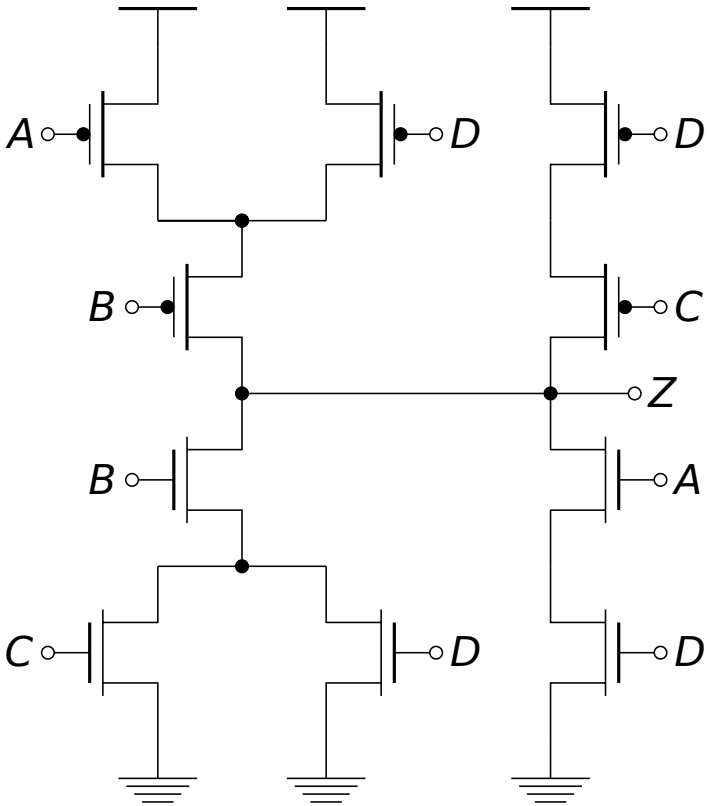


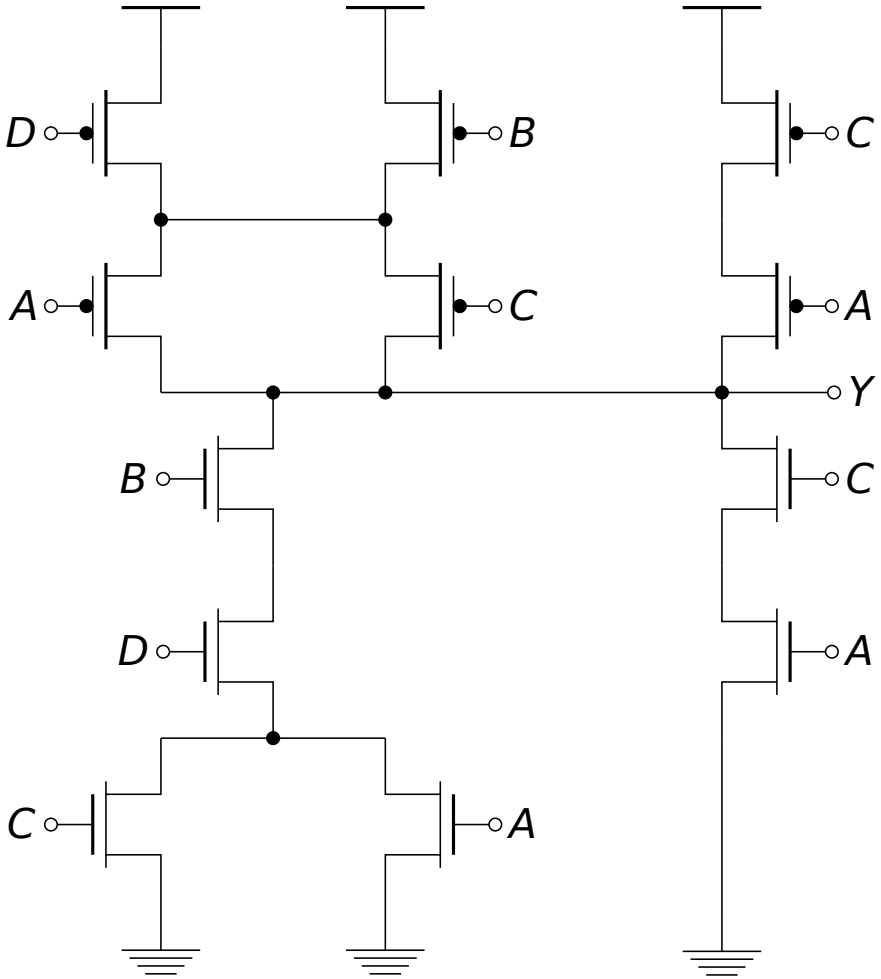
NAND - Z output



AND - Y output

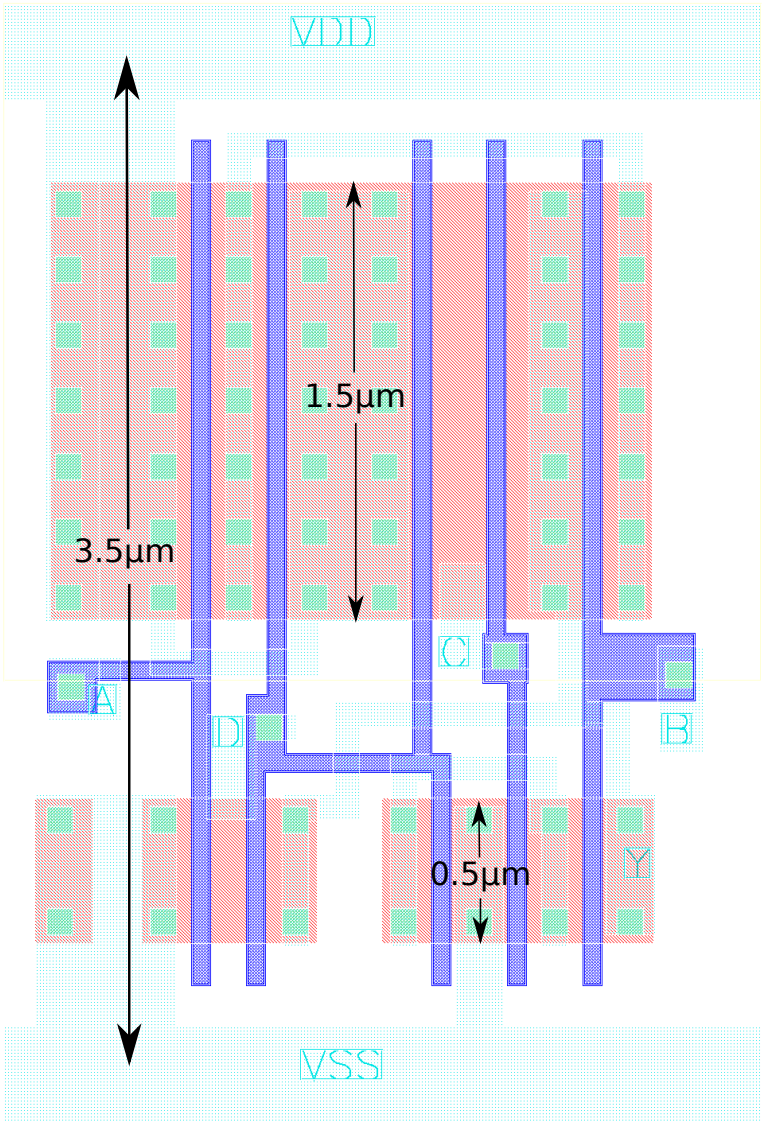
Schematic of a 2-input D2RA AND-NAND



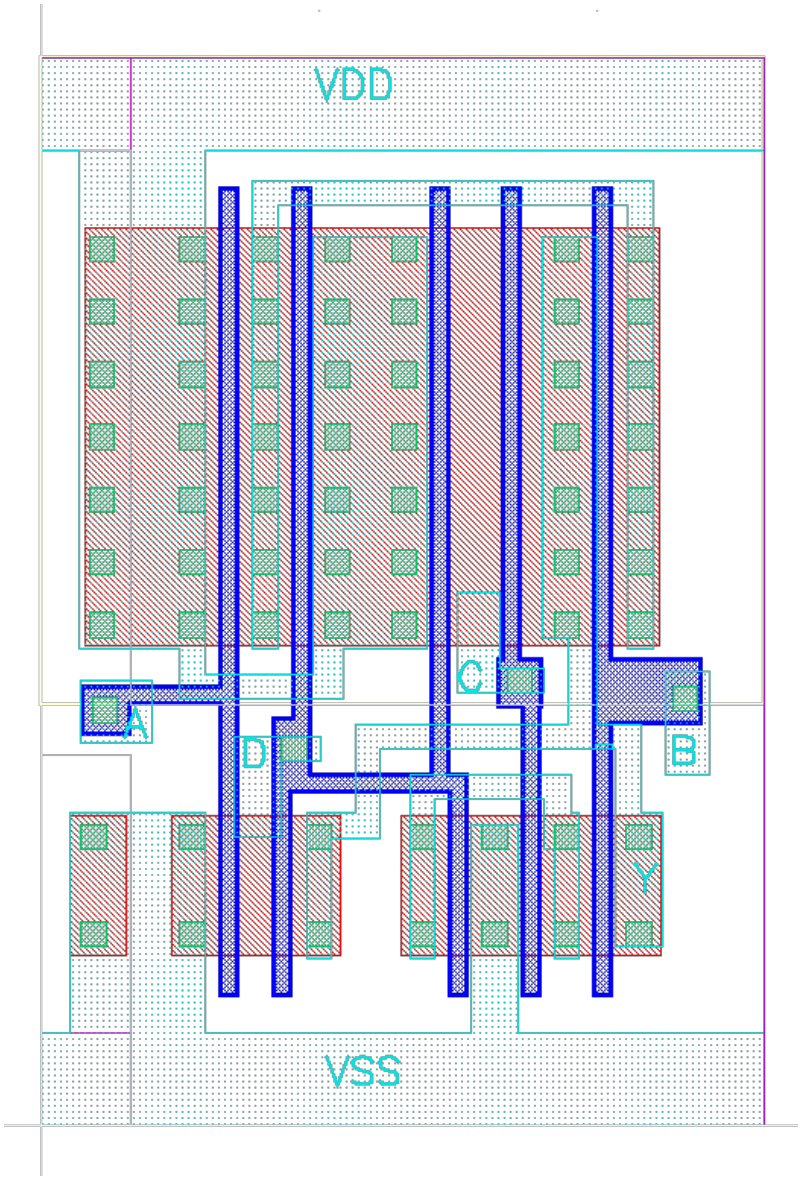


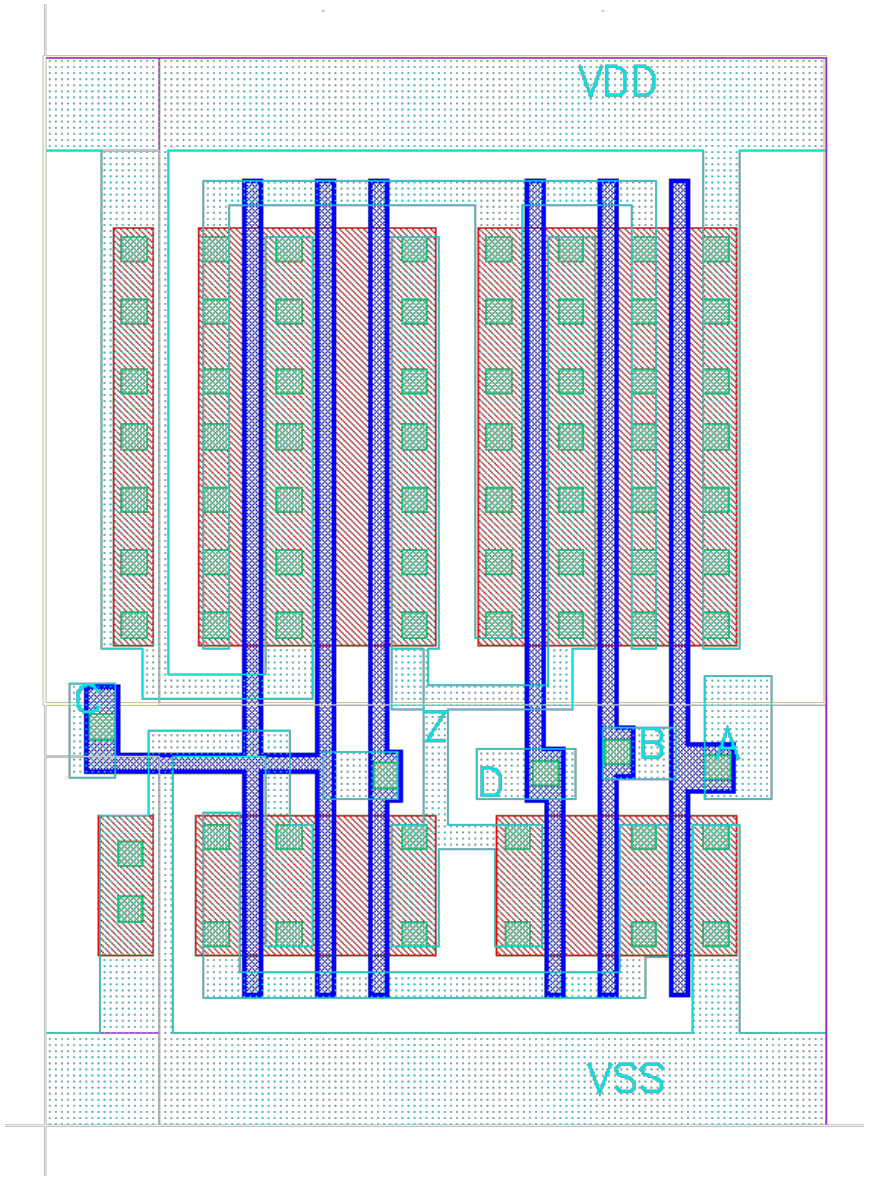
Layout approach for Standard Cells

- To reduce loss of transconductance at 10 MGy, transistors width is not minimum:
  $W_{\text{pmos}} = 1.5\,\mu\text{m}$
  $W_{\text{nmos}} = 0.5\,\mu\text{m}$
- Fixed cell height
- Power supply and ground nets at top and bottom of cells



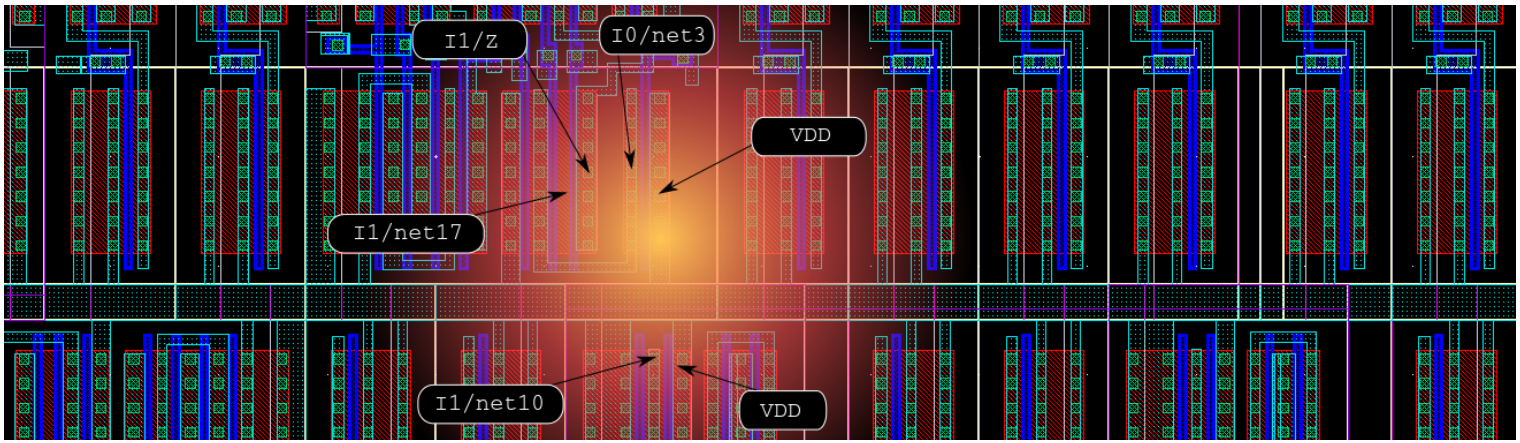
D2RA AND / NAND layout



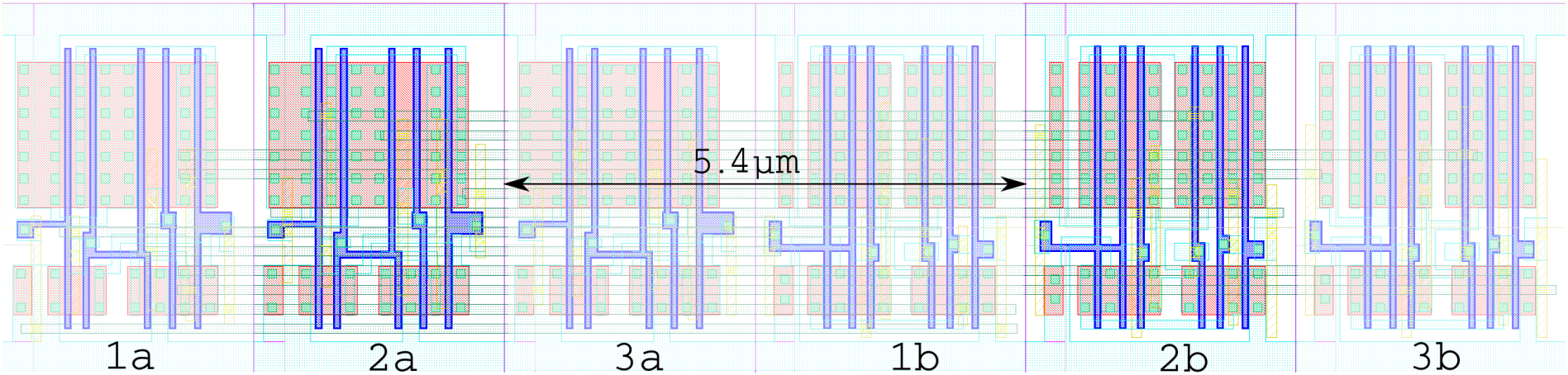


SET effect mitigation

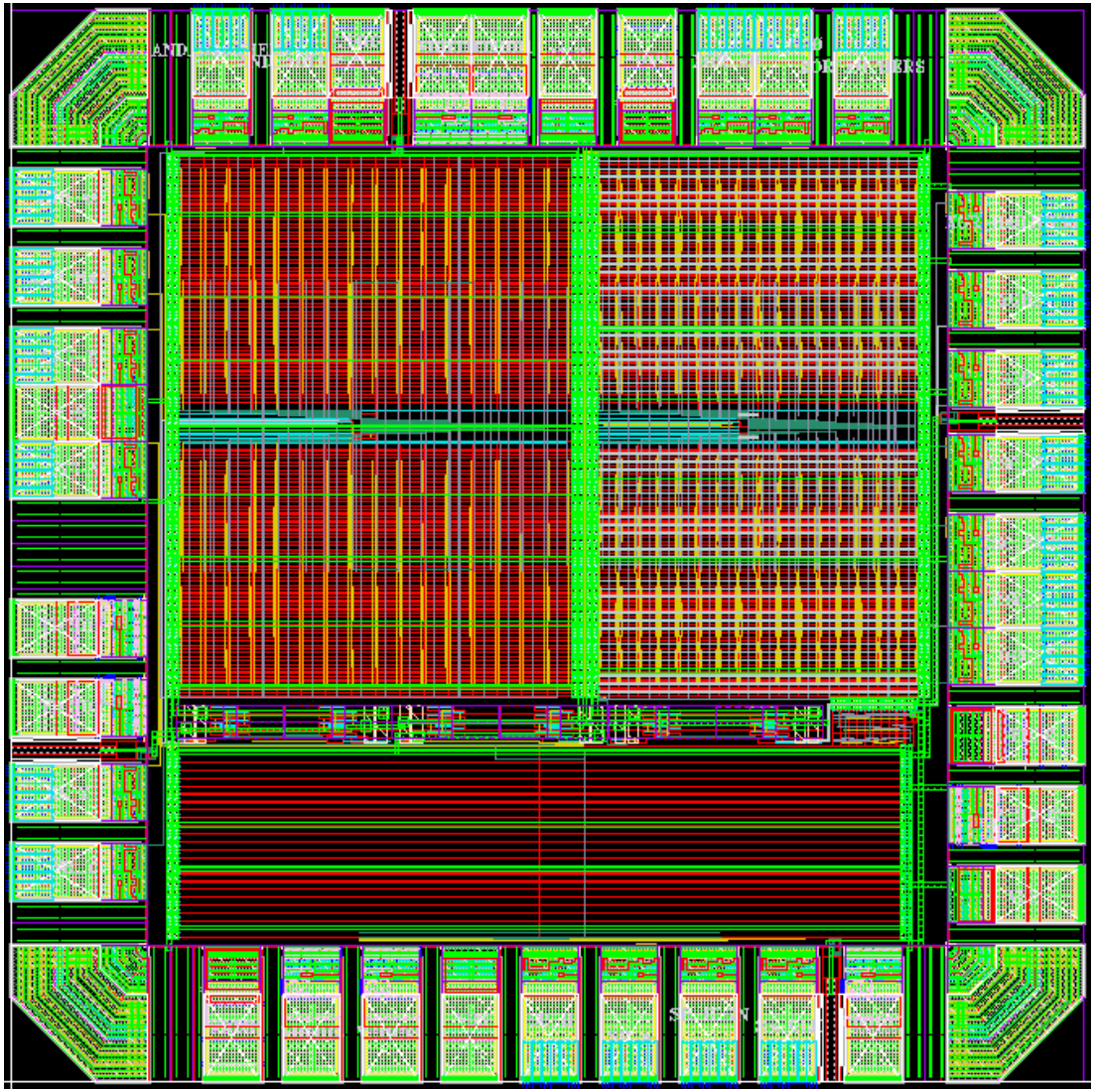
When radiation hits a circuit, the generated charge can affect several nodes causing SETs.



The two parts of a D2RA cell must be placed at a minimum distance of 5 µm:



2nd test chip: CHIPIX-D2RA-2



Layout:
AND/NAND and XOR/XNOR trees; shift register; ring oscillator
all designed with D2RA cells

Conclusion

- DICE SRAM available for test
- Simulation results show good immunity to both SEE and TID
- D2RA: new rad-hard logic family
- Logic cells design:
  - Combinational cells
  - Sequential cells
- Test chip designed and submitted

Future activities:

- Laboratory characterization and radiation test of prototypes
- Improvement of models for radiation simulation at circuit level
- Study of combined TID/SEE effects in 65 nm
- Develop a methodology for radiation hardness verification at layout level