WP 6 / NA5 – Task 4

AIDA-2020 Kick-off meeting

4 June 2015

Giovanni Darbo – INFN / Genova

WP6.4 deals with development of capacitive interconnections

Perform basic R&D on capacitive interconnection for electrical test structures and using different adhesives and gluing techniques. Optimise gluing process for precise alignment, high and uniform capacitance and sufficient yield and reproducibility…

Task 6.4 - Hybridization

***Task 6.4 Beneficiaries and (INFN) interested groups**:*

- **INFN-GE**, IFAE, UNILIV
- Additional INFN groups involved: Milano.

Activities on HV/HR-CMOS hybridization funded by 3 year INFN project:

- 2015 – 2017
- INFN Interested not only on hybridization but in the whole HV/HR-CMOS project: **chip design, assembly with R/O, module test in the lab, at test beam and with irradiation**

Preliminary studies and on-going activities reported in the next slides:

- Process studied is front-end to HV/HR-CMOS chip gluing (chip-to-chip)
- Test with dummies – achieved results and future plans
- Prototypes with available HV-CMOS chip and FE-I4 R/O chip

CCPD – Capacitively Coupled Pixel Detectors

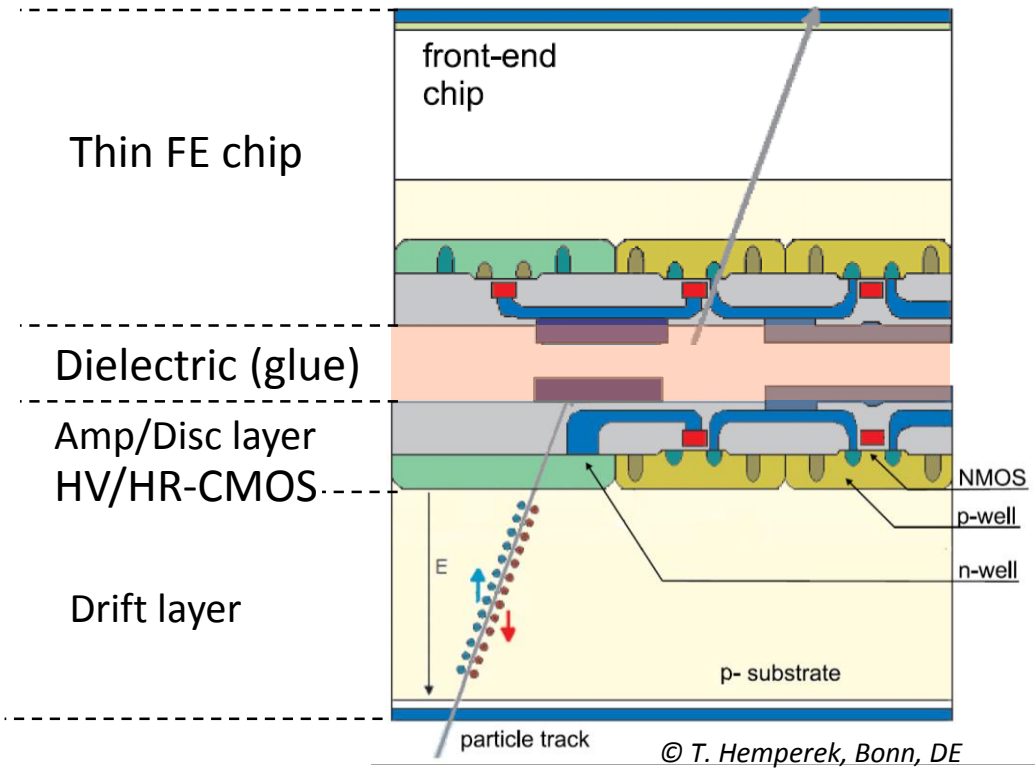
New generation of Pixel detectors under development for the ATLAS Pixel detector at the HL-LHC

- Passive hybrid detectors use "resistive" coupling between sensor and R/O chip
- HV-CMOS detector use a High Voltage chip technology to make sensor and amplifier which is then coupled to the "usual" front-end chip…

- through a dielectric…

Why capacitive?

- Passive sensors need diode biasing from amplifier other than for collecting charge: AC coupling is (almost) not an option.
- **Capacitive coupling it might be cheaper**: glue and alignment looks easier.



© T. Hemperek, Bonn, DE

(Some) Requirements

- *Capacitance uniformity*
  - Between pixels, from an assembly to another: ~10 % → thickness uniformity
  - Most critical for analog coupling (no discriminator in the HV/HR-CMOS)
  - RD-53 chips will have 50µm pitch, but also versions for very small pixels: 25µm pitches are considered
  - X-Y alignment: better than few µm (cross talk / signal loss)

- *Glue requirements*
  - Low viscosity: 0.1 ÷ 0.5 Pas
  - Radiation hard: epoxy
  - Not degassing
  - Low temperature curing, investigating UV/Temp curing glues
  - Minimum thickness of glue to give for full adhesion (usual specs are 1-2 mil, but we want less!)

- *For chip-to-wafer and wafer to wafer TVS are needed on one or both facing chips*
  - For the moment we are looking at chip-to-chip processes

Controlled Glue Thickness

Procedure for Controlled Glue Thickness

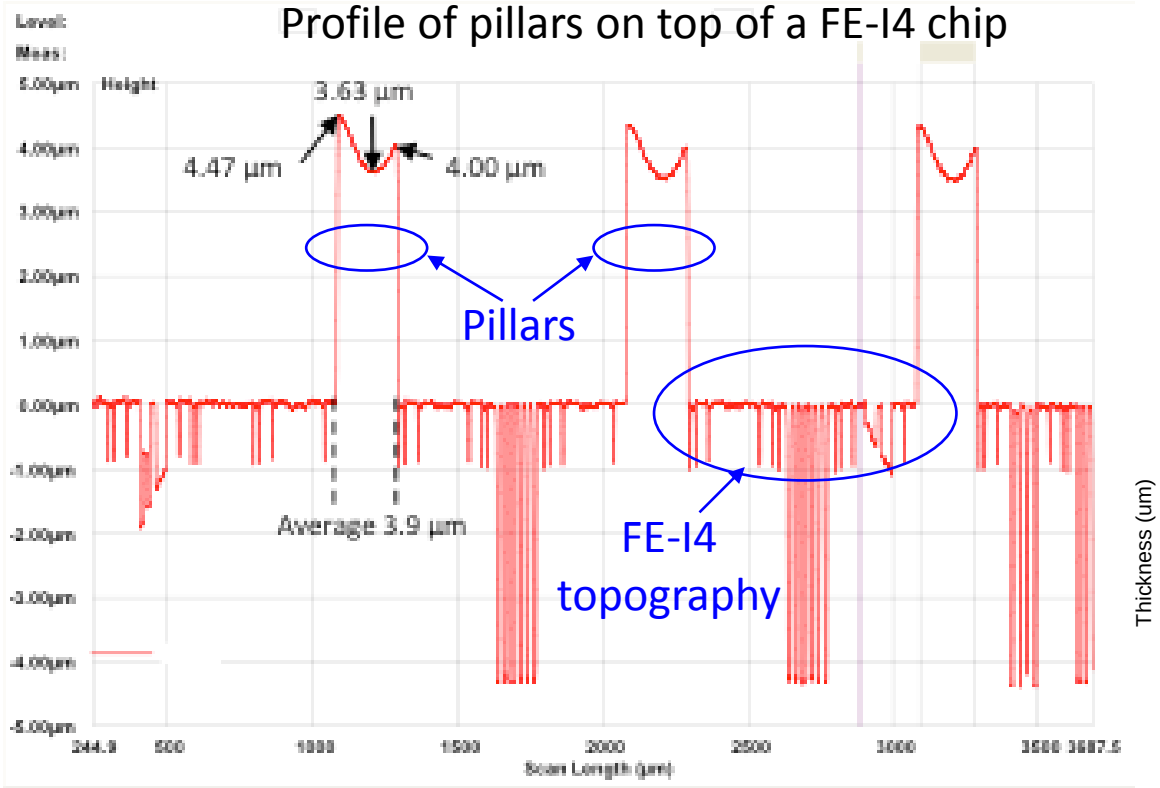
- Deposit uniform layer of SU8 photoresist on R/O chip wafer (or single chip) by spinning – tune for 5 µm layer by controlling RPM speed
- Pattern pillars using lithographic process .

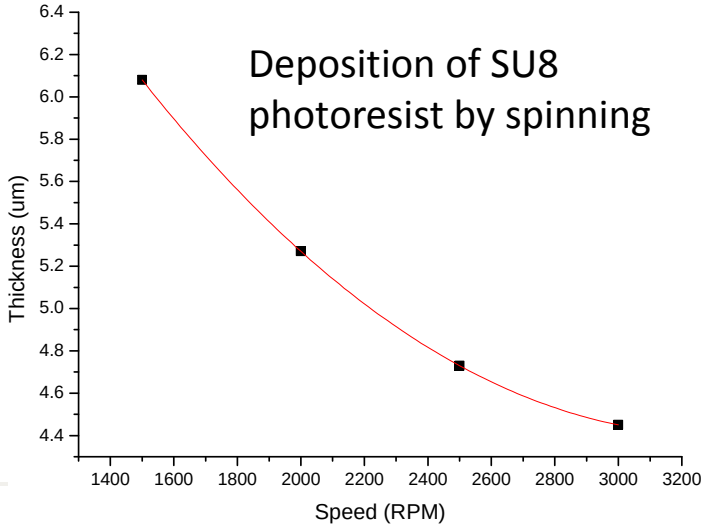
Spin SU-8 photoresist
Pattern pillars by mask

Glue deposition

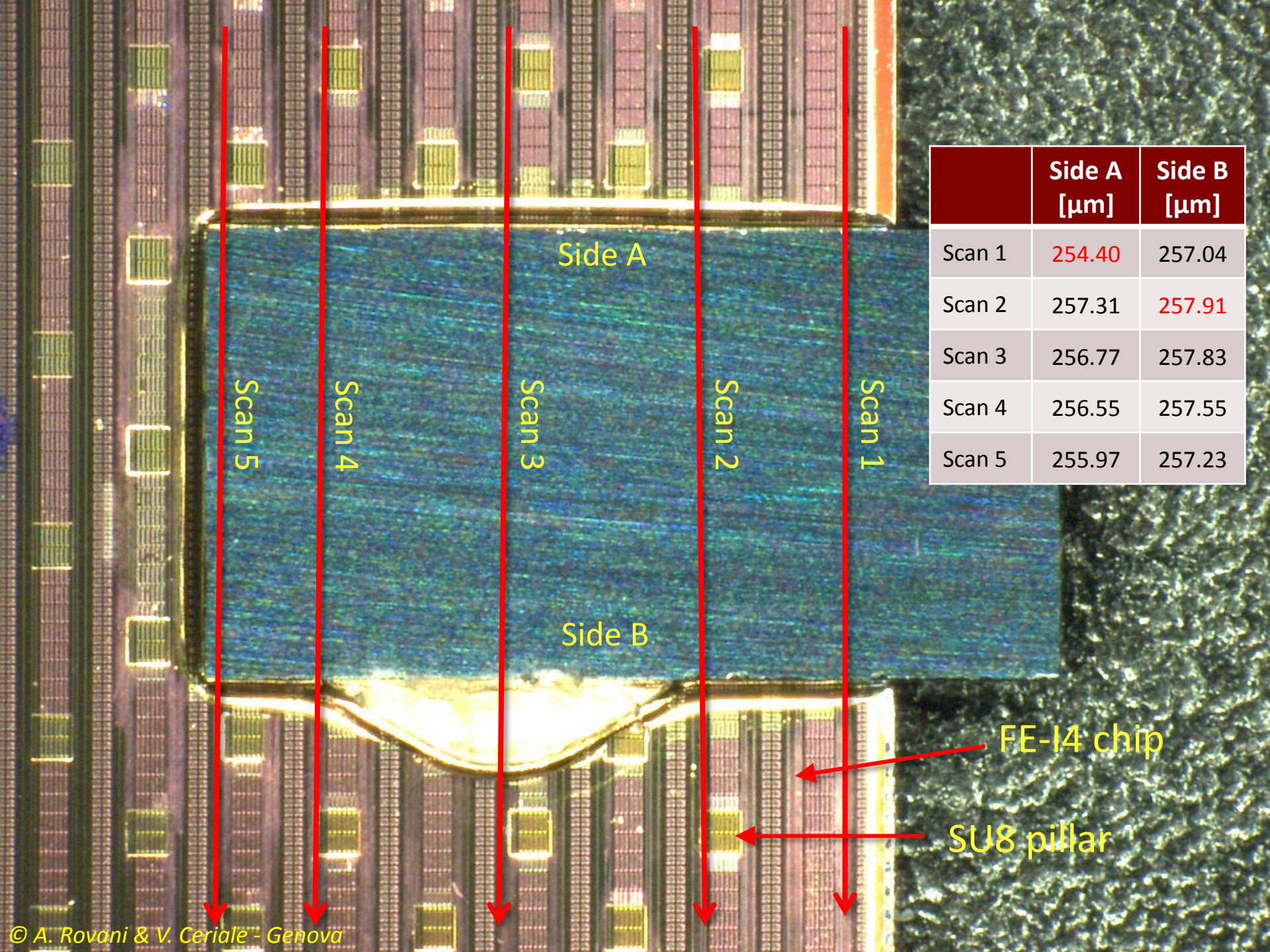
Align & pressure

Profile of pillars on top of a FE-I4 chip





Deposition of SU8 photoresist by spinning



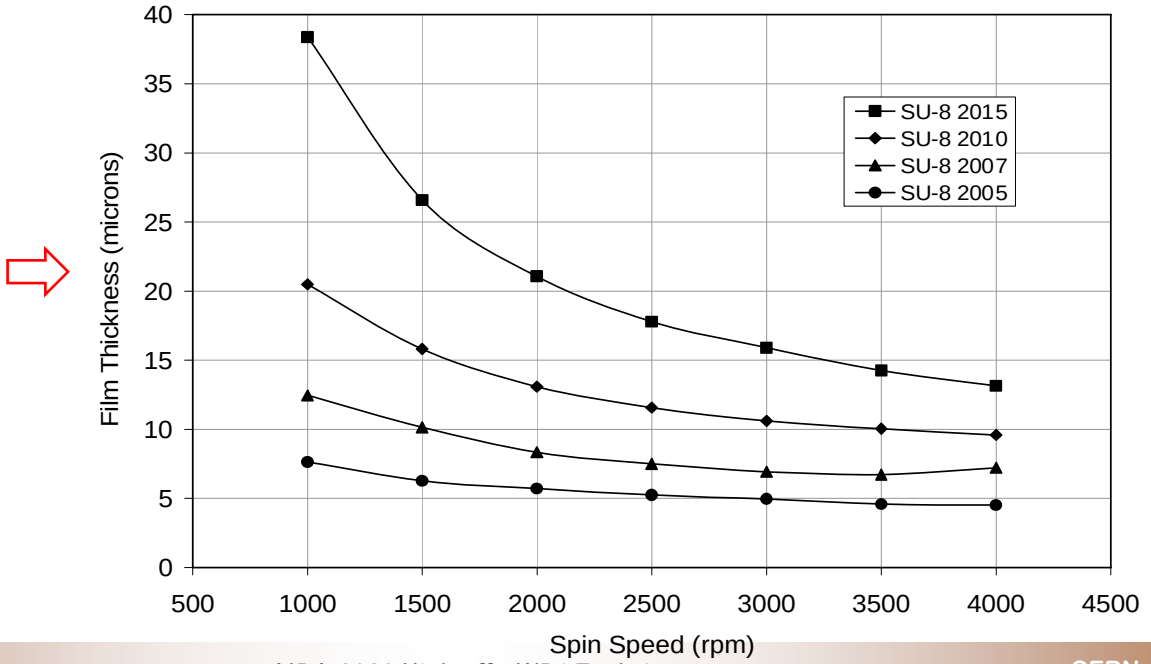
	Side A [µm]	Side B [µm]
Scan 1	254.40	257.04
Scan 2	257.31	257.91
Scan 3	256.77	257.83
Scan 4	256.55	257.55
Scan 5	255.97	257.23

Basic CCPD Process under Study

Pillars can be produced by standard lithographic processes:

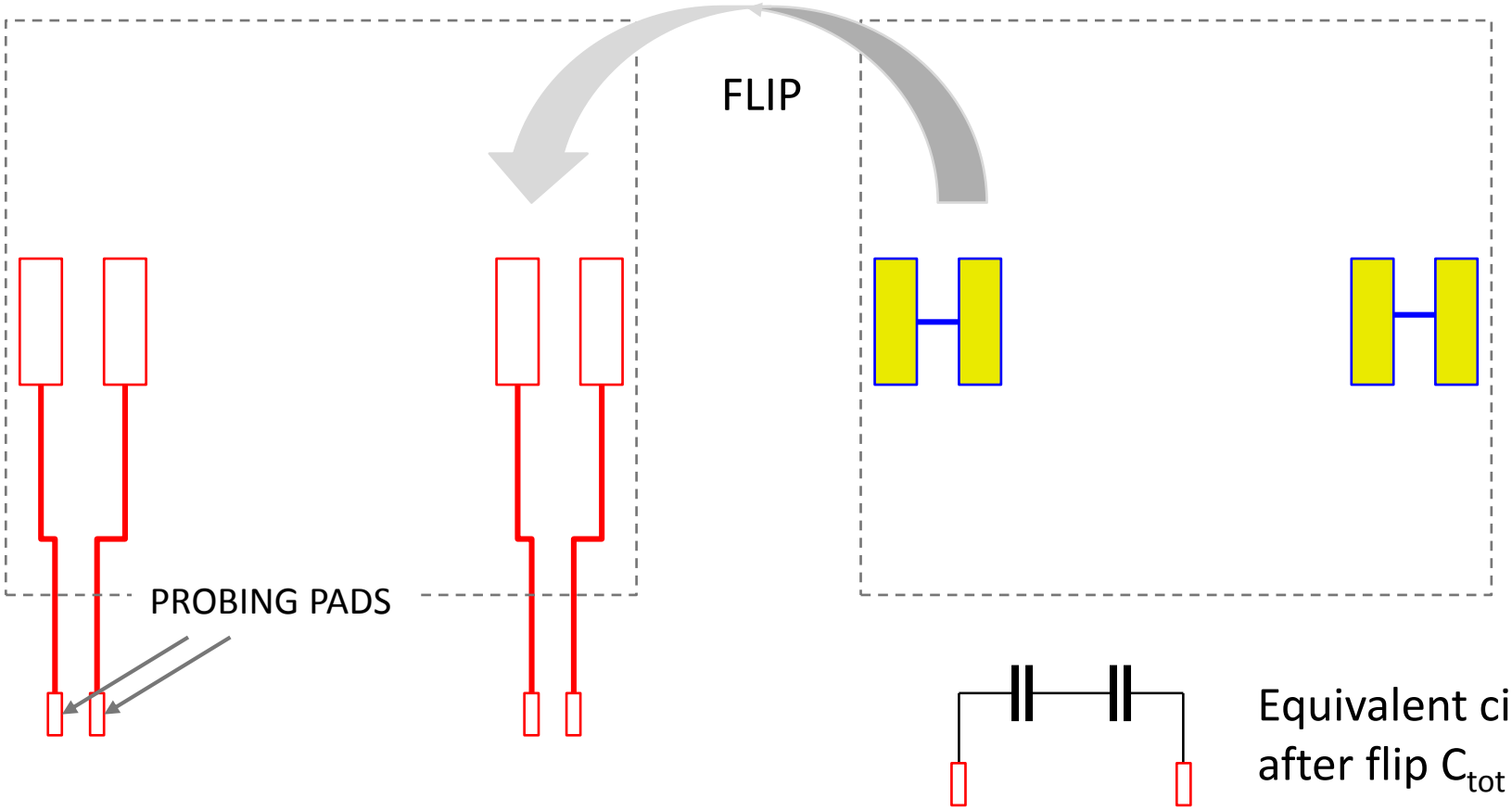
- SU8 photoresist deposition (3 – 5 µm thickness) by spinning on 8 – 12-inch wafers (for testing we could use 6-inch wafers)
- Pillars are made by mask as for bump-bonding openings in the photoresist
- Chips need alignment after a glue is deposited (flip-chip machine)
- Glue polymerization by UV light (tacking) and complete process in an oven

- SU8 deposition by spinning

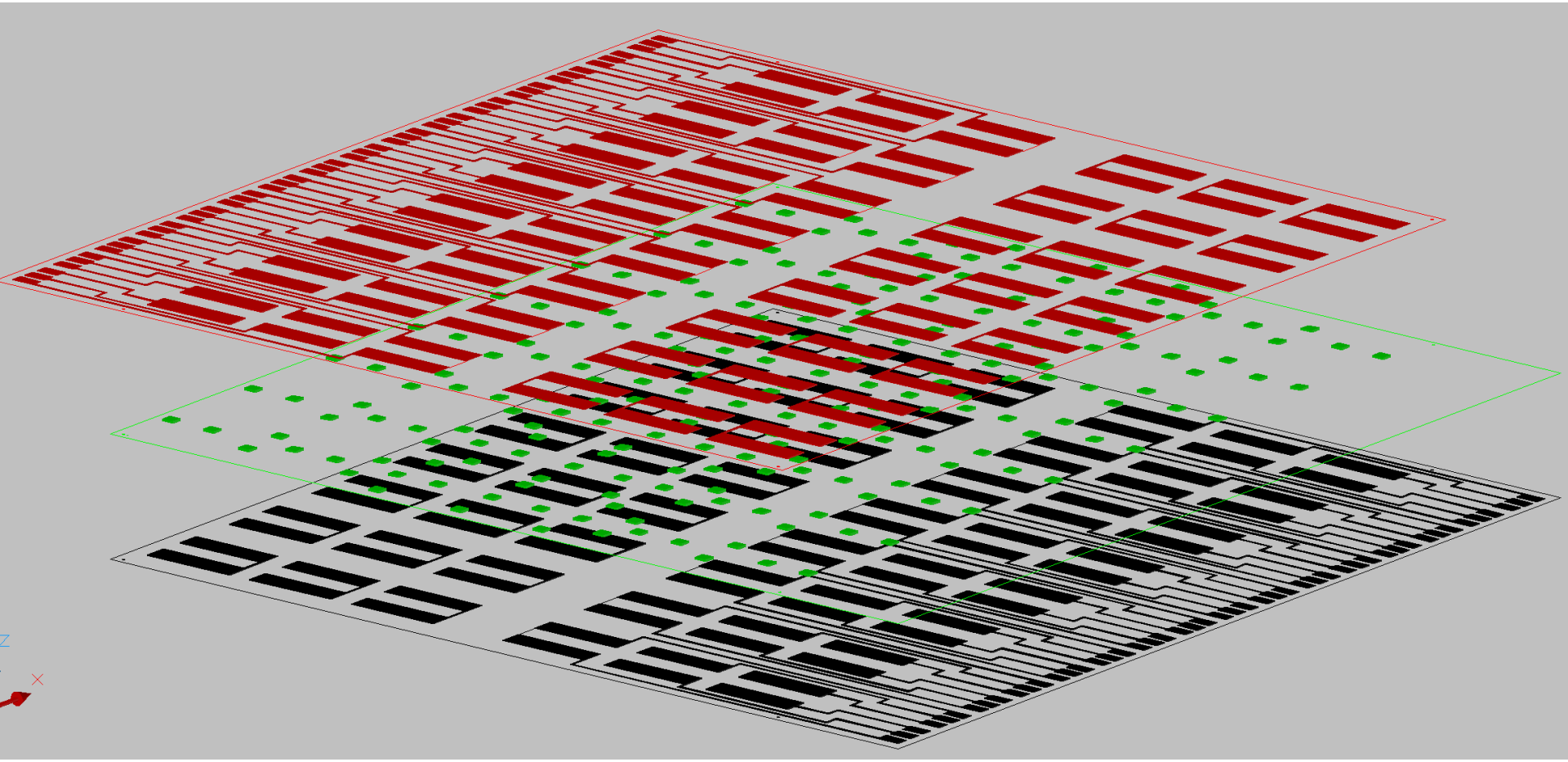


Plan for Hybridization – Dummy wafers

- *Test pillar and glue process on dummy wafers/chips*
  - Design a 6-inch wafer with FE-I4 size dummies
    - Place 48 capacitors of 1 mm^2 each on every dummy chip.
    - Capacitance gives information of glue thickness uniformity

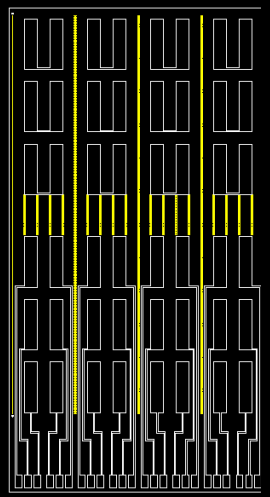


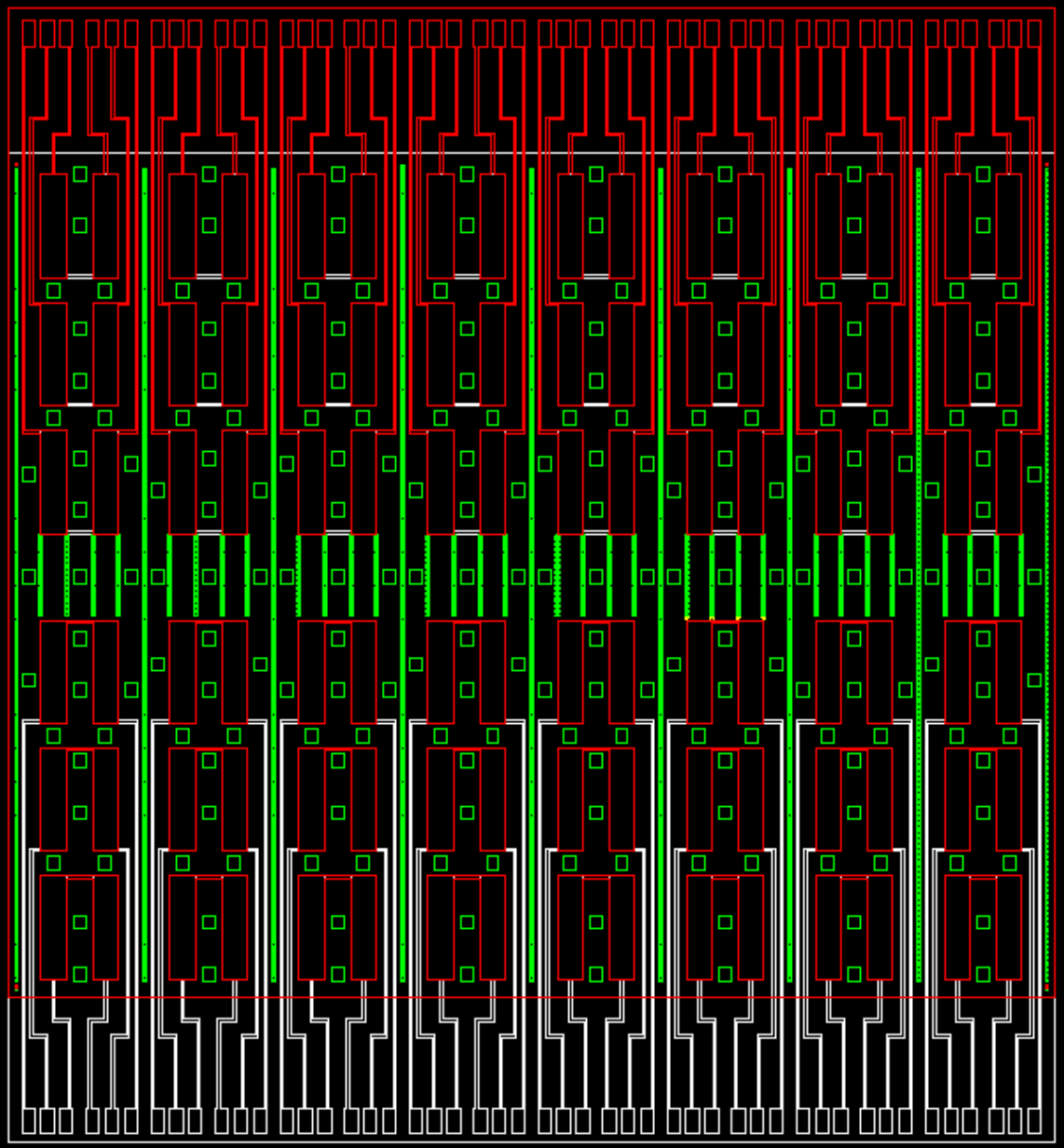
Dummy Assembly

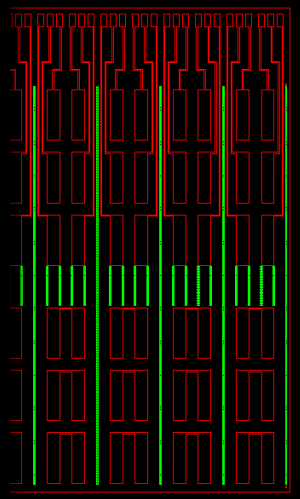


Credits: Alessandro Rovani – INFN / Genova

Overlaid – Bottom metal + SU8 pillard + Top metal

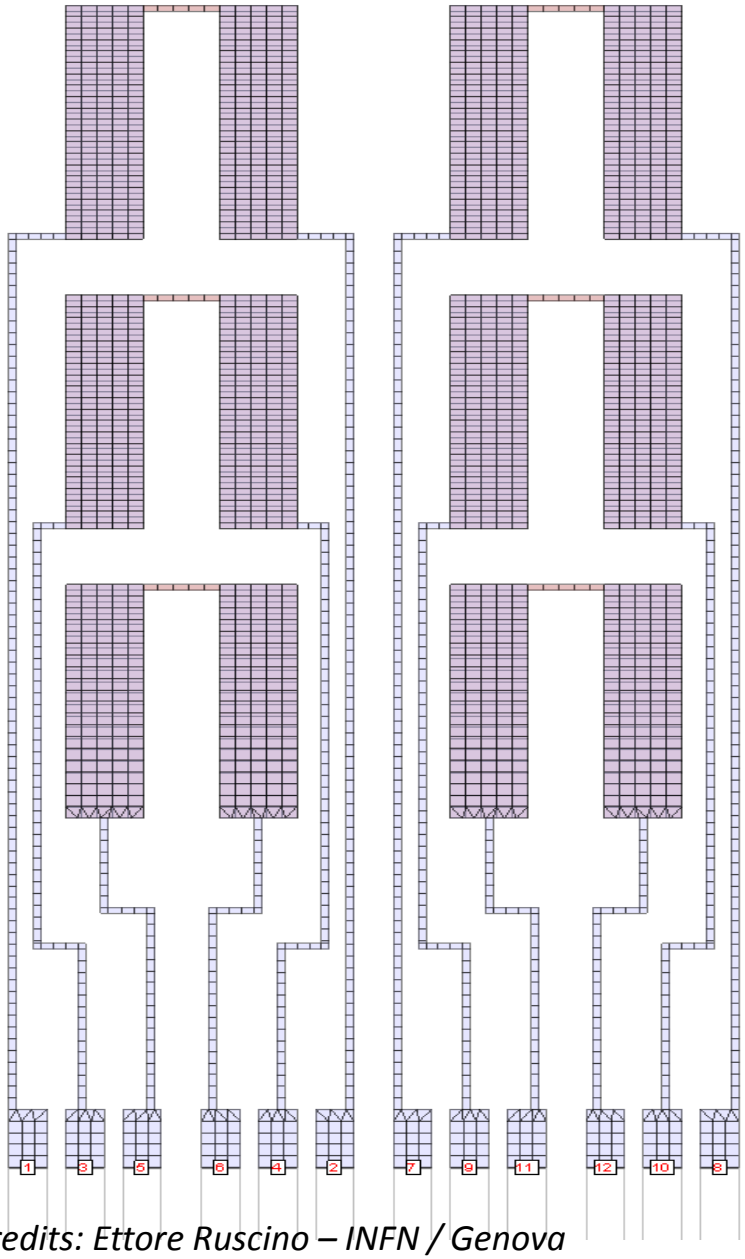






Credits: Alessa

3D Simulation - HyperLynx® 3D EM



Credits: Ettore Ruscino – INFN / Genova

	#	Z
☑	6	1306.000000
☑	5	656.000000
☑	4	655.500000
☑	3	650.500000
☑	2	650.000000
☑	1	0.000000
☑	A	3D Polygon

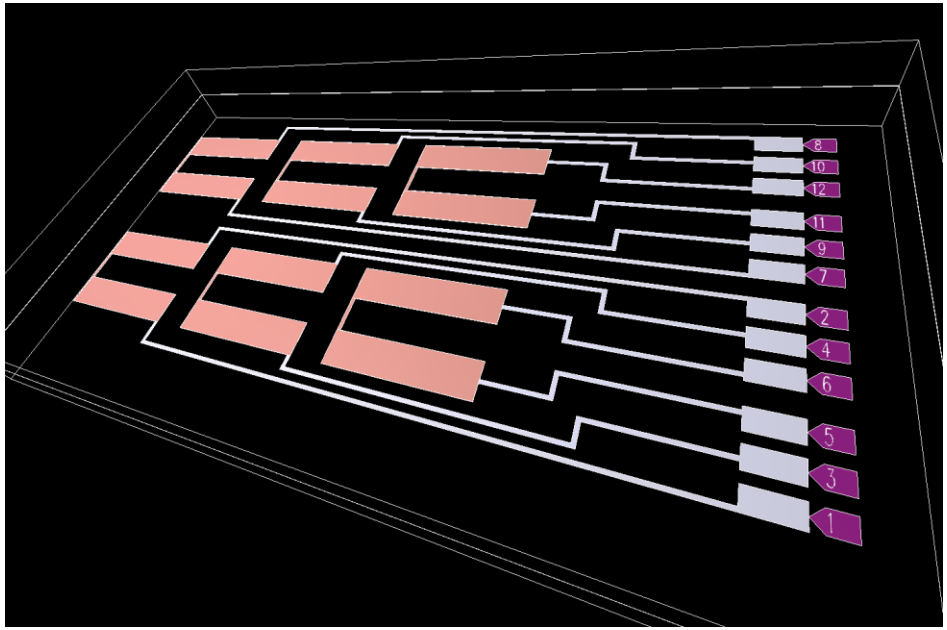
5µm dielectric thickness

Stack-up:

Substrate Layers | Metallic Strip Types | Finite Dielectric Types

Conductor Assumption Limit: 1000000 Max DK: 500 Display Margin: 1000 Default Transparency 0 Merge

No. 6:	D	Ztop=1e+018	T=1e+018	Epsr=1	TanD(E)=-0	Mur=1	TanD(M)=-0	Sigma=(0, 0)	Ei=0	Fd=0	Cmt=AIR
No. 5:	D	Ztop=1306	T=650	Epsr=11.7	TanD(E)=0.005	Mur=1	TanD(M)=-0	Sigma=(0, 0)	Ei=0	Fd=0	Cmt=Silicon_Top
No. 4:	D	Ztop=656	T=0.5	Epsr=3.9	TanD(E)=0.001	Mur=1	TanD(M)=-0	Sigma=(0, 0)	Ei=0	Fd=0	Cmt=SiO2_Top
No. 3:	D	Ztop=655.5	T=5	Epsr=3.8	TanD(E)=0.012	Mur=1	TanD(M)=-0	Sigma=(0, 0)	Ei=0	Fd=0	Cmt=Glue
No. 2:	D	Ztop=650.5	T=0.5	Epsr=3.9	TanD(E)=0.001	Mur=1	TanD(M)=-0	Sigma=(0, 0)	Ei=0	Fd=0	Cmt=SiO2_Bottom
No. 1:	D	Ztop=650	T=650	Epsr=11.7	TanD(E)=0.005	Mur=1	TanD(M)=-0	Sigma=(0, 0)	Ei=0	Fd=0	Cmt=Silicon_Bottom
No. 0:	G	Ztop=0 Epsr=1	TanD(E)=-0	Mur=1	TanD(M)=-0	Sigma=(4.9e+007, 0)	Ei=0	Fd=0	Cmt=GND		

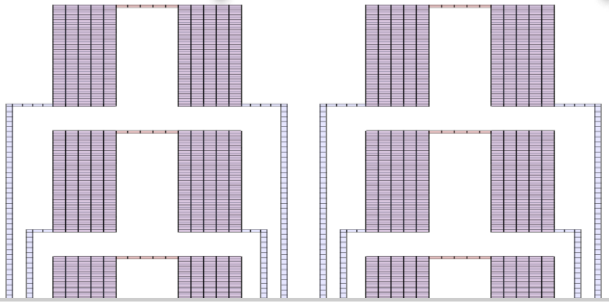


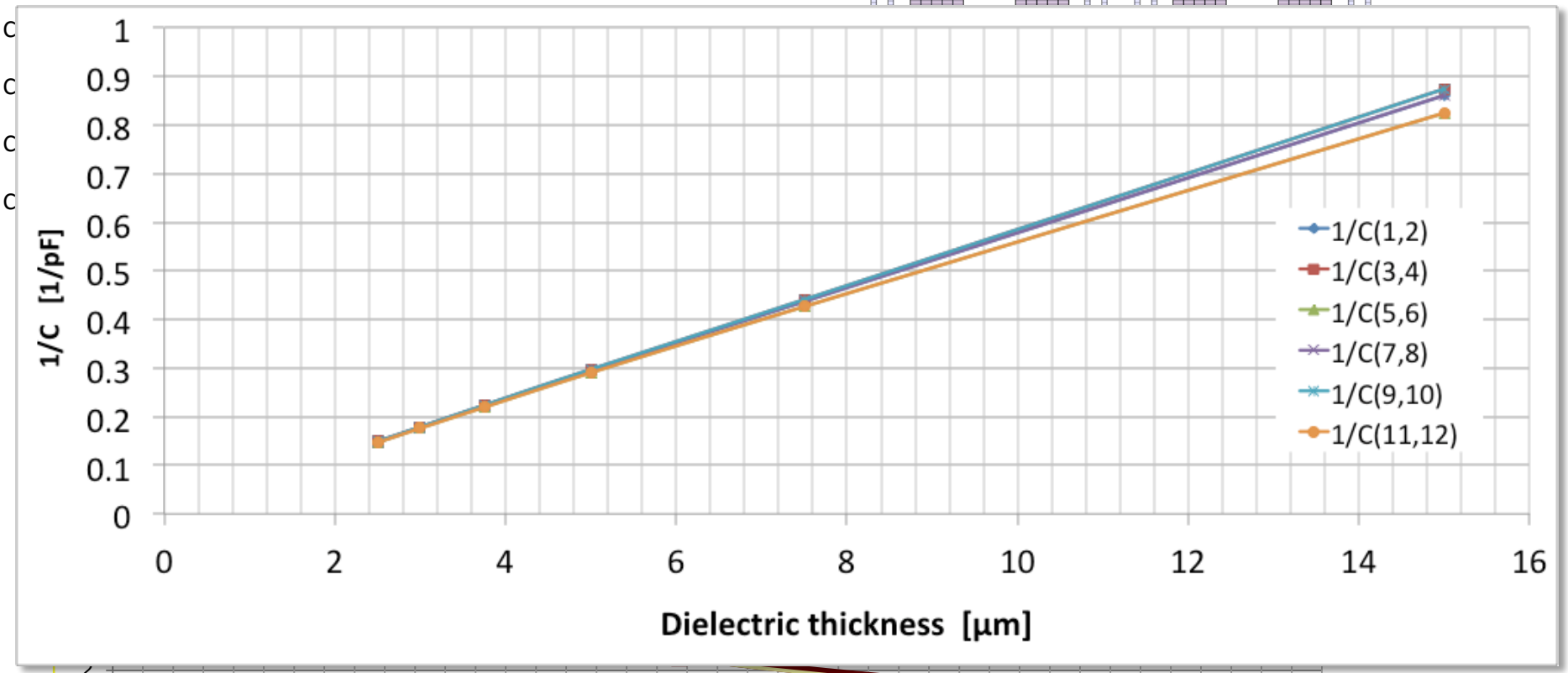
Dielectric thickness (µm) → Capacitance (pF)

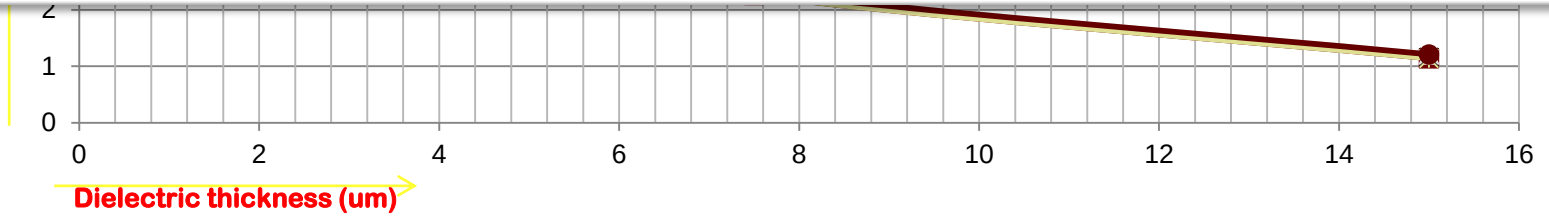
10 MHz

Credits: Ettore Ruscino – INFN / Genova

Dielectric	2.5um	3um	3.75um	5um	7.5um	15um
C(1,2)	6,7485	5,6125	4,4937	3,3829	2,2878	1,1613
C(3,4)	6,7267	5,5912	4,4731	3,363	2,268	1,1436







Dummy Wafers & Process Plan…

- *Dummy wafer layout completed*
  - 6-inch wafer will be produced by FBK – standard thickness, one metal layer on top of passivation (oxide)
- *SU8 process at Selex*
- *Flip chip at Genova or at other sites*
  - Modified the flip-chip machine for UV curing
- *After qualification, process a full FE-I4 wafer.*
- *We are also looking at full simulation of HV/HR-CMOS – FE chip coupling for optimal signal transfer*
  - Configuration data from R/O chip to HV/HR-CMOS can be transmitted capacitively… only power/ground need DC connection (laser soldering to flex hybrid as in ALICE proposal?)

***Timeline**: these initial test cover, approximately, the first year of AIDA-2020, we think to have partial answers before end of this year.*