AIDA2020 – WP6

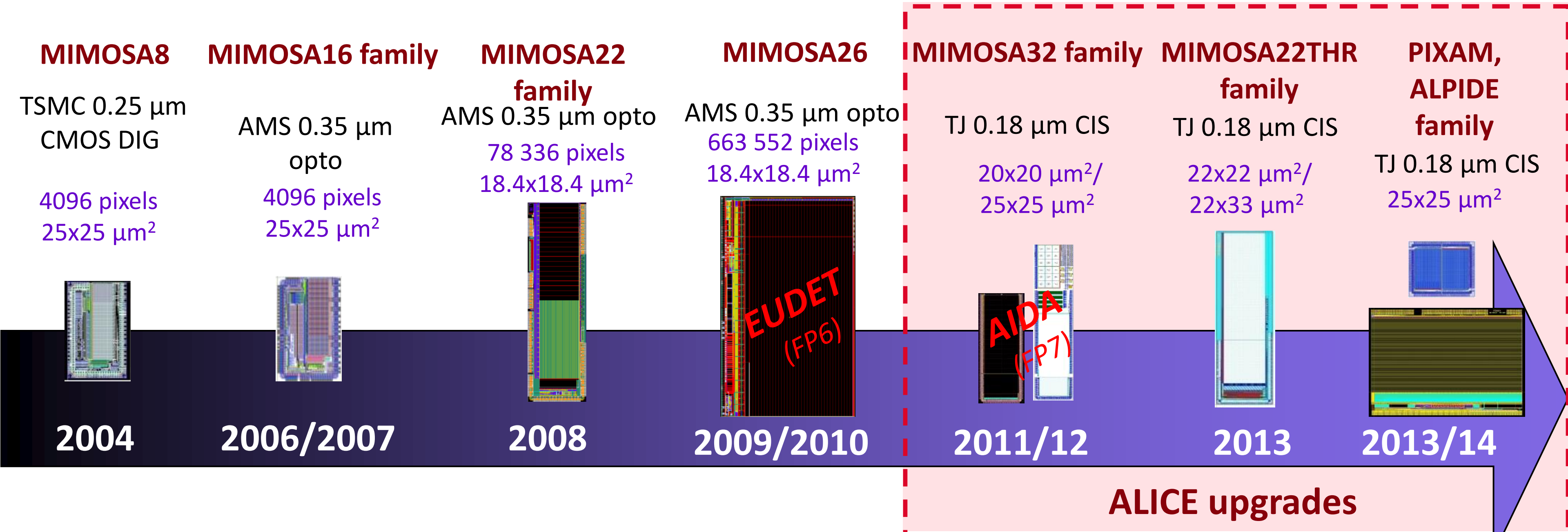
CEA (IRFU)

Y. Degerli, F. Guilloux, C. Guyot, F. Orsini, P. Schwemling

04 June 2015

HISTORIC – CMOS MONOLITHIC PIXELS SENSORS DEVELOPMENT AT CEA

- Since ~2004, CEA (IRFU) has launched a R&D program on CMOS MAPS technology starting in the framework of the ILC project (vertex detector)
- CEA (IRFU) has designed the first digital MAPS (MIMOSA 8) jointly with IPHC
- ~20 MAPS with digital outputs have been designed, realized and tested in the past 10 years (from small prototypes to large sensors) in collaboration with IPHC for ILC VX, EUDET (FP6), AIDA (FP7) and recently for ALICE-upgrade projects (MAPS design effort driven by CERN consortium)
- It has demonstrated the validity, maturity and the excellent performances of this detection technology for charged particles tracking



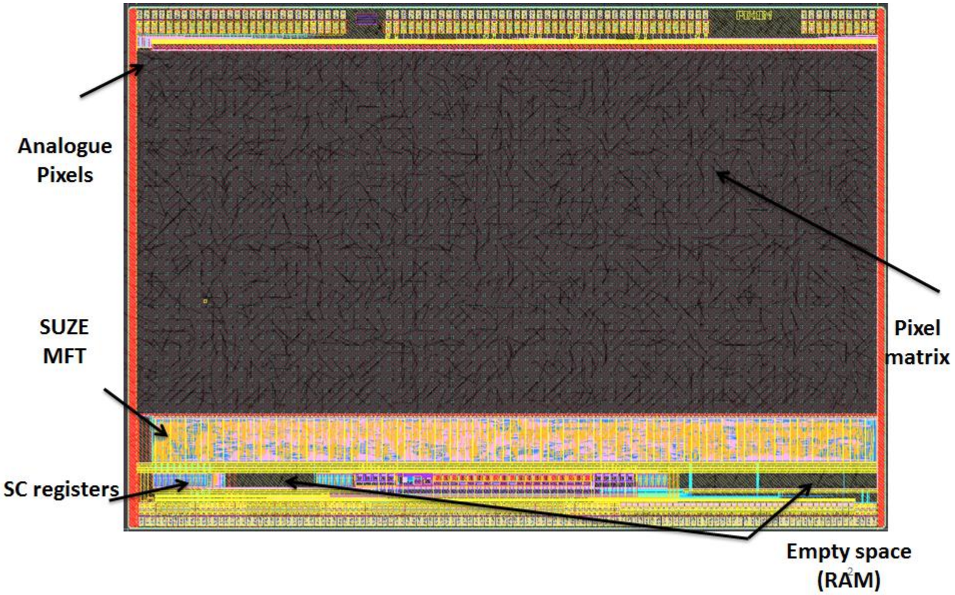
RECENT FULL MAPS CHIP DEVELOPED AT CEA

PIXAM (FSBB prototype)

developed specifically for the ALICE - Muon Forward Tracker project

CMOS monolithic pixel sensor using Tower Jazz 0.18 µm CIS technology

- **1/3 of final matrix (10 mm × 7 mm)**
- **Rolling Shutter Binary Pixel architecture**
  - **25 µm pitch**
  - **In each pixel: amplification, CDS, discriminator with continuous offset compensation**
- **2 lines readout simultaneously**
  - **Readout nominal : 15.36 µs**
  - Evaluation for readout : 10 µs
- **Zero suppression logic**
  - **Cluster 3x3 pixels**
  - 7 clusters / row/ FSBB
- **Digital Outputs**
  - Compatible with Pxi DAQ
- Removable peripheral test blocks



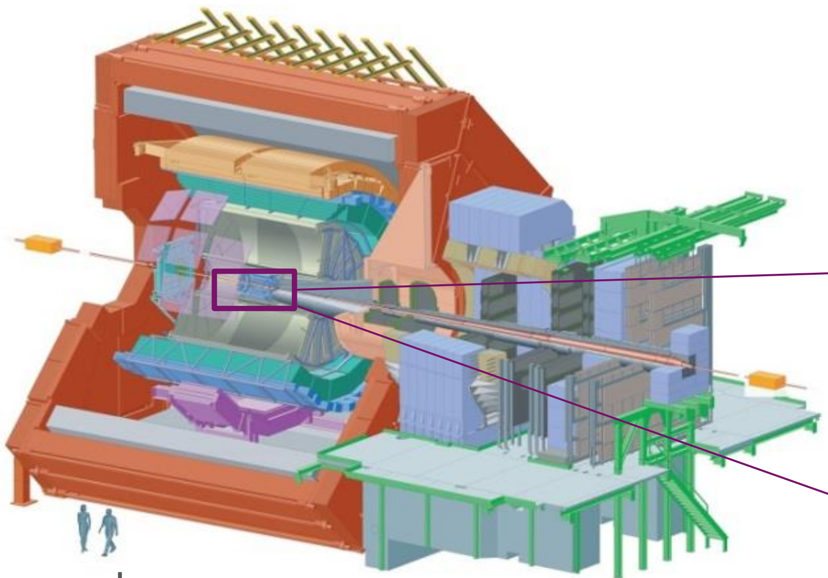
Submitted in May 2014

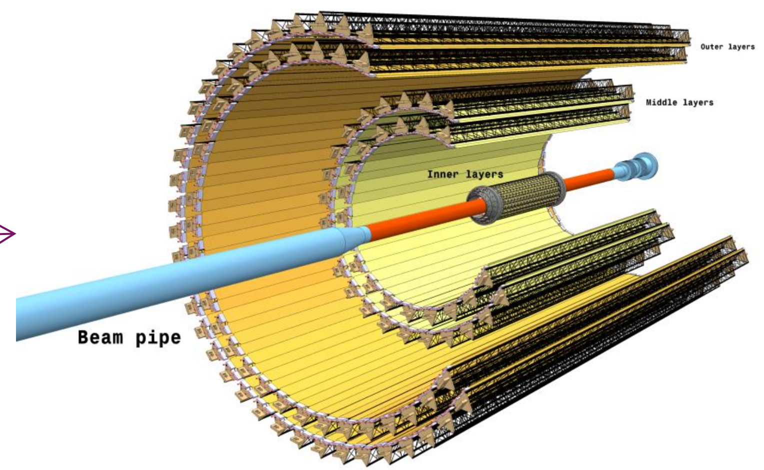
Power Dissipation (estimation)

- Analog: 105 mW/cm^2 (not optimized)
- Digital: 45 mW/cm^2

CMOS MONOLITHIC PIXELS SENSOR FOR ALICE UPGRADE: ITS & MUON FORWARD TRACKER

CMOS monolithic pixels sensor in common for ITS-inner barrel and the Muon Forward Tracker

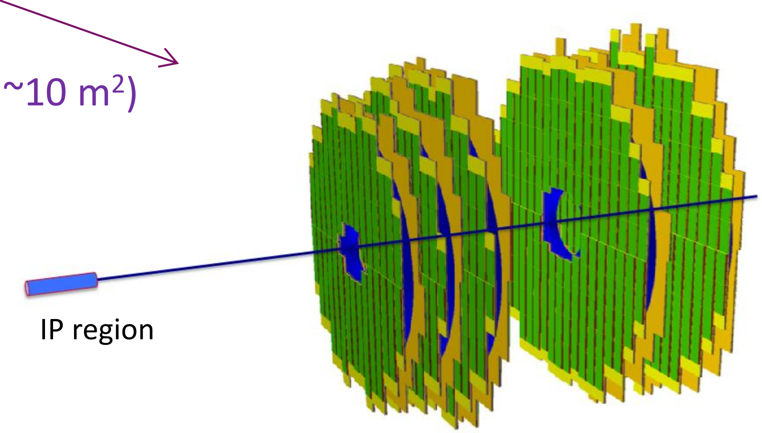




ITS

ITS upgrade:

- 7-layers barrel geometry based on MAPS (~25 000 sensors ~10 m^2)
- r coverage: 23–400 mm
- η coverage: |η|≤1.22



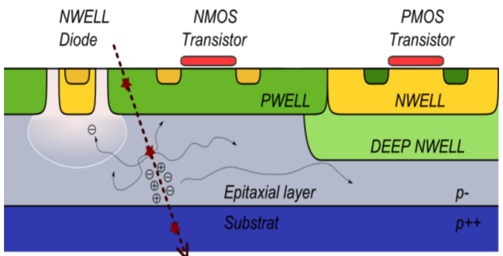
MFT

Muon Forward Tracker: vertexing for the ALICE Muon Spectrometer at forward rapidity

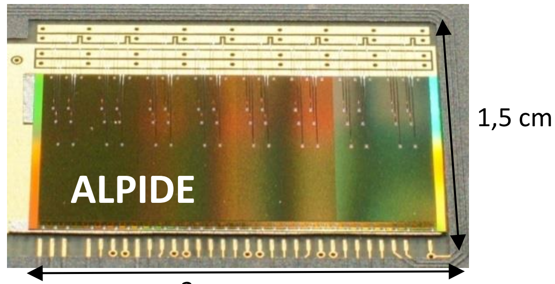
- 5-planes geometry based on MAPS (~900 sensors, ~0.5m^2)
- η coverage: -3.6 < η < -2.45

CMOS MONOLITHIC PIXELS SENSOR FOR ALICE UPGRADE: ITS & MUON FORWARD TRACKER

Monolithic pixel chip using Tower Jazz 0.18 µm CIS technology



Schematic cross-section of CMOS monolithic pixel sensor – no HV

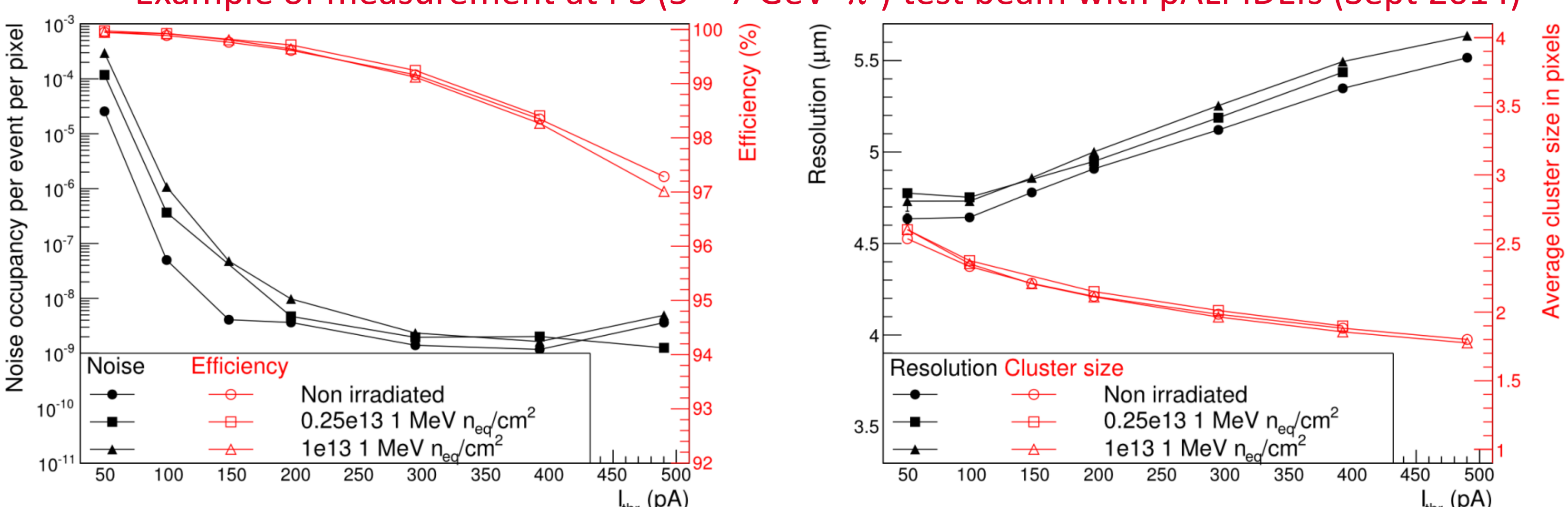


pAlpide-V1 (full scale chip) on carrier board

Parameter	Value
Spatial Resolution	~ 5 µm
Detection Efficiency	> 99.5%
Integration Time	< 20 µs
Sensor Thickness	50 µm
Power dissipation	< 150 mW/cm²
Radiation Tolerance (10-years operation)	~ O(10^{13}) n_{eq}/cm^2 ~ O(700) kRad

⇨High resistivity (> 1kΩ cm), p-type epitaxial layer (20 µm – 40 µm thick) on p-type substrate

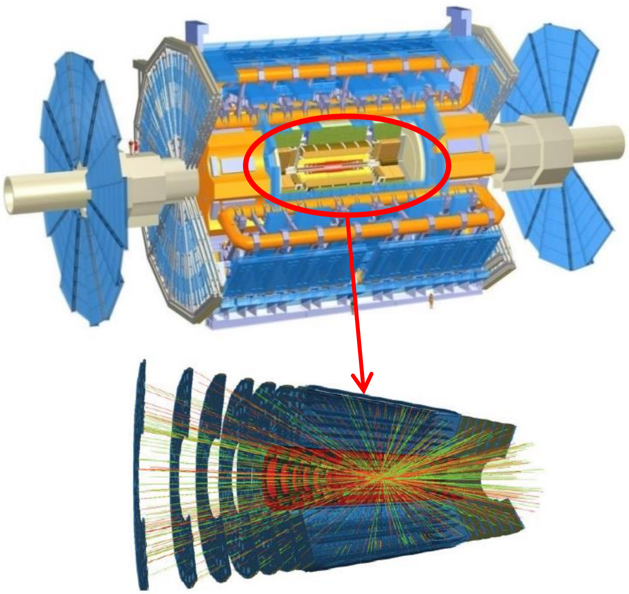
Example of measurement at PS (5 – 7 GeV π-) test beam with pALPIDEfs (Sept 2014)



with 50 µm thick chips: non irradiated and irradiated with neutrons (0.25 x 10^{13} and 10^{13} 1MeV n_{eq} / cm^2)

ATLAS PHASE II INNER TRACKER

- CEA (IRFU): large group of physicists already involved in ATLAS → new interest to participate in the R&D effort for Phase II Inner Tracker project thanks to the expertise of the micro-elect design team
- Expertise acquired on ALICE (complex full-MAPS chip, laser-soldering technic and readout system) → ease to quickly understand new issues and to propose/participate in sensors development



	ATLAS-LHC	ATLAS-HL-LHC
Bunch crossing [ns]	**25**	**25**
Particles rate [kHz/mm^2]	1000	10000
Neutrons flux [n_{eq}/cm^2]	**2x10^{15}**	**2x10^{16}**
Dose (ionizing part) [Mrad]	**80**	**>500**

- High resistivity wafer
- Application of high voltage → complete depletion possible

+

- Material budget improvement
- Thinner granularity
- Cost improvement

=

HV/HR CMOS Pixels

Challenges for phase II

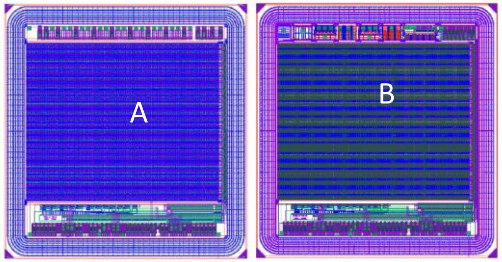
- Radiation hardness
- Readout time

CURRENT ACTIVITY/INTEREST: PIXELS HV/HR CMOS

1/2

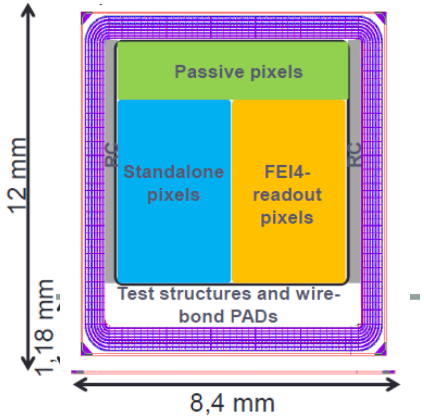
- Work on-going in collaboration with CPPM (S. Rozanov' team) and Bonn
  - First discussions with CPPM → summer 2014
  - Design work has started in January 2015 on HV technologies (Global Foundry 130 nm then LFoundry 150 nm) → *Weekly meetings with CPPM (P. Pangaud, S. Godiot, J. Liu) & Bonn (T. Hemperek, H. Krueger, L. Gonella, P. Rymaszewski, T. Hirono)*

- 2015 : 2 steps
  - Participation to the micro-electronic design of the LF_CPIX demonstrator with CPPM & UBONN → submission foreseen in Q3 2015
  - Plan to participate to the CCPD_LF prototype tests in-lab and in-beam



Prototype CCPD_LF

- 2016 :
  - LF_CPIX demonstrator validation
  - Choice of the pixel technology → end of 2016

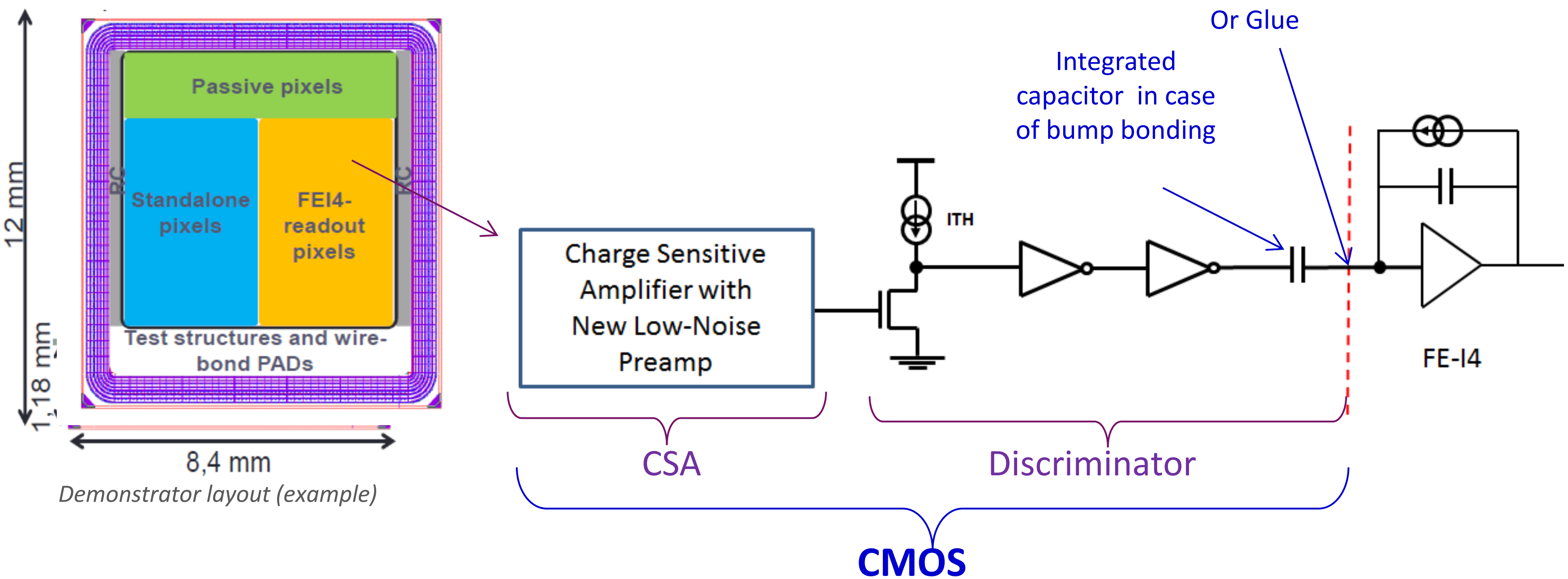


Demonstrator layout (example)

CURRENT ACTIVITY/INTEREST: PIXELS HV/HR CMOS

2/2

- CEA contributions to the LF_CPIX demonstrator (LFoundry 150 nm)
  - Focus on active pixels to be readout with the FE-I4 chip;
  - A new preamp has been proposed for the demonstrator;
  - The new preamp seems to be interesting in terms of noise, power dissipation and speed
  - The design of a full active pixel with saturated output (simple discriminator) is on-going
  - Power supply rejection and radiation hardness improvements of the pixels are on-going



Demonstrator layout (example)

INTEREST & COMMITMENT FOR AIDA2020-WP6

- **Task 6.3 Sensor development** (CEA, CNRS-CPPM, KIT, UBONN, STFC-RAL, UNIGLA, UNILIV)
  - *Design and production of test structures and sensors*
  - *Characterization of test structures and sensors*
  - *Radiation-hardness evaluation*

- **CEA (IRFU) resources contribution**:
  - Human resources: 11 h.month → profile: micro-elect designers & physicists
  - EC request funding = 52 k€ ; + 12k cash contribution from CEA (IRFU)

- **Main milestones where CEA is concerned:**
  - MS6.3 → MPWR submission → M12 → Purchase order submitted
  - MS6.5 → First irradiation campaign with sensor prototype assemblies → M16 → Irradiation performed

- From Sept 2015: possibility to get a PhD student on CEA fund (application in progress)
- From Jan 2016: possibility to reinforce the micro-elect design team with digital designer