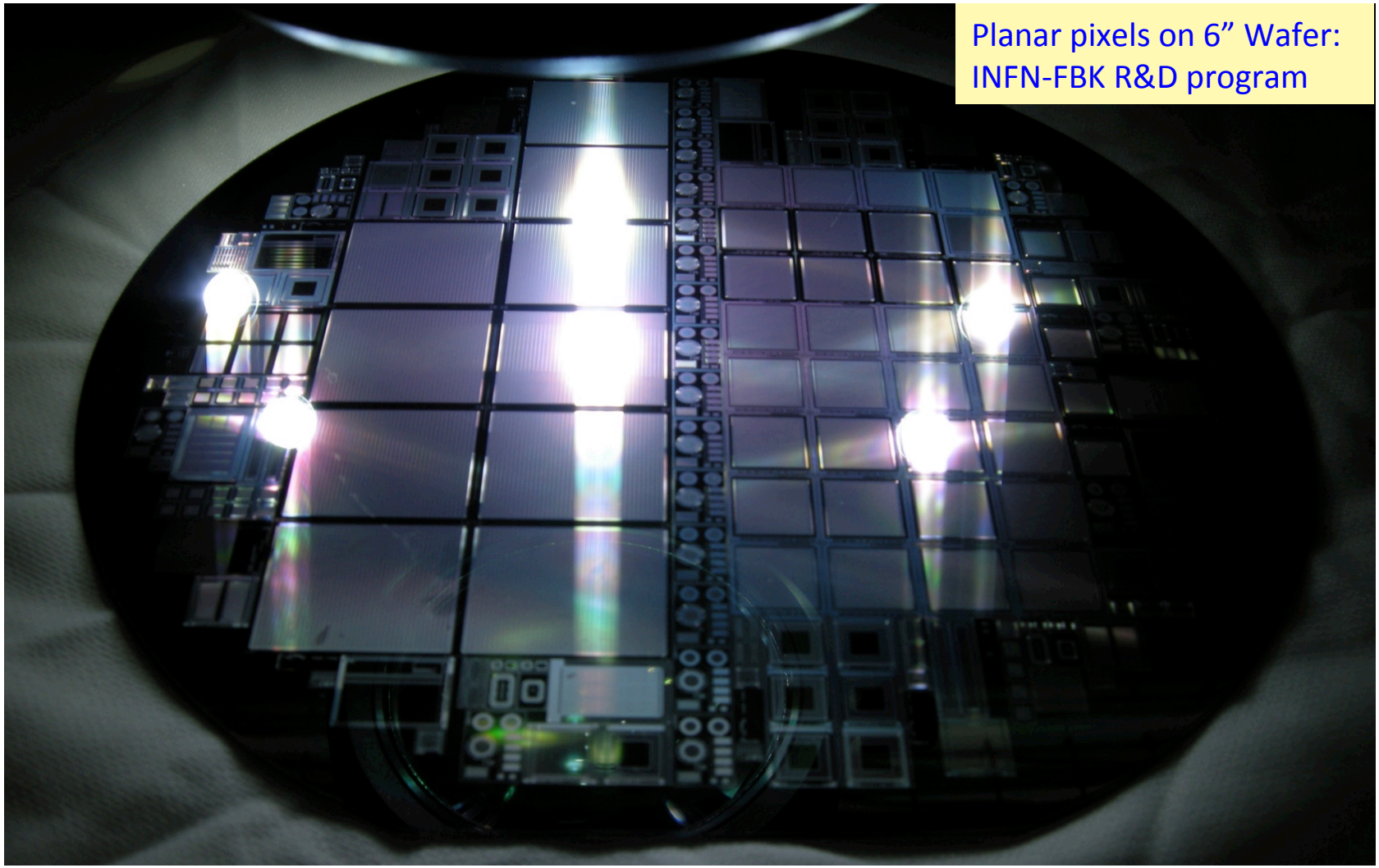
Plans and Activities for the AIDA-2020 Starting Phase in Firenze



Planar pixels on 6” Wafer:
INFN-FBK R&D program

Marco Meschini
INFN Firenze

Pixel R&D in Florence and AIDA-2020

- Florence is participating in AIDA-2020 WP7 Task 7.4 “Detector validation for tracking devices” for both 3D and Planar Pixels
- Since 2014 Florence is also part of a four year R&D program on 3D and Planar Pixel Sensors for HL-LHC under INFN – FBK special agreement. This R&D, funded by INFN, is a common project originating from CMS and ATLAS researchers in Italy, involving different Italian groups
- Scientific objectives: new small thickness pixel sensors, to be used in particular in the inner layers of future trackers in high radiation environment. As a final goal the pixels must have small pitch size, possibly developed in agreement with the new readout chip in 65nm technology under development in the RD53 collaboration
- Bump bonding to present and future readout chips, characterizations, irradiations, and beam test of detectors are essential steps of our program
- High density bump-bonding, spark isolation techniques, different active and handle wafers are also features to be studied and tested
- The INFN-R&D and AIDA-2020 have many common aspects, hence synergies are quite straightforward
- Given the overlaps between AIDA-2020 and INFN-R&D we plan to take profit of the resources allocated by INFN for the R&D to help fulfilling our milestones in AIDA
- **We are planning to ask for AIDA support and collaboration on sensor design, production, irradiations, test beams**

Activity Plan Task 7.4

- Workplan on 3D and Planar Pixels
  - Interaction with foundries on materials, technologies, design options, process optimization and yield
  - Full characterization
  - Hybridization with present and RD53 prototype readout chips
  - Irradiation to fluences up to 1 or 2 10E16 neq/cm2
  - Radioactive source and Test Beam measurements, in particular after irradiation, to check charge collection, spatial resolution, detector efficiency
- Deliverables
  - Contribute to the characterization of first 3D and planar pixel sensor hybridized
  - Give Feed-Back to the foundries
  - Demonstrate tracking capabilities of irradiated sensors suitable for use in HL-LHC
- Milestones
  - Participation in MPW runs
  - Test Beam with irradiated sensors

Associated Partners and Collaborators in WP7

- Italian INFN and University Partners (not AIDA beneficiary, funded by INFN)
  - Not mentioned in AIDA2020
    - Pisa: sensor design, layout, characterization, Bump Bonding quality control, relations with industries
    - Milano Bicocca: irradiations, DAQ, Test Beam
  - Mentioned in AIDA2020 WP7 or WP6 or WP13
    - Bari: characterization, hybridized sensor test
    - Milano: Bump Bonding quality control, relations with industries
    - Genova: 3D sensor design, hybridized sensor test
- Other collaborators:
  - LPNHE Paris: planar and Active Edge pixel design, FE-I4 DAQ (LPNHE funds)
  - Max Planck Institute: planar design, lab DAQ, FE-I4 expertise, introduction and tutorial for FE-I4 use

An important remark: we should try to find a solution on how to acknowledge the contributions and work done by INFN collaborators which are not beneficiaries

R&D Pixel Sensor Batches with FBK

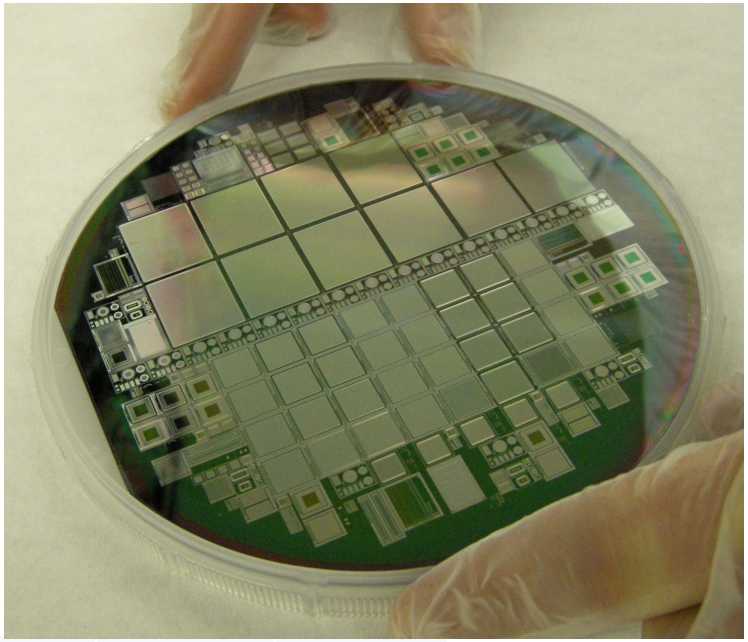
- All batches will be on 6” n-in-p Wafers
- Different wafer types:
  - Direct Wafer Bond (DWB) 100um and 130um active FZ, 500um handle CZ
  - Silicon On Insulator (SOI) 100um and 130um active FZ, 500um handle CZ

First Planar batch on DWB wafers already completed!

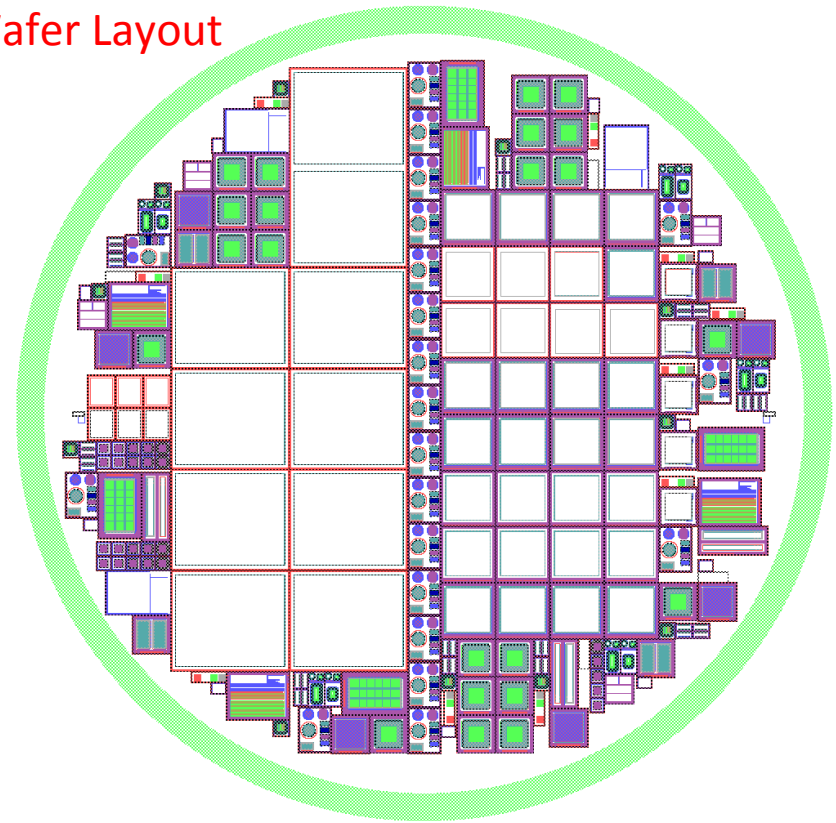
- Wafers containing ATLAS (FE-I4) and CMS (PSIdig) sensors with different options (PT, p-stop, p-spray), one FE-I4 Doublet and a few 55*55, 50*50 and 30*100µm2 pitch mini-sensors, plus test structures
  - finished December 2014, wafers tested at FBK, Firenze, Pisa;
  - now shipped for BB to IZM (Germany) and Selex (Italy)
  - Flip-chips ordered
- First 3D single-side batch on DWB wafers on the starting line
  - ATLAS and CMS standard sensors
  - Small pitch pixels

First Planar FBK Batch

Pixel standard Sensors:
32 PSI
4 FE-I4 standard
4 FE-I4 new PT
1 FE-I4 doublet



Wafer Layout



wafer #	material	thickness
30	Si-Si	100
33	Si-Si	100
49	Si-Si	100
63	Si-Si	130
69	Si-Si	130
74	Si-Si	130
75	Si-Si	130
80	Si-Si	130
81	Si-Si	130
1	FZ	275

Wafers Tested at FBK Florence and Pisa

Three P-spray doses

Sensor Wafer Processing at IZM

Present status (June 2015)

- Planar Sensors:
  - 5 wafers will be processed having following active thickness
    - 2x 100 µm, 3x 130 µm
    - Thinning of support wafer:
      - 1x 100 µm active thickness --> to 200 µm total thickness
      - 1x 130 µm active thickness --> to minimal thickness ~150-180 µm
      - 1x 100 µm, 2x 130 µm active thickness --> to 285 µm total thickness
  - Backside metal deposition (Al sputtered) and patterning
  - BCB spark protection layer on sensor (Benzo-Cyclo-Butene)
    - Design and 7" mask preparation: mask to be designed by IZM upon agreement with INFN
  - Dicing, all pixel sensors singularized

ROC Wafer Processing at IZM

- One PSI 46 DIG ROC 8” wafer will be processed
  - SnAg bumping of readout chip wafer
  - Thinning to 175um, same as CMS Pixel-Phase-I (TBC)
  - Dicing in single (244) ROC chips (~ 1x1 cm2)
  - BCB spark protection layer
    - Design and mask preparation at IZM
    - BCB deposition and patterning: mask to be designed by IZM upon agreement with INFN
- FE-I4 wafer: still under discussion, we are in the “Global ATLAS order” to have one wafer thinned to 450µm and deposited
  - we have bought three FE-I4 wafers in total, still waiting to be tested
  - a few bumped FE-I4 chips available from ATLAS collaborators (LPNHE Paris, MPI Munich, INFN Genova)

WP7 and RD53 Prototype ROC: Be Prepared!

- We are in contact with RD53 people to include the floor-plan of the RD53 read-out chip prototype(s)
- It looks possible that there will be a small pre-prototype beginning 2016 and a bigger prototype late 2016 (early 2017?): we do not know neither if they they can be bump bonded nor the cost
- Overall dimensions not yet defined
- I do not want to write dates, sizes or numbers here, but we must be ready when the first prototypes will be available

- The INFN-R&D choice: stay on the safe side and Be Prepared(*).
- Options to design two pixel arrays, large and small, in the 3D batch which could be potentially bonded on RD53 prototype(s). This chip should be same size or bigger than the pixel sensor (smaller is extremely difficult if not impossible to be bump bonded)

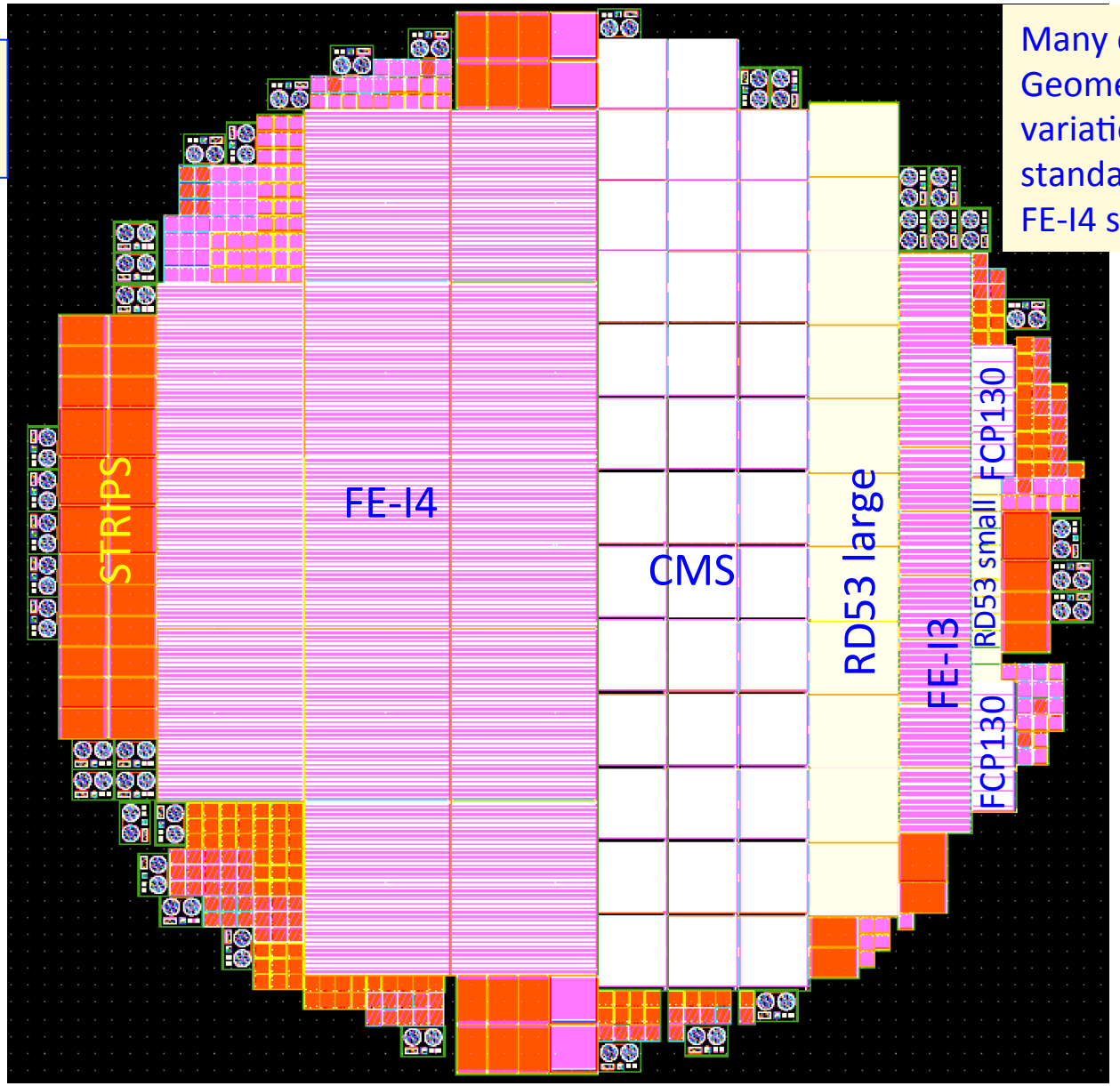
(*) Robert Baden-Powell, 1937

3D Pixel Layout on 6”, FBK Single Side Process

Almost final version, under revision June 2015

Many different Geometries and pitch variations, including standard PSIdig and FE-I4 sensors

Multiplicities
13 FEI4
38 CMS
9 FEI3
6 FCP
11 RD53 large
12 RD53 small
+ diode, strips, test structures



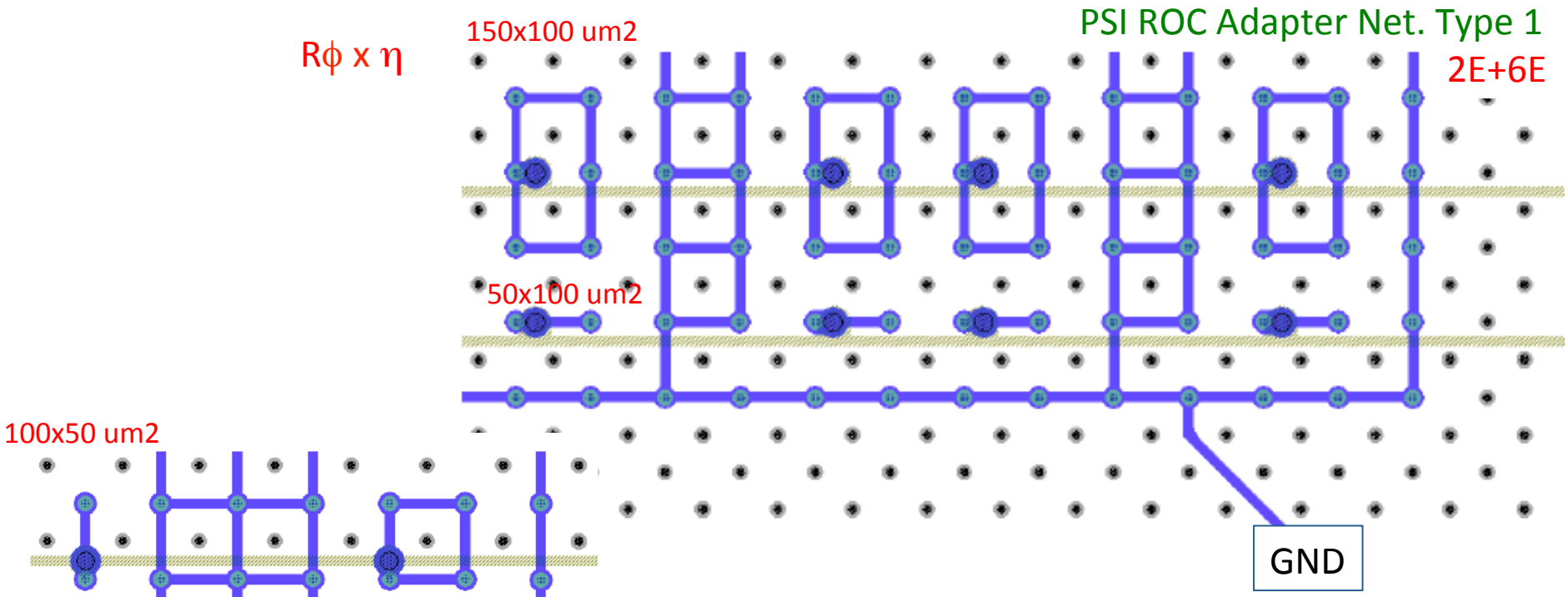
G.F. Dalla Betta et al

List of Pixel Variants

- FE-I4/I3
  - 50 x 50 1E
  - 25 x 100 1E and 2E
  - 25 x 500 1E
- PSI46dig
  - 50 x 50 1E + 2E
  - 50 x 100, 100 x 100: 2E + 4E
  - 100 x 50, 100 X 150: 2E + 6E
  - 25 x 100: 1E + 2E
- FPC
  - 30 x 100 1E
- RD53 “Large/Small Prototype”
  - 50 x 50 1E
  - 25 x 100 1E + 2E
- Standard FE-I4
  - 50 x 250 2E
- Standard PSI46dig
  - 100 x 150 2E and 3E

CMS PSI46dig layouts with additional metal grids to readout small pitch pixels

Rϕ x η



Similar approach with FE-I4 grids to read pixels down to 25 x 100 μm^2

PSI ROC Adapter Net. Type 2

2E+4E

G.F. Dalla Betta UNITN
M. Meschini INFN-FI

New Layout for Planar Active Edge Pixel Sensors

-Studies are underway, design not yet defined;

- 10 wafer batch, 5 DWB + 5 SOI

-Add sensors from common CMS R&D design

-Options to add some FE-I4 for serial power R&D

Production on INFN funds, second half 2015

A.E. on 6" DWB and SOI wafers

100 & 130 µm active thickness

We are missing designers!

-Sharing of wafer area with ATLAS to be agreed, there is interest from

G. Calderini(LPNHE Paris) for FE-I4: 2 doublets + 2 singlets

LPNHE could contribute on wafers, design and BB

-Optimize area usage

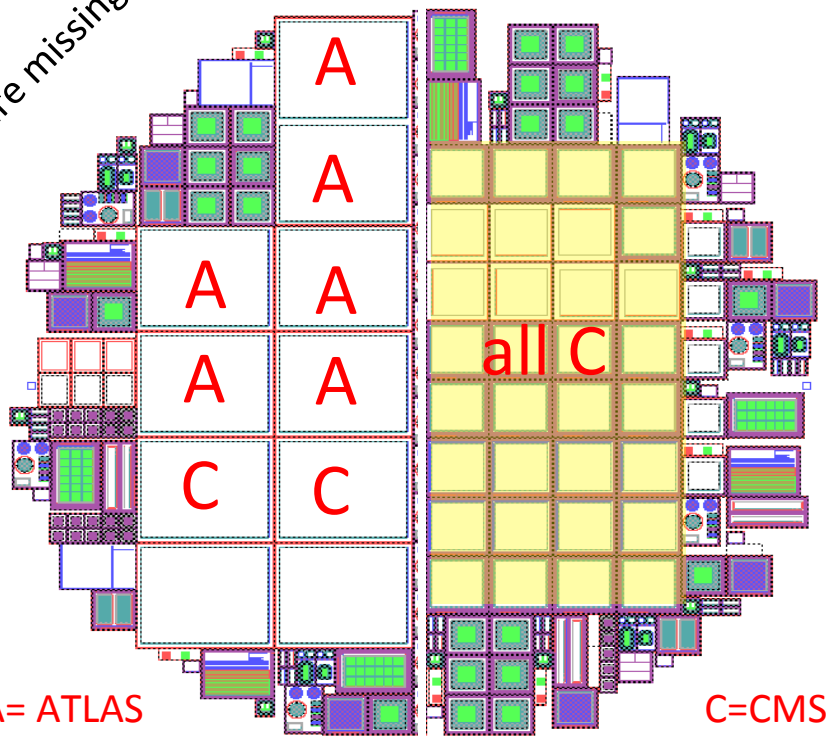
-New Sensors?

-Reduce zoology?

-Reduce TS?

-Inherit from 3D layout studies

Again (as in 3D) use Metal Grids to adapt present ROCs pitch to 50µm and 25µm pixel pitch



A possible draft from present planar layout

Pixel Batches with FBK: Future

- Two new batches with small pitch size are foreseen (second iteration of 3D and Planar AE)
- Funds for production will be requested for 2016-17, again under INFN-FBK agreement
  - these new batches will profit of the results obtained in the previous ones and will include, if available, the bump-pad layout for the RD53 demonstrator chip

- Dummy sensors with high density BB pads, large sensor size (2*3 cm2 ? Multi Sensors?) for Bump Bonding tests. Detailed program still to be discussed within INFN R&D collaboration
- All of these future activities could be open to WP7 inputs and possible needs

Irradiations

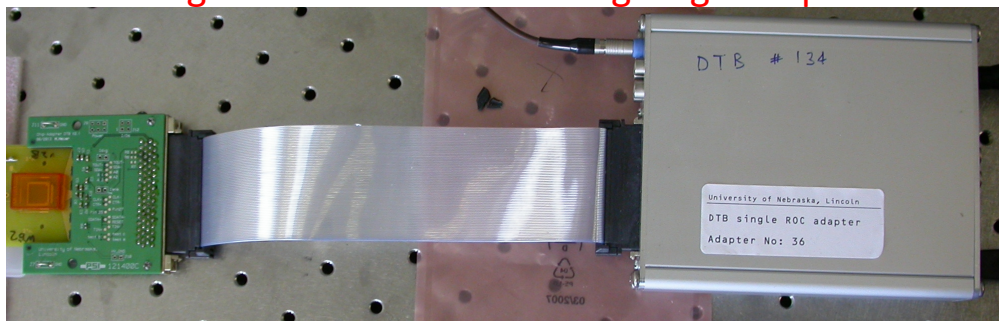
- In the INFN R&D program we have foreseen a few steps of irradiations
  - we will start with moderate fluences (~10E15 neq/cm2) to verify hybridized sensor behaviour after initial irradiation, then gradually increase toward 10E16 neq/cm2
  - we will probably hit the ultimate fluence limit for PSIdig
  - we need to find alternatives to reach 1-2*10E16 neq/cm2 on hybridized sensors
    - Is flip-chipping of irradiated sensors onto non-irradiated ROCs a viable solution?
    - Will the RD53 prototypes be radiation hard up to …?

- **We plan to profit of the Irradiation and Test Beam AIDA-2020 Transnational Access WPs**

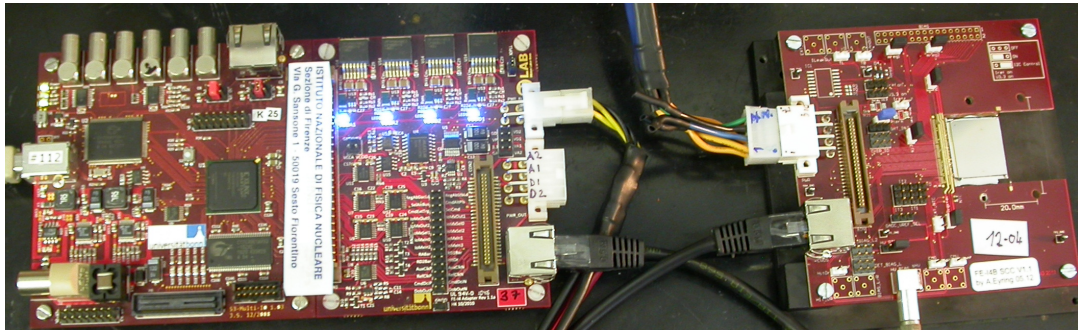
Characterization and Test in Florence

- It is part of our AIDA-2020 task
- Pixel sensors have to be characterized before and after irradiation to be qualified for HL-LHC environment
  - Optical inspection of wafers under stereo microscope (axial and/or grazing light source)
  - Cooled Probe station for I-V, C-V measurements
- Test of hybridized sensors
  - PSIdig readout board
  - FE-I4 system presently based on USBpix card (on loan, G. Calderini, LPNHE Paris) and FE-I4 SCC pixel (Thanks to A. Macchiolo, MPG Munich)
  - BIC card to read out 4x FE-I4 procured

Digital Test Board for PSIdig single chip readout



USBpix for FE-I4 readout



Powering Options R&D in Florence

- The inner pixel layers at HL-LHC will likely have to be powered serially
- The future RD53 ROC will include the Serial Power Option (also in prototype chips)
- The FE-I4 ROC has already a built in Shunt-LDO regulator: nice playground
- We are in the line to get the new FE-I4 readout system ATLAS is producing
- We will be working in contact with ATLAS Bonn group (L. Gonella, F. Hueggins)
- Standard FE-I4 sensors from FBK batches will be used in the first period, then we will move to the RD53 prototypes with new sensors
  - Beta source in lab and then test beams
  - This R&D will possibly contribute to the final characterization of 3D and planar irradiated sensors with final readout chip prototype in a realistic powering situation: AIDA-2020 WP7 milestone

Conclusions

- There are many overlaps and synergies to be exploited in the framework of AIDA-2020 and INFN R&D
- We are facing big issues: we must be open to collaborate and discuss on how to overcome difficulties and reach in the most effective way milestones and deliverables for AIDA-2020
- We plan to use AIDA funds in Florence to partially cover the costs to hire a PhD/Post-Doc for 24 months to work on the AIDA-2020 project, beginning of 2016. We are looking for qualified candidates to work on this cutting edge R&D
- A lot of work is in front of us: joining efforts is the recipe for the “Happy End”

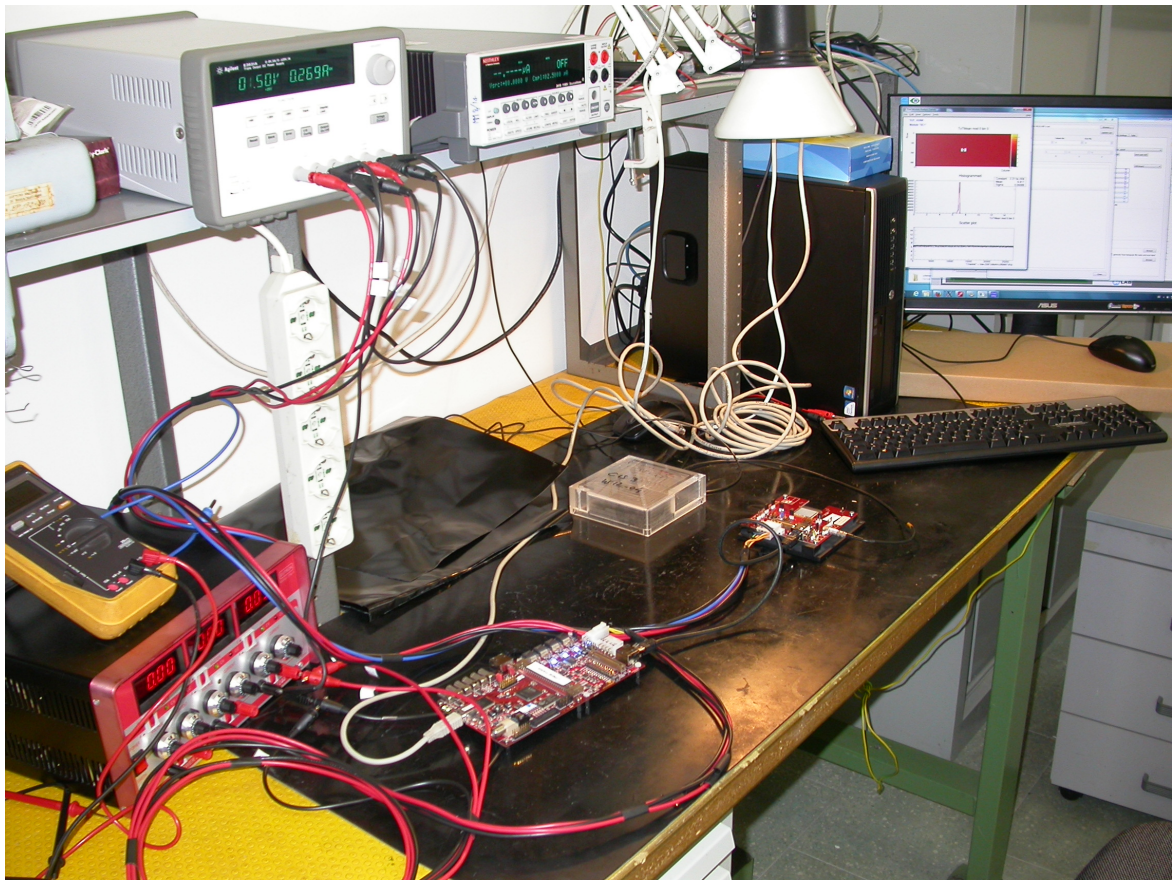
BACK UP

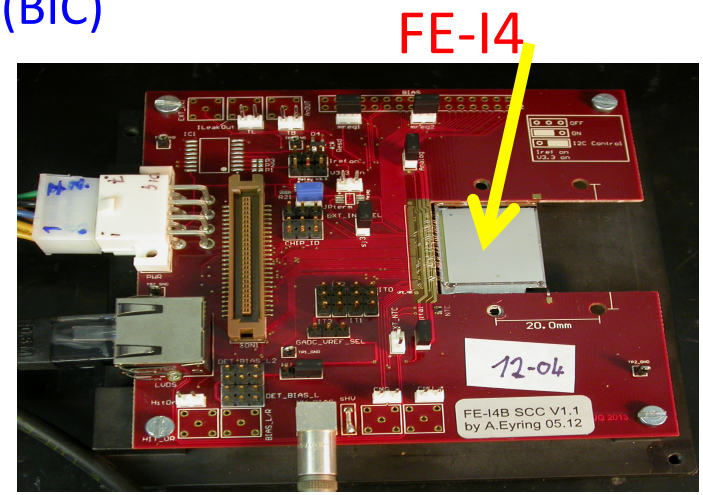
Readout Chips and Bump Bonding

- For R&D Bump Bonding usage we have bought both FE-I4 and PSIdig ROC wafers (with CMS-Italy funds)
  - Our FE-I4 will go to IZM only (ATLAS side has already FE-I4 at both Selex and IZM)
  - PSIdig is at IZM and a new one will probably go to Selex for BB test with a different firm
- Other ROCs we would like to use, provided BB feasible (cost?)
  - ROC4sens is a 50*50um2 pitch ROC for R&D purpose, under design but not yet available
  - FCP130 is a 30*100um2 pitch ROC designed at FNAL, first iteration under test, 2nd submission planned for summer 2015
- Pixel arrays suitable to be Bump-bonded to 50*50um2 ROC4sens were already included in the first planar batch layout
- We are planning to bump-bond a large number of pixel sensors from each batch and then proceed to irradiation campaigns and test beams
  - number of flip chips are still to be defined and depend heavily on available funds and BB costs

FE-I4 Serial Power R&D Setup in Florence

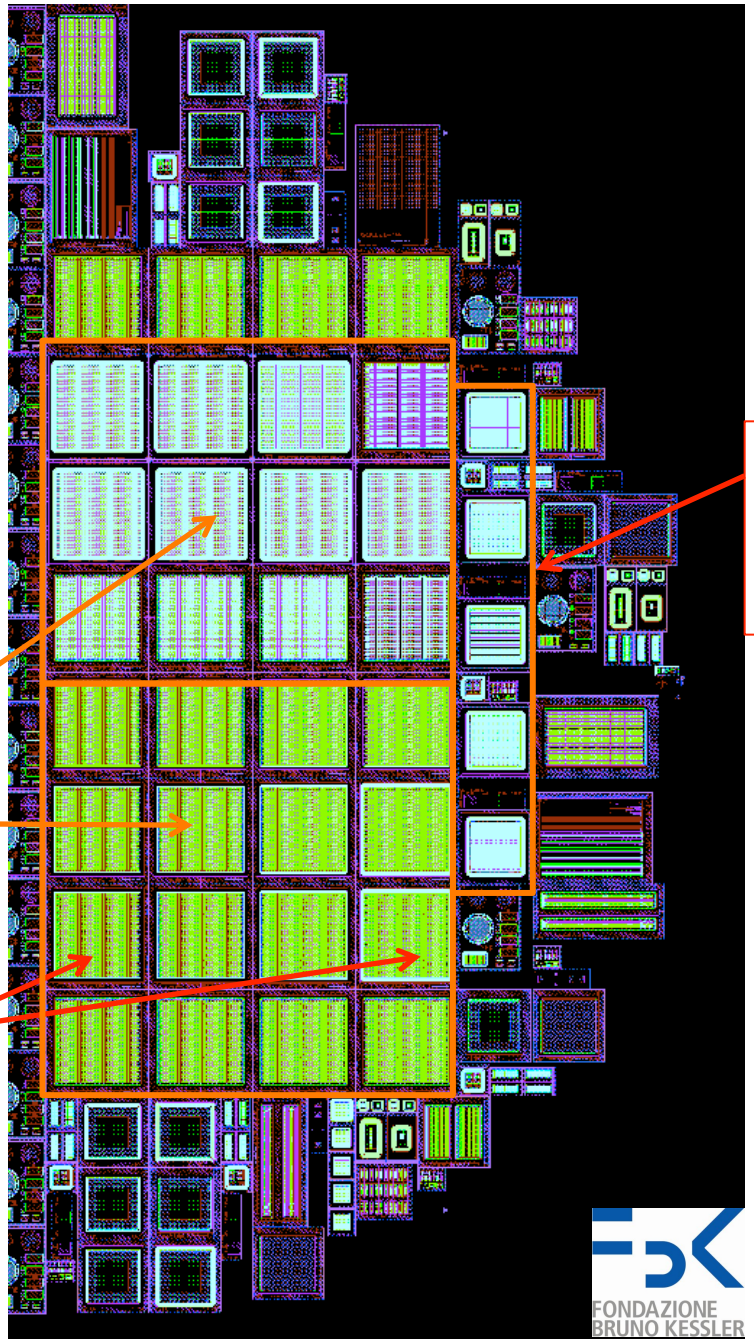
- Single FE-I4 readout system
- A new Four-chip readout card has been procured (BIC)



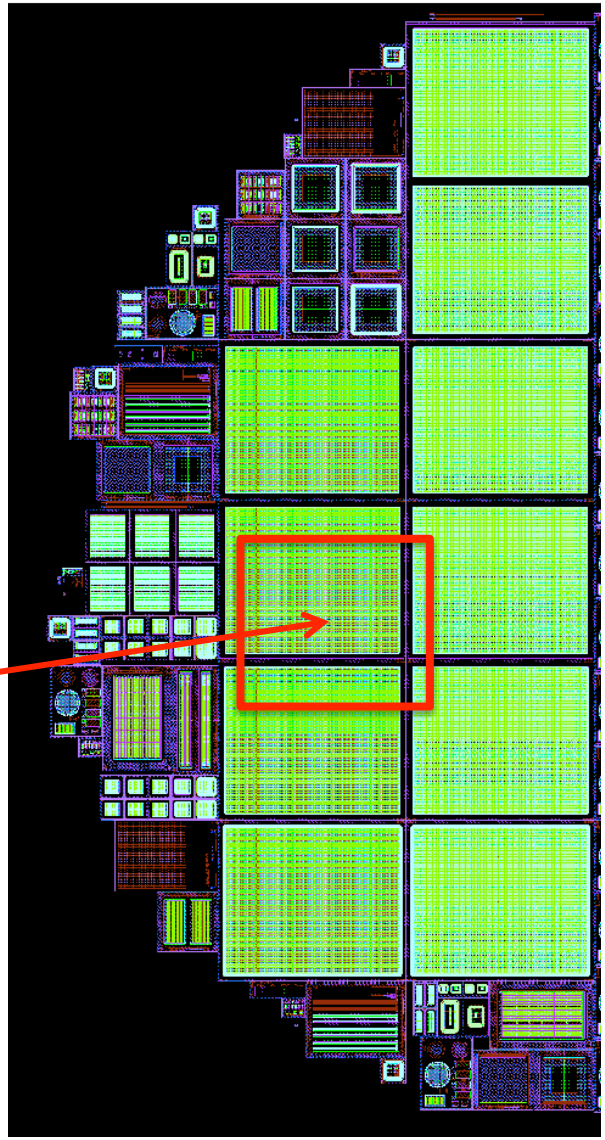


The CMS Side of the Moon

Active Device Float Zone Si-Si DWB
from Icemos
P type
CZ Handle wafer, 0.1-1 Ohm cm
resistivity, 500μm thick
FZ Sensor wafer resistivity > 3kOhm cm
2 thicknesses: 100μm and 130 μm,
used for planar, 3D, AE batches, DRIE
Column investigations



Each sensor is replicated from
1 to 5 times in each wafer

ATLAS half moon

ATLAS sensors (FE-I4)