# Task 14.4

## Readout systems for innovative calorimeters

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AIDA-2020 Kick-off meeting
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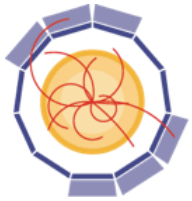


AIDA 2020

HELMHOLTZ ASSOCIATION

LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

DESY

# Overview of Task 14.4

**Definition of Task 14.4: Readout systems for innovative calorimeters**

1. Interfaces for calorimeter prototypes to the central DAQ system for linear colliders
2. Highly integrated readout elements addressing challenges of real-size highly granular calorimeters
3. Development of test stations for determining the performance of front end electronics
4. Test stand for readout ASICs as a prototype for mass testing of ASICs for next generation calorimeters

**Participating Institutes:**

- IPASCR
- IPNL, LLR, LAL
- DESY, U Wuppertal

**Subdivision:**

1. LC Calorimetry specific DAQ interfaces (IPASCR, DESY, IPNL, LLR)
2. Low power Readout & Monitoring Systems (DESY, U Wuppertal, IPNL, LAL)

# Milestones and Deliverables

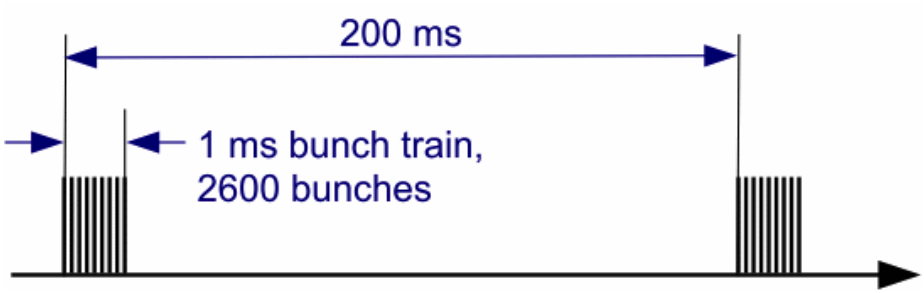
- Milestone 58: [month 24]
  Definition of optical and electrical coupling of readout, interface functionality and **DIF design**. Technical documentation and a viable schedule for hardware production and testing
  Verification: DIF data sheets

- Deliverable 14.5: [month 36]
  **Common running of calorimeter prototypes**
  Data acquisition system to allow for a common data taking of different highly granular calorimeter prototypes in beam tests at CERN and DESY. These tests should provide data files containing events synchronised between the subsystems

- Deliverable 14.6 [month 44]
  Adaptation of **readout system for operation in compact LC detectors** implying optimisation of space and power consumption. **Demonstration of concept** with existing calorimeter prototypes and **proposal of extrapolation to full size** detector.

# Requirements for Linear Collider calorimeter DAQ

- time structure of ILC beam:
  1ms beam, 199 ms gap
- no active cooling within main detector volume




➔ **low power consumption**

- very low for components inside the active layers
- low for detector interfaces

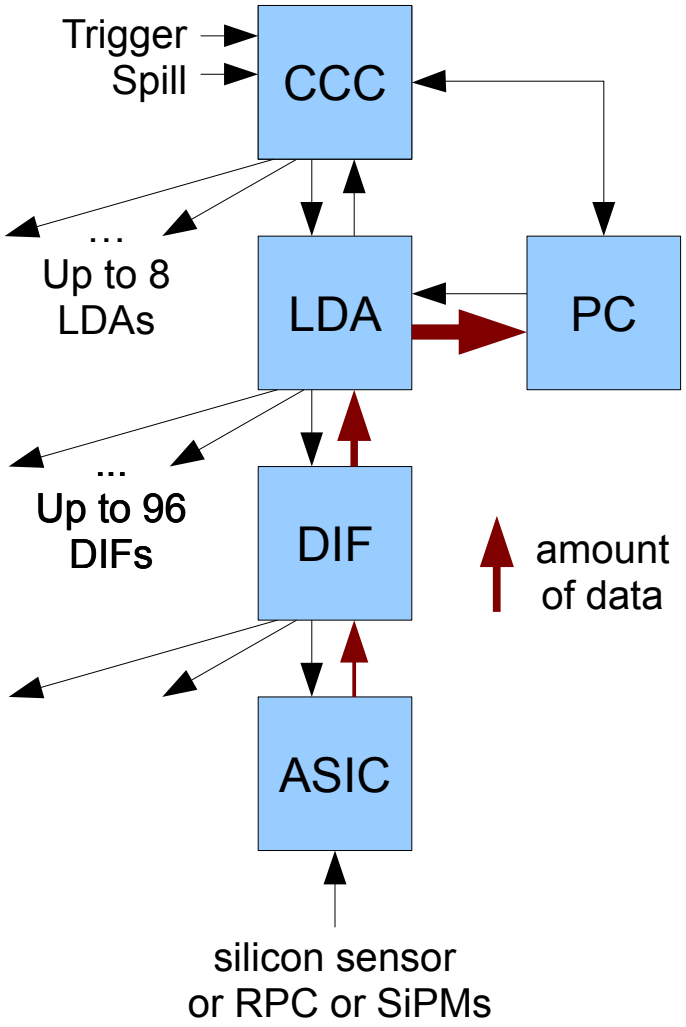
- **power pulsing**

- low data rate (compared to LHC detectors)

- **at the same time: efficient running in beam tests**

# LC calorimeter DAQ Hierarchy

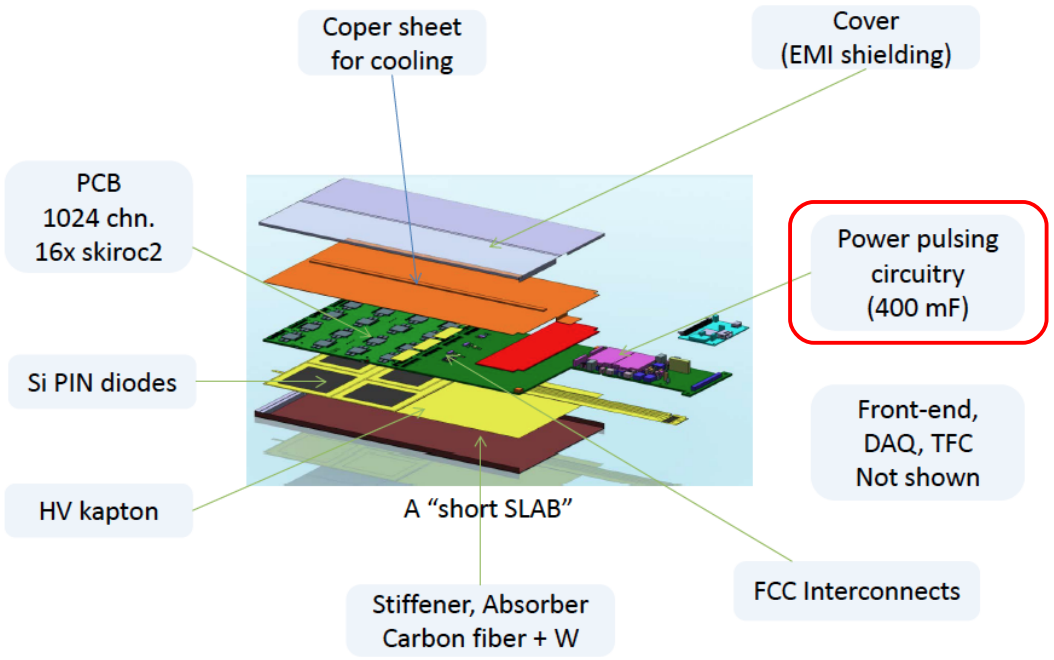
- Clock and Control Card (**CCC**)
  - Provides master clock
  - Starts and stops the acquisition
- Link Data Aggregator (**LDA**)
  - Packet collecting & processing (decoding, merging)
  - Send the packets to DAQ PC
- Detector InterFace (**DIF**)
  - Controls the ASICs (voltages, acq. state)
  - Controls power pulsing
  - **Collects data from all ASICs in one layer**
  - Sends the data to LDA (or PC for SDHCAL)
  - **Detector specific aspects**
- very front end ASIC (...ROC family, Omega)
  - SKIROC, HARDROC, SPIROC



# Infrastructure for ECAL

## DAQ for silicon readout

building the infrastructure for a very compact digital readout system: miniaturisation of the readout electronics



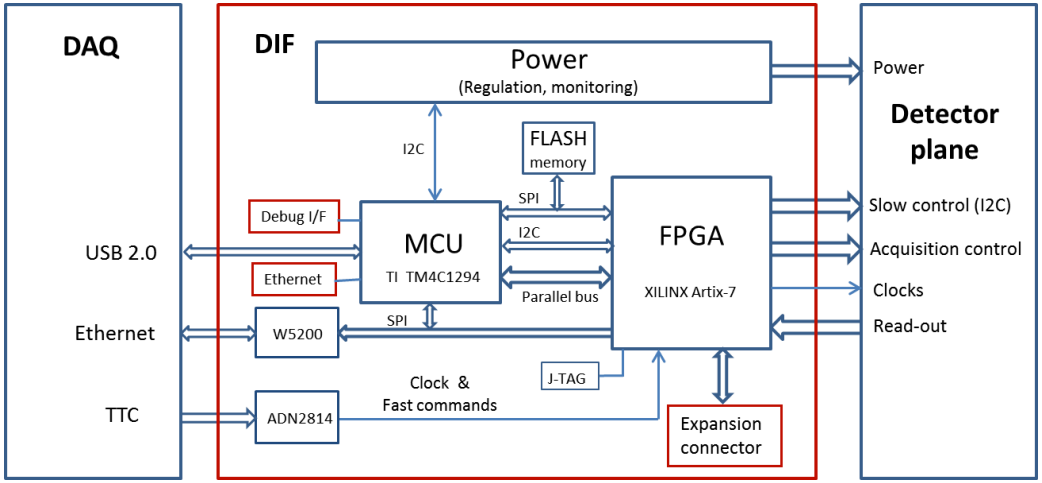

## Detector Interface card (DIF)

## Institutes: LLR, LAL

- current design works and is used in testbeams
- current design not ok for a final system
- need to work on power distribution (long slab)

# Infrastructure for Semi-Digital HCAL

## DAQ for RPC readout




## Detector Interface card (DIF)

## Institutes: IPNL

- goal: 1 DIF per layer (up to 432 readout ASICs/~30000 channels, now up to 48 readout ASICs)
- Data transmission to/from DAQ by Ethernet
- Clock and synchronization by TTC (already used in LHC)
- Upgrade USB 1.1 to USB 2.0
- new communication bus (I2C) for next generation very front-end ASIC

# Infrastructure for Semi-Digital HCAL

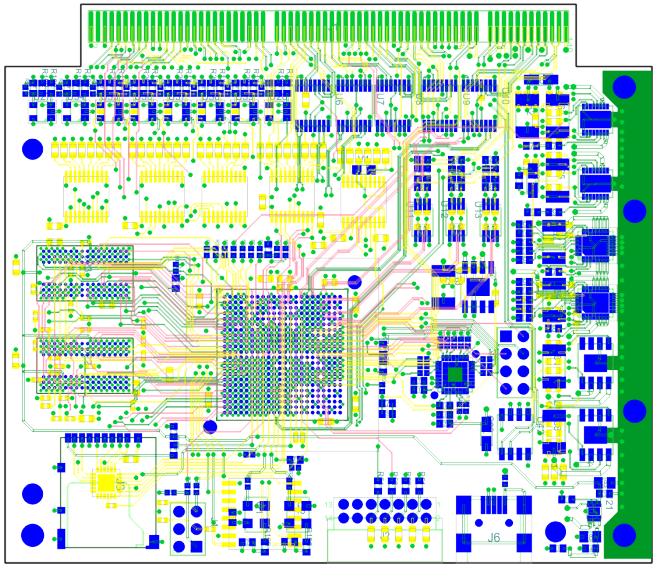
Implementation of a GBT based communication for ROC chips

Institutes: IPNL

- GBT: Gigabit Transceiver protocol, transmission protocol for high speed data transfer in HEP experiments (used in CMS)
- primary design for HARDROC 2 & 3 and PETIROC, but easily adaptable to any ROC very front end ASIC
- hardware platform: new SDHCAL DIF when available, GLIB (from CMS) before
- goal: ILD SDHCAL (low-power GBT) with potential synergy with CMS Muon chambers (low-power GBT or full GBT)
- deadlines
  - HARDROC 2 version: Q4 2015
  - HARDROC 3 version: Q3 2016

# Infrastructure for Analog HCAL

## DAQ for SiPM readout



Detector Interface card (DIF)

Institutes: DESY, IPASCR Prague

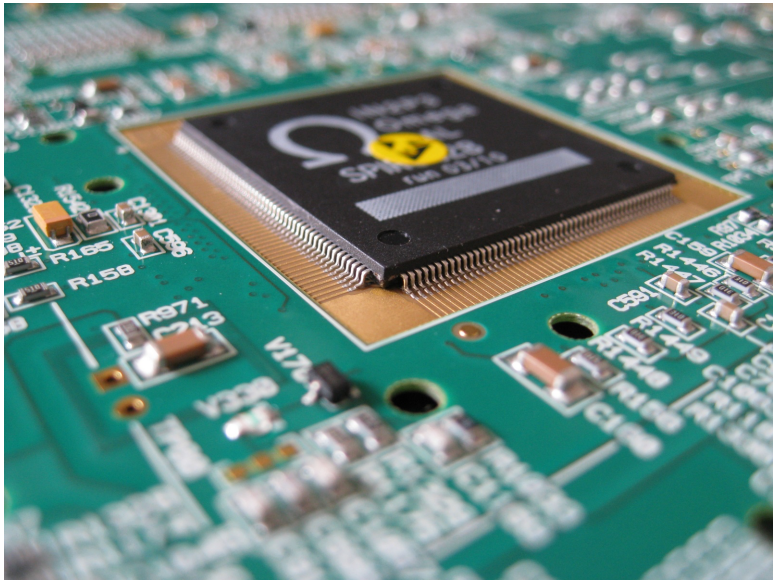
- 1 DIF per ~2500 readout channels
- control of LED calibration system
- existing DIF respects geometry and power consumption restrictions for ILC detector
- uses old FPGA, more flexibility needed
- new communication bus (I2C) for next generation very front-end ASIC

# Infrastructure for Analog HCAL

## ASIC test bench

## Institutes: DESY, U Wuppertal

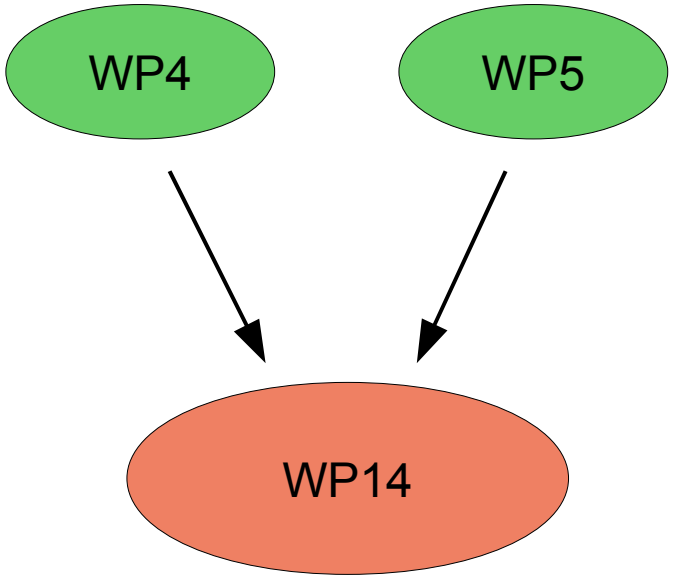
- ~200 000 very front-end ASICs needed for ILD HCAL
- mass testing necessary
- up to now: test board to measure a variety of quantities per channel for one ASIC
- development of a prototype test bench for mass tests of very front-end ASICs



# Connection to other Workpackages

## Integration into common DAQ (WP 5)

- ensure compatibility of calorimeter DAQs
- integration with other detector components
- integration with instrumentation in beam test areas
- common testbeam




## Interface with very front end (WP 4)

- ensure compatibility and system aspects (total power dissipation, space allocation, ...)