Task 14.3: Test infrastructure for innovative calorimeters with semiconductor readout

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on behalf of the WP14.3 task participants

CNRS-LLR, CNRS-LAL,
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UK-IC, CERN
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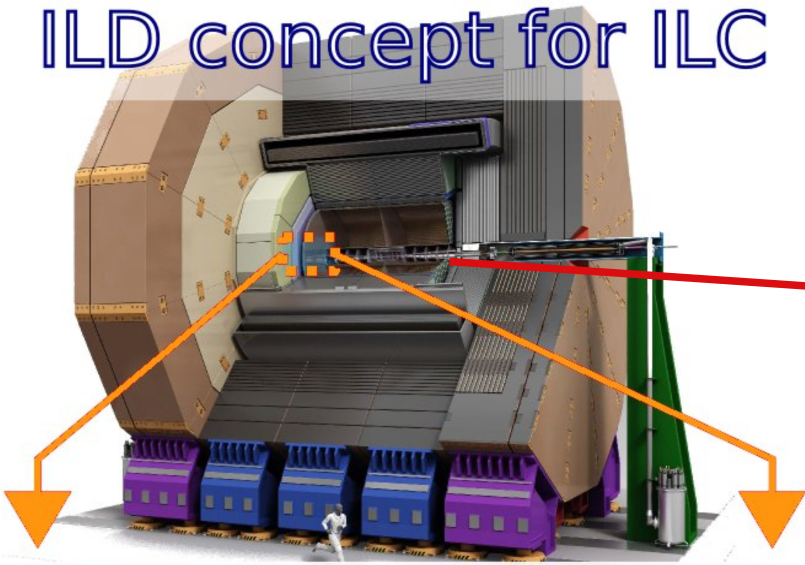
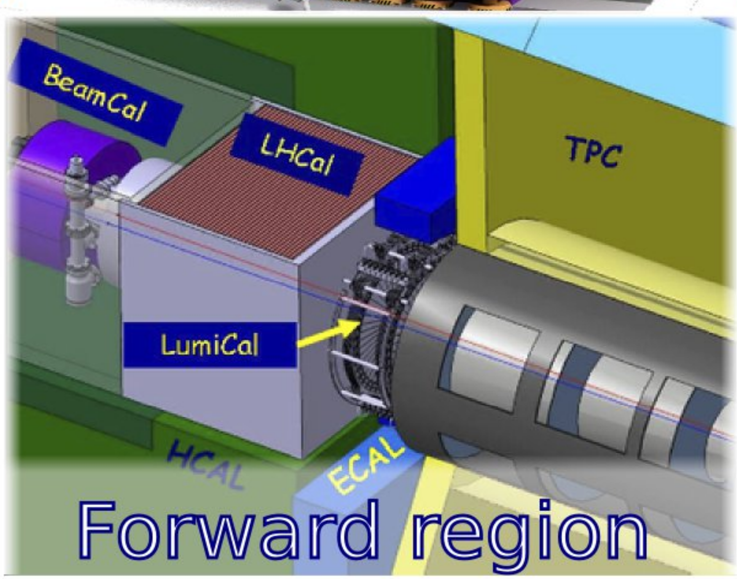
HGCAL

AGH-UST Cracow, DESY Zeuthen,
TAU Tel Aviv & VINCA (with IFJPAN Cracow partner)

AIDA-2020 Kick-Off meeting
3–5th of June, 2015

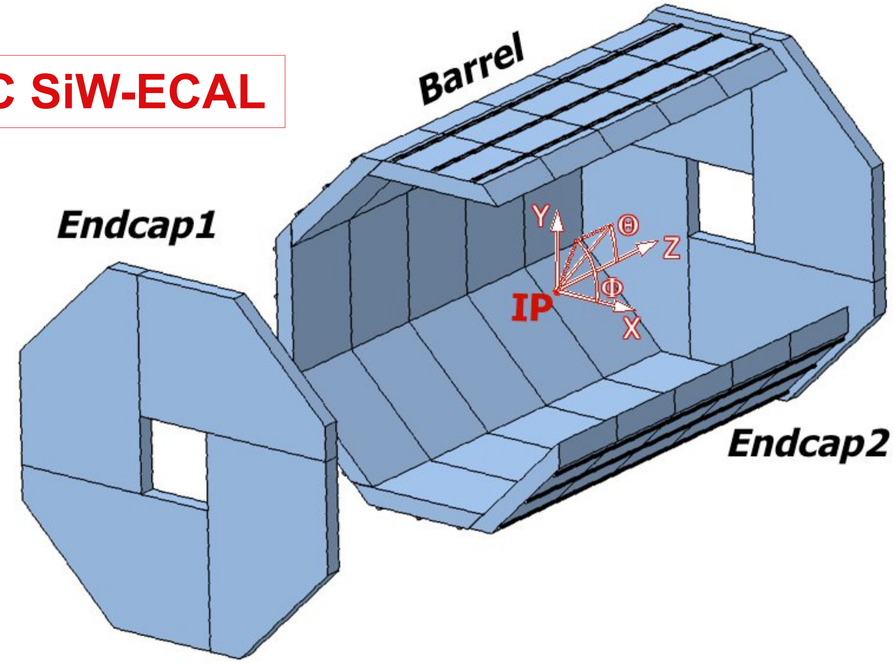
Silicon Sensor calorimeters



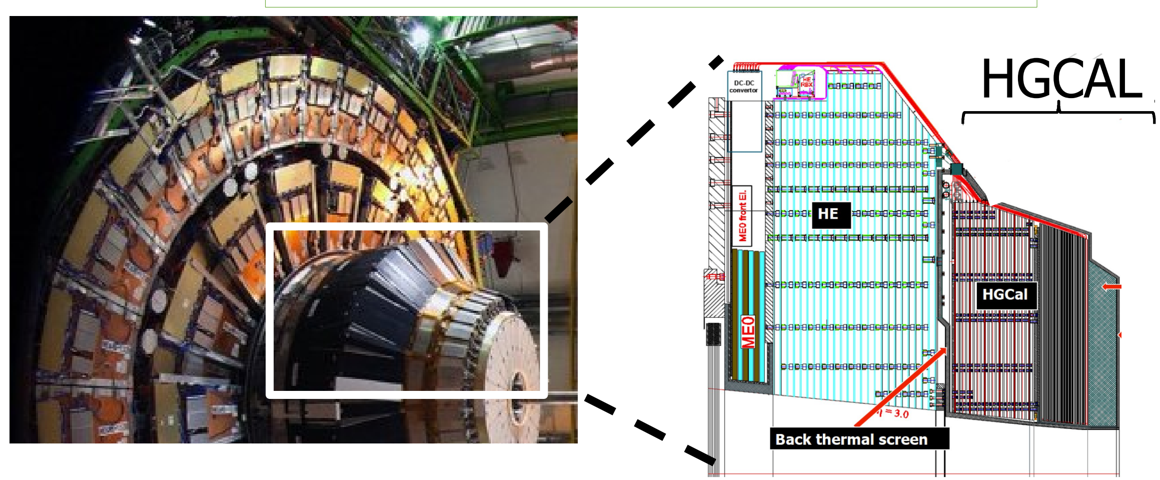


ILC Forward Calorimeters

ILC SiW-ECAL



CMS PHASE 2 Upgrade: HGCAL



Task 14.3 Test infrastructure for innovative calorimeters with semiconductor readout

(**CERN**, **CNRS-LAL, CNRS-LLR, CNRS-LPNHE**, **DESY, TAU, AGH-UST**)

T3.1: Assembly and QA chain for silicon-based ECAL's

- Development of an assembly line for highly granular calorimeters with semiconductor readout
- Test benches for individual silicon wafers and PCB for quality assurance and to study alternatives
- Development of a test station to determine signal characteristics in highly irradiated silicon sensors

T3.2 : Validation of a compact calorimeter prototype including flexible precision mechanics and readout

CALICE SiW-ECAL

Task 14.3.1‘.1’

Calorimeters with pixelated Si wafers allow for an excellent particle separation. After an extensive R&D activity supported by EUDET and AIDA, the next step is the development of tools for construction and quality assurance of large-scale prototypes for an ILC-like detector. This starts with the production of test benches for Si wafers and interface boards. These components are glued together into a detection unit of the order of 20×20 cm² using a robotic system. Up to 10 units will be assembled into detector layers using automated tools.

SiW ECAL: Physics & Technological prototype

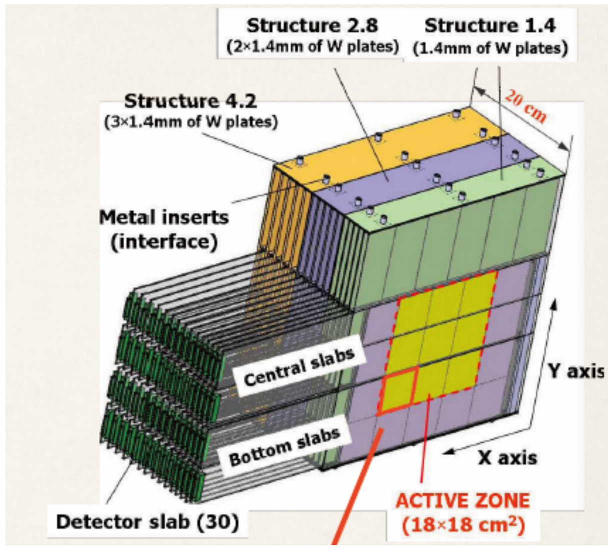
Physics prototype: 2005-2011

PFA proof of concept with comparison to MC (PandoraPFA etc.)

Electronics outside

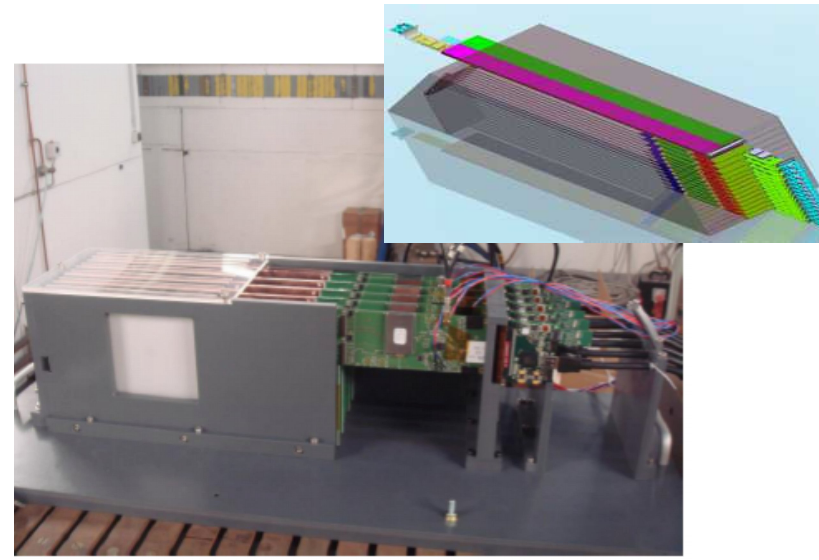
- 1cm x 1cm pixels
- full 30 layers

(used for PAMELA sat.)



16.5%(stochastic) 1–2% (constant) obtained with 1–45 GeV e^-/e^+ at 2006/2008 BT

Technological prototype



Embedded electronics

- SKIROC2 analog/digital ASICs
  - auto-triggered, zero suppr., PP
- pixels 5×5mm²

Assess the feasibility:
Establish procedures and develop
test benches for mass production : ***AIDA-2020, pre-prod test benches.***

- 10 000 SLAB's ⊃ ~75 000 ASU to be produced for ILD

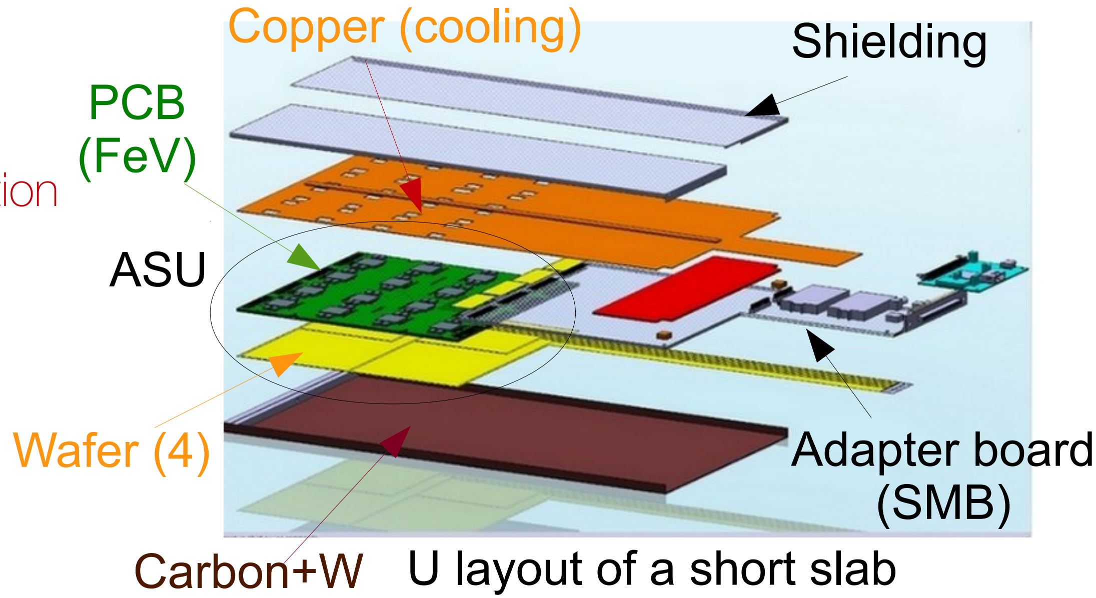
SLAB Assembly: full chain

R&D for “mass production” and QA

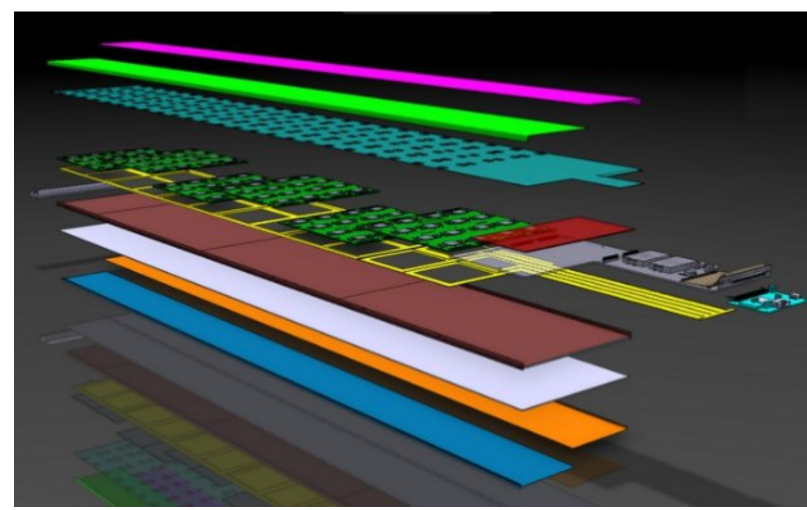
- Quality tests & preparation of large production
- Modularity → ASU & SLABs
  - Choice of square wafers (≠ from hex: SiD, CMS HGCAL)

Numbers (R_{ECAL} = 1,8 m, $|Z_{Endcaps}|$=2,35m) (likely to be reduced by 30–40%)

- **40** Barrel modules: 40 (as of today all identical)
- **24** Endcap Modules: 24 (3 types)
- **9600** Slabs = 6000 (B) + 3600 (EC)
  - many ≠ lengths
- **~75K** ASUs
  - **300K** Wafers (2500 m^2)
  - **1.2M** VFE chips
  - **77M** Channels

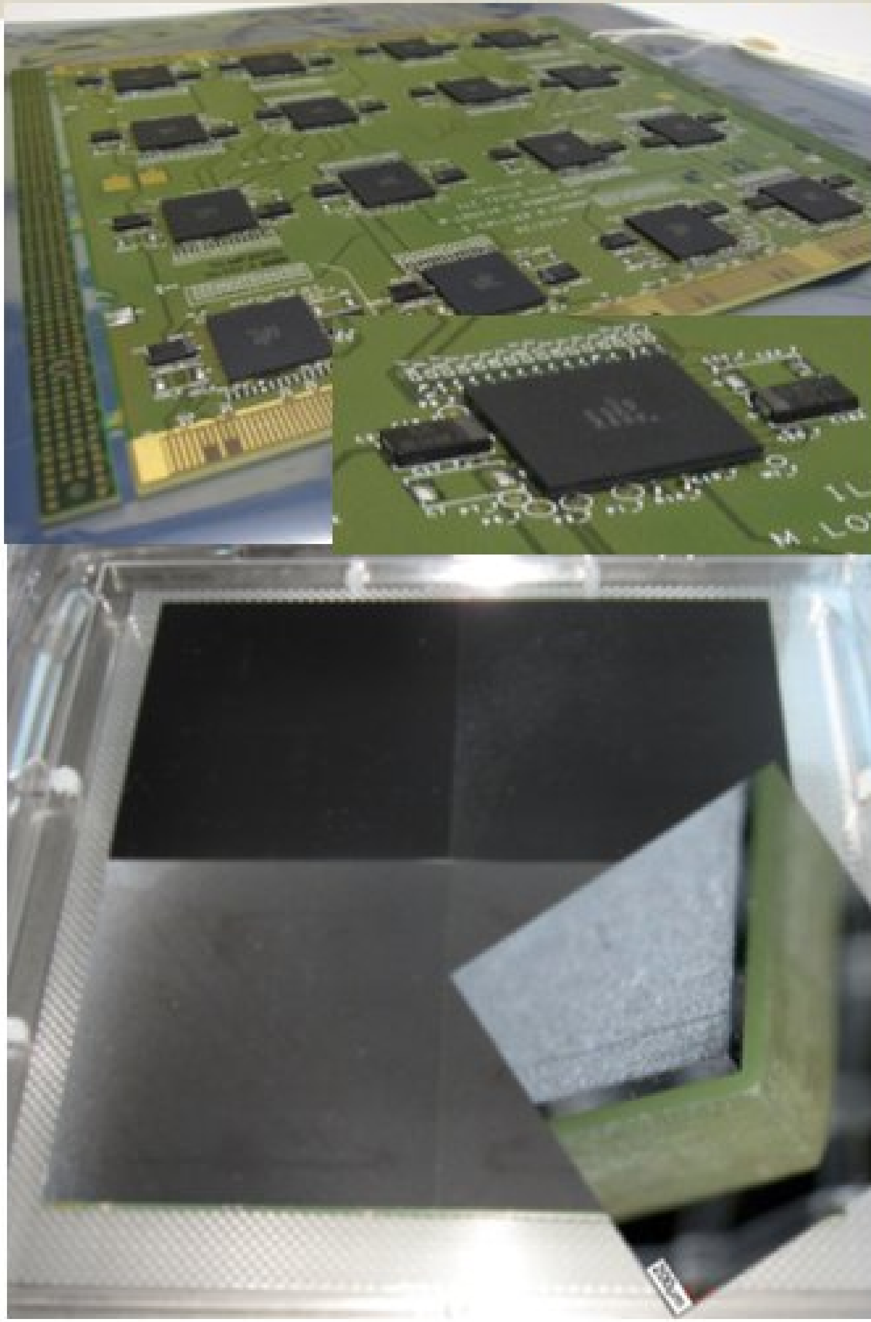


U layout of a short slab

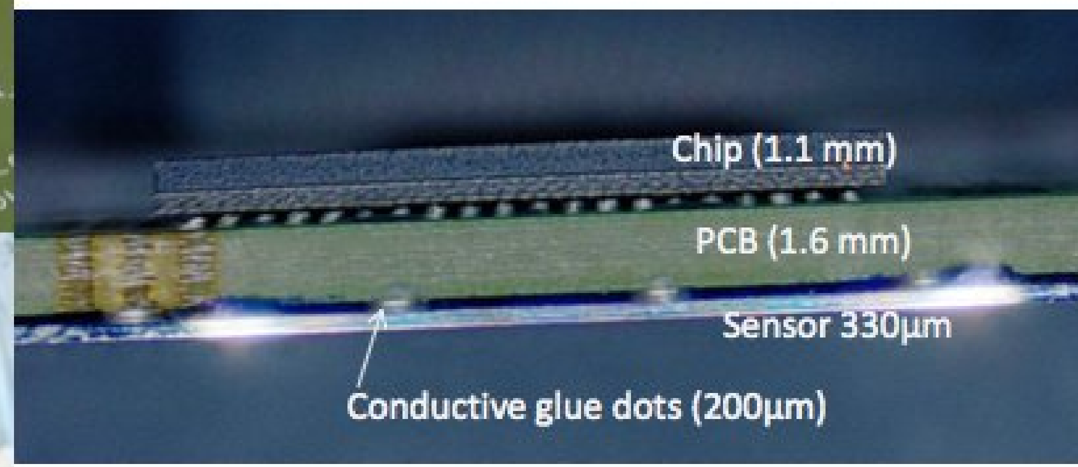


U layout of a long slab

Detector module assembly



Robots for gluing sensors are developed
Manual tools for the assembly of a short slab are existing



4 wafers 9cm x 9 cm wide can be glued with a 20 µm precision and reproducible process.
Glue is dispensed in order to form 200 µm thick dots

Courtesy of R. Cornat

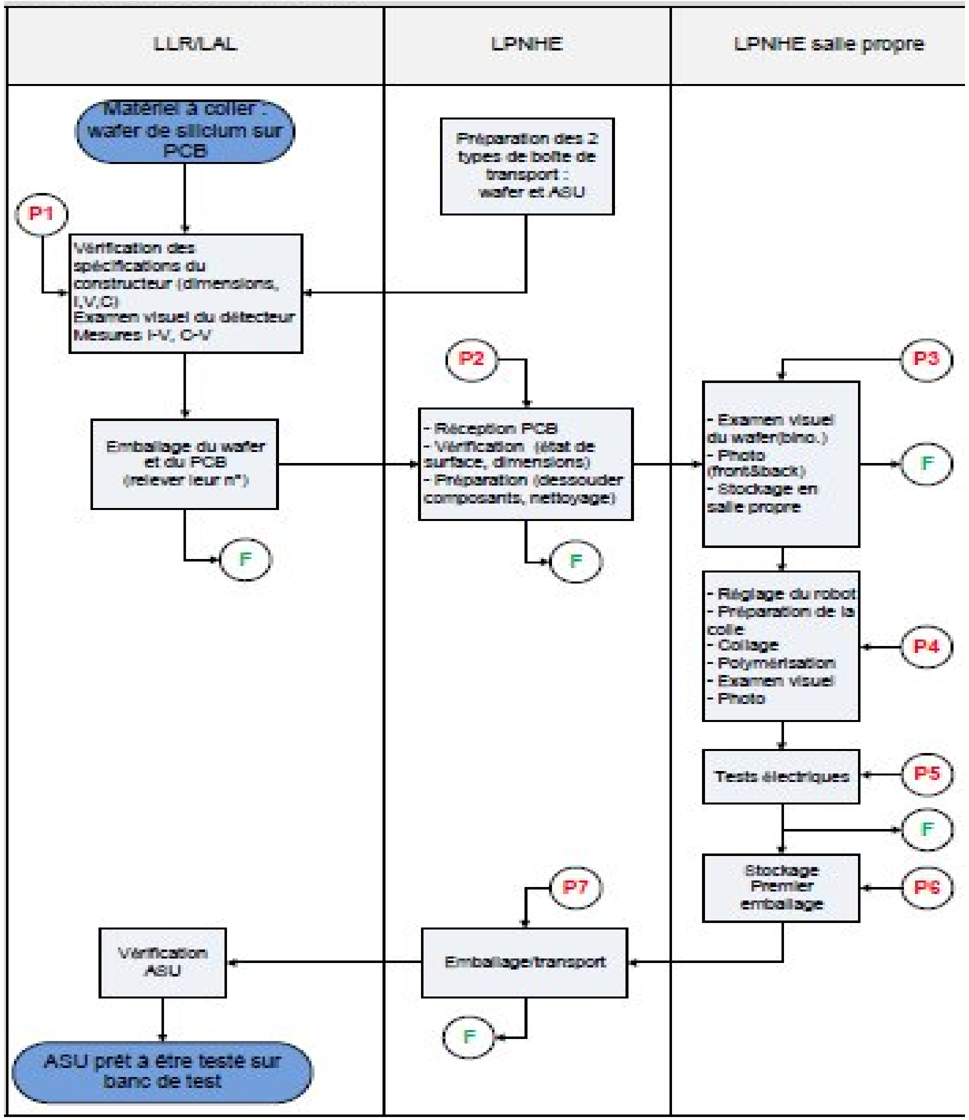
Plans for CALICE/ILC SiW-ECAL

Deliver test benches for a limited production of Detector Assemby Units (ASU)

- Pre-automatic benches being designed
  - LPNHE ↔ LLR ↔ LAL work flow
- Procedure, validation, semi-automatisation part of AIDA-2020-WP14.3.1

Production:

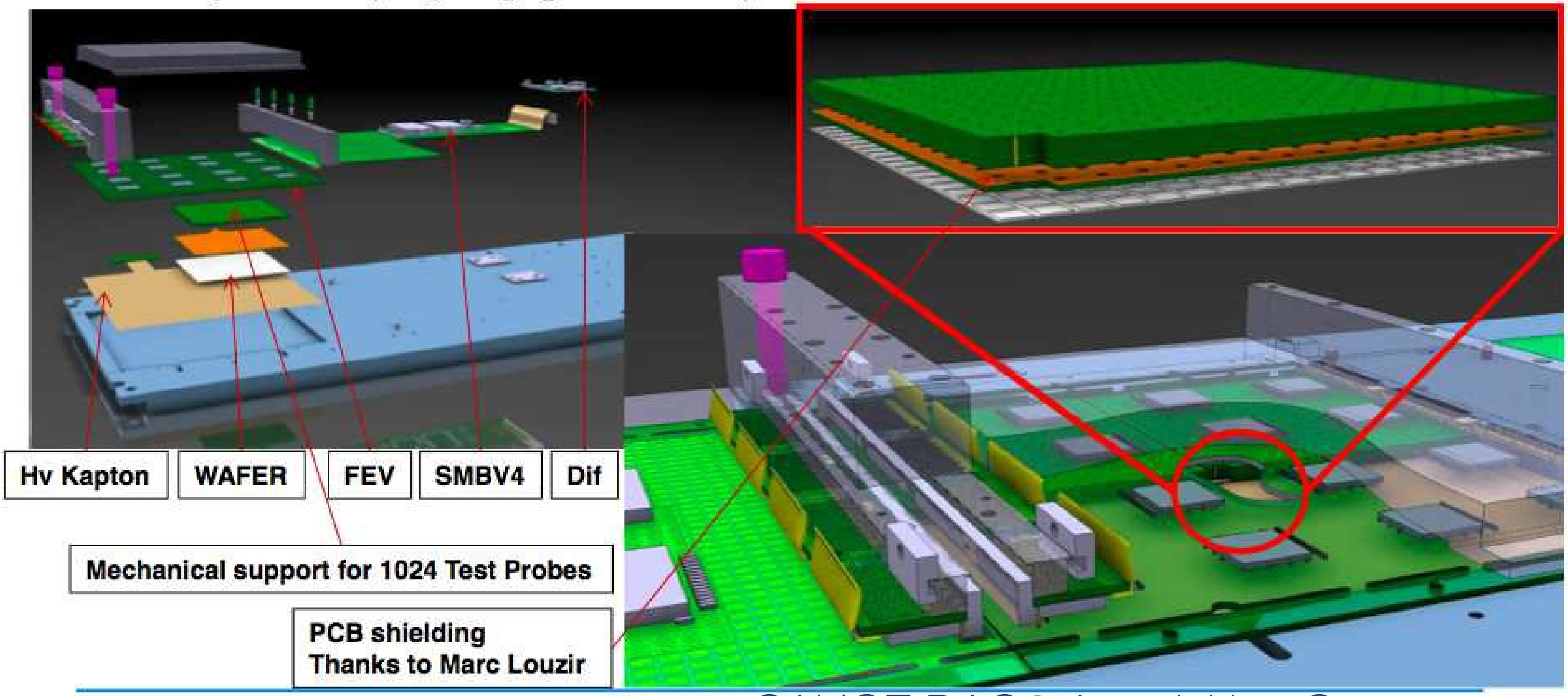
- 2015: 1st batch of ~6–8 ASU's
  - for testing of procedure, debugging, test beam
  - → gain of knowledge on building
  - → 6-7 short slabs + 1 "naked" long SLAB
- 2016: 2nd batch of 12+ ASU
  - aim at semi-automated procedure
  - ≠ type of wafers (edgeless, 500 & 700µm), …
  - 1 SiW Stack + 1 long SLAB



Flexible FE test bench

2.0 – Setup option with support of test electric probes for connecting WAFER to FEV

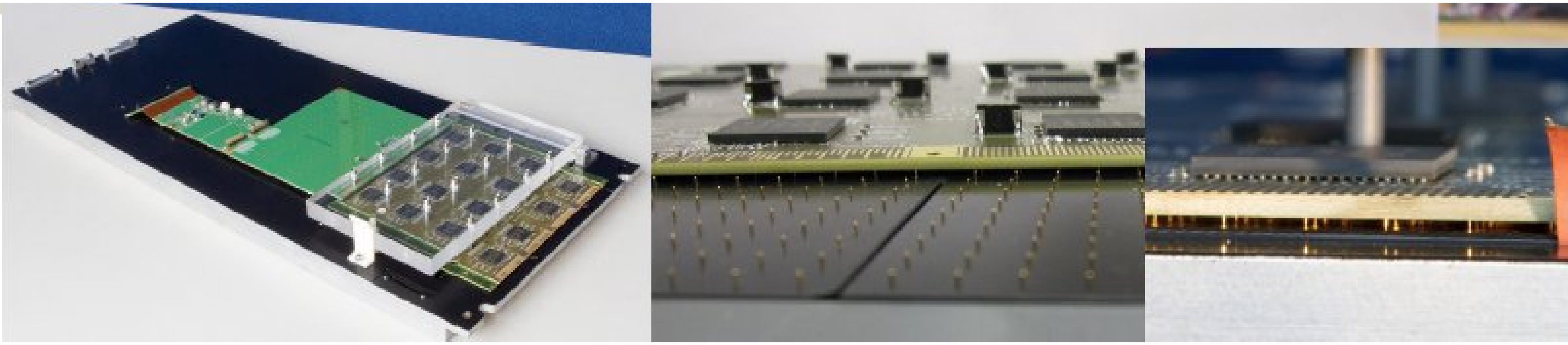
- Realize an assembly with removable wafer in order to acquire cosmic data. This assembly will test the entire acquisition chain (Wafer-FEV-SMBV4-DIF-GDCC-CCC-PC-Software) before the wafer gluing operation. The first test was realized last week

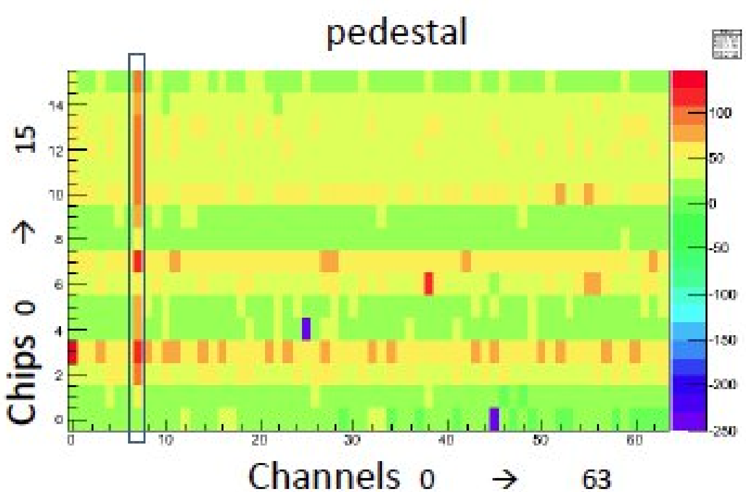


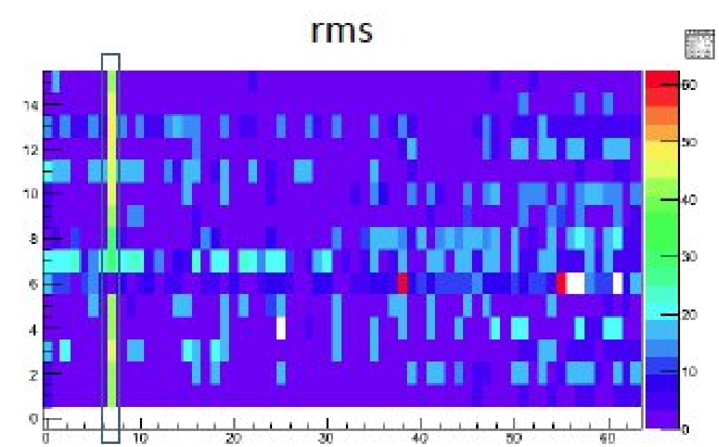
CALICE DAQ2 Acquisition System

Flexible (no gluing, no soldering) benches for R&D
- Qualification of PCB before assembly
  - Basis for later mass test

Flexible bench first results



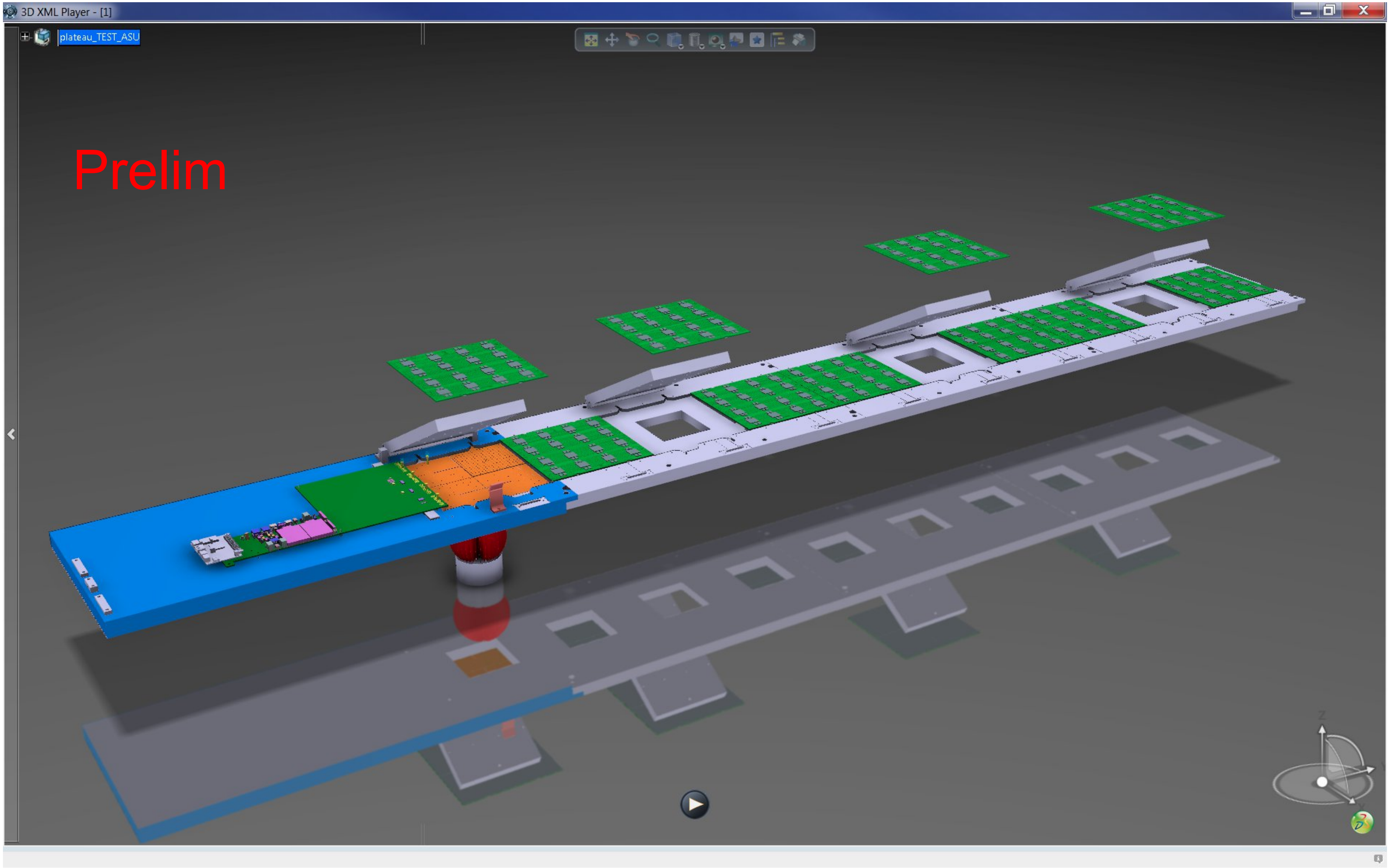




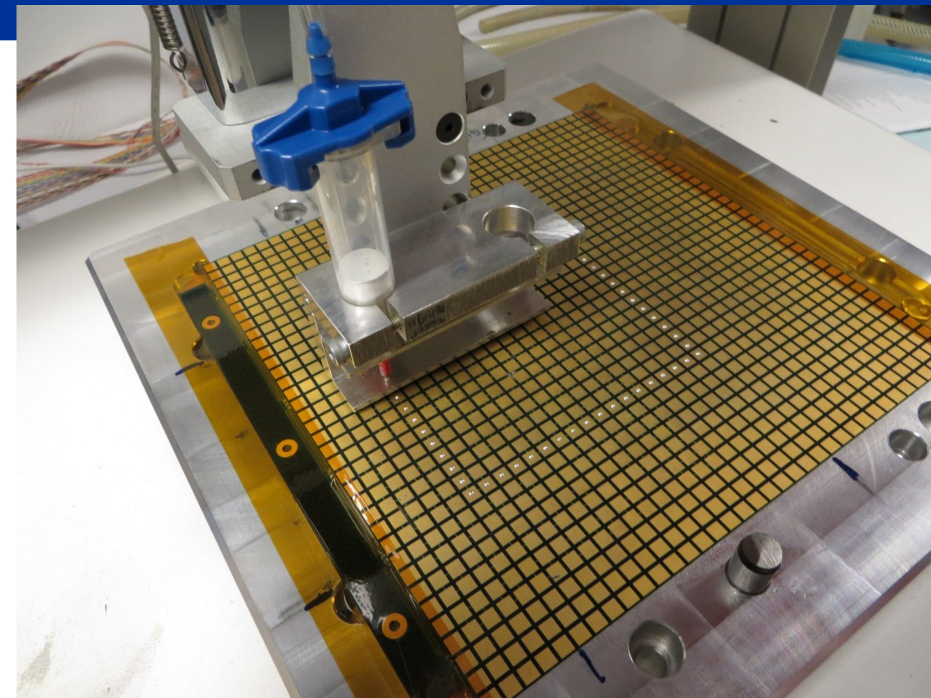
25% of channels are disabled for triggering, all 1024 channels are power pulsed
Chip is triggered injecting a signal on channel 7 (black frame)
Some non uniformity may be due to bad contacts with micro springs (being investigated)

⚠ FIRST TRY ! Much improved results on 1 assembled ASU. ⚠
→ Semi-automated placement and reliability to be developed

Possible extension for long slabs



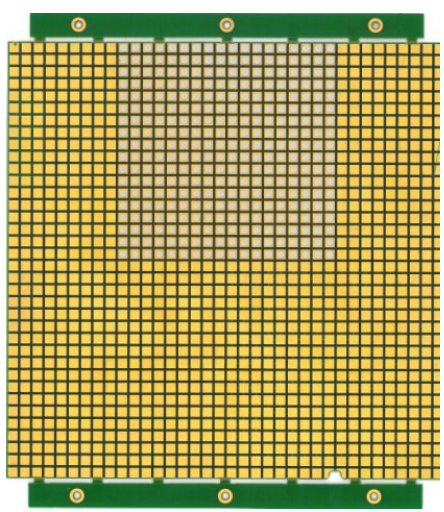
First step : one wafer glued per PCB

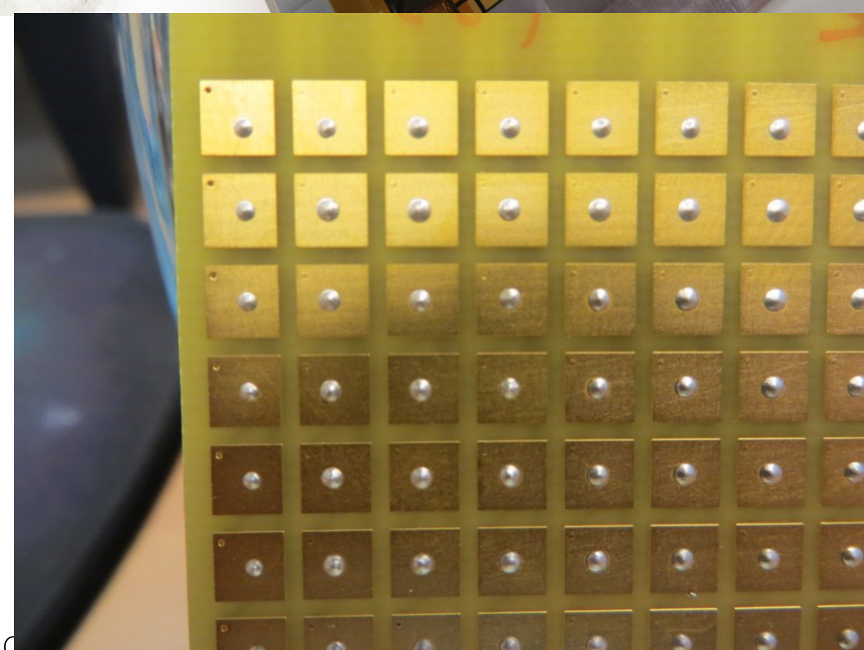


The parameters of the gluing robot have been optimized to glue a silicon sensor (18×18 pads) on a PCB

→ identification of constraints on the PCB geometry:

- Flatness
- Parallelism of the edges
- Uniform height of the ASIC soldered on the board





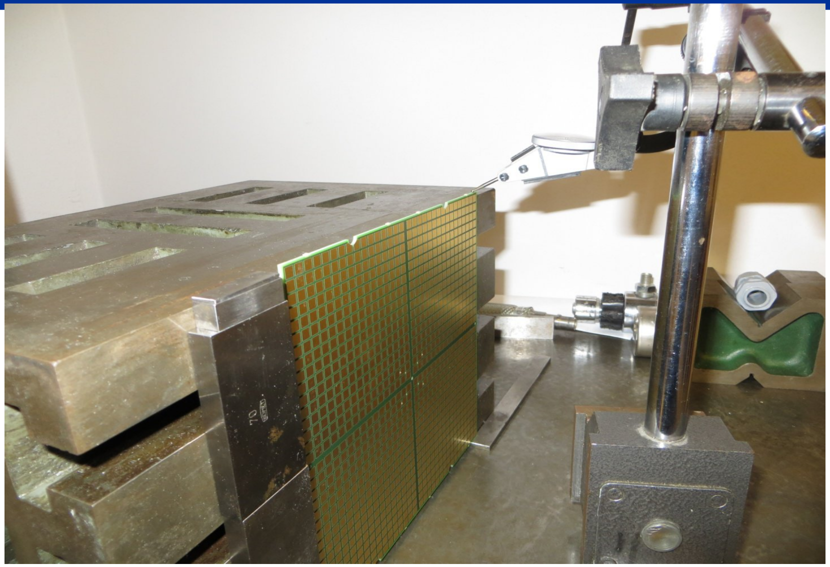
PCB metrology

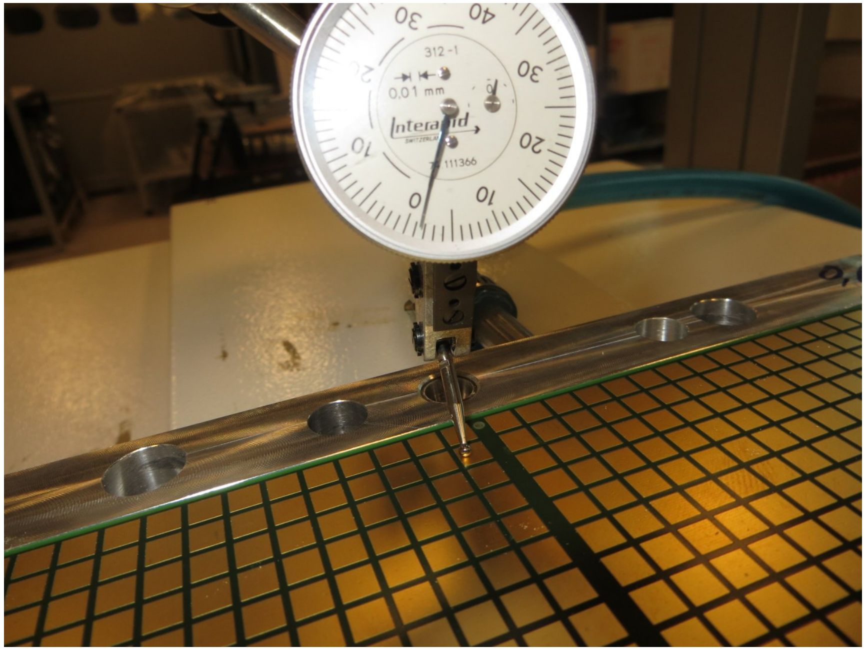
Before cabling:

- Squareness
- Parallelism of edges
- Dimensions
- Thickness (flatness under depression)
- Flatness

After cabling : flatness and thickness

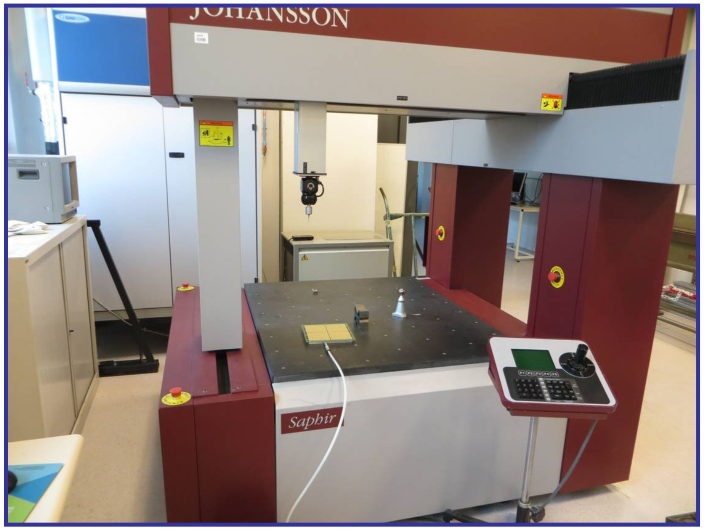
- ATLAS Metrology robot being refurbished

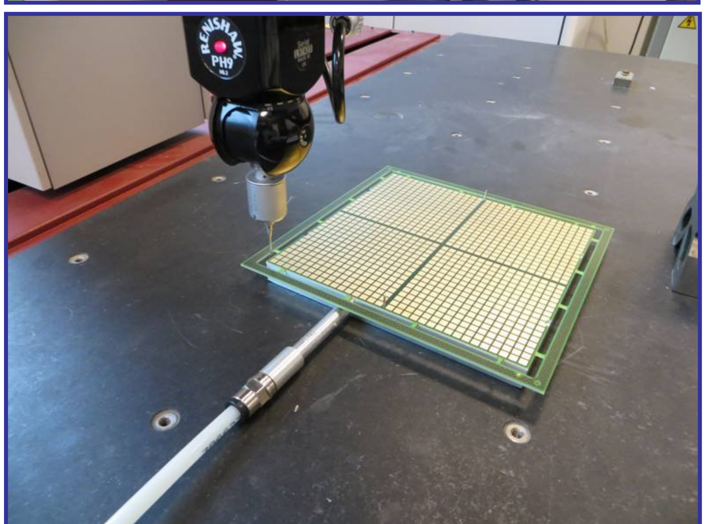


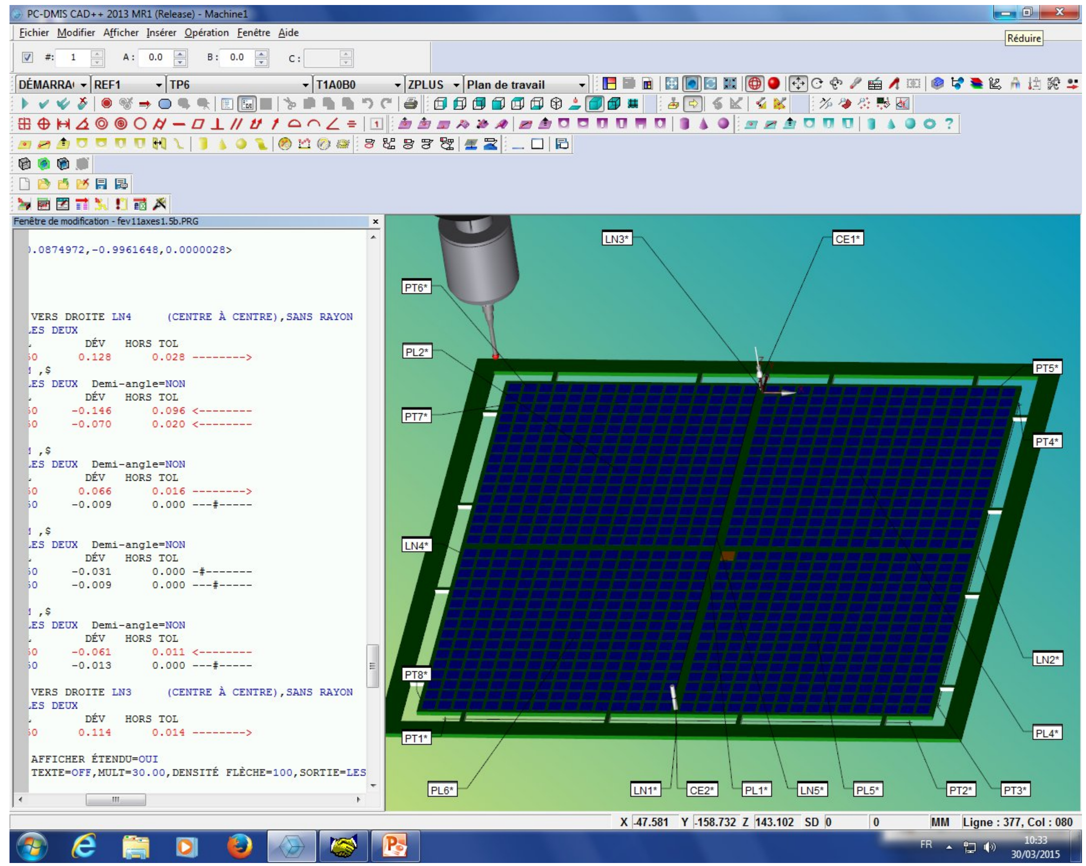


PCB Metrology

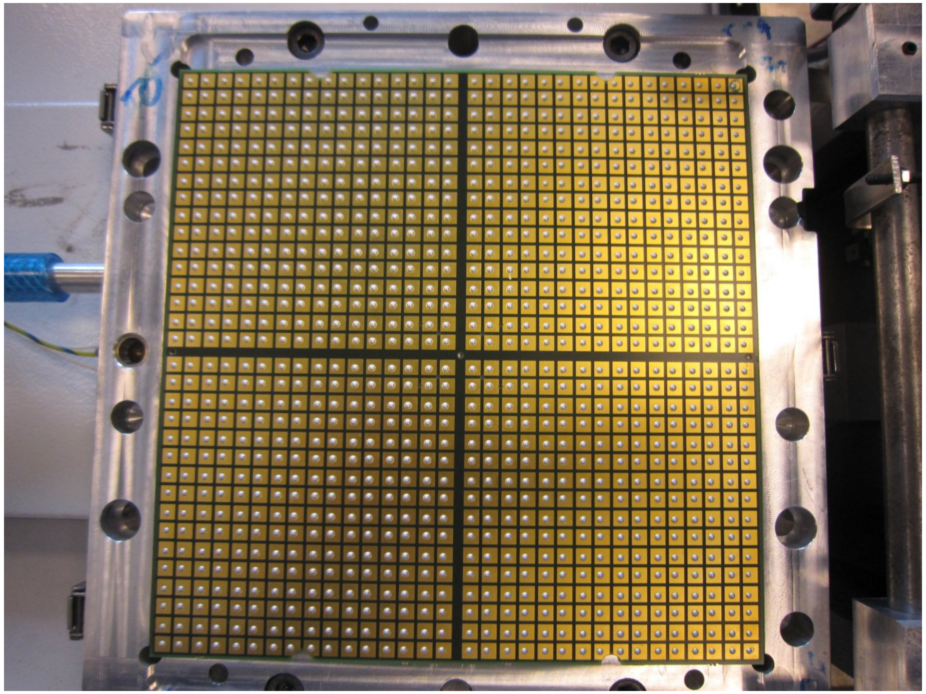
Development of an automatic process using a coordinate measuring machine in one step.



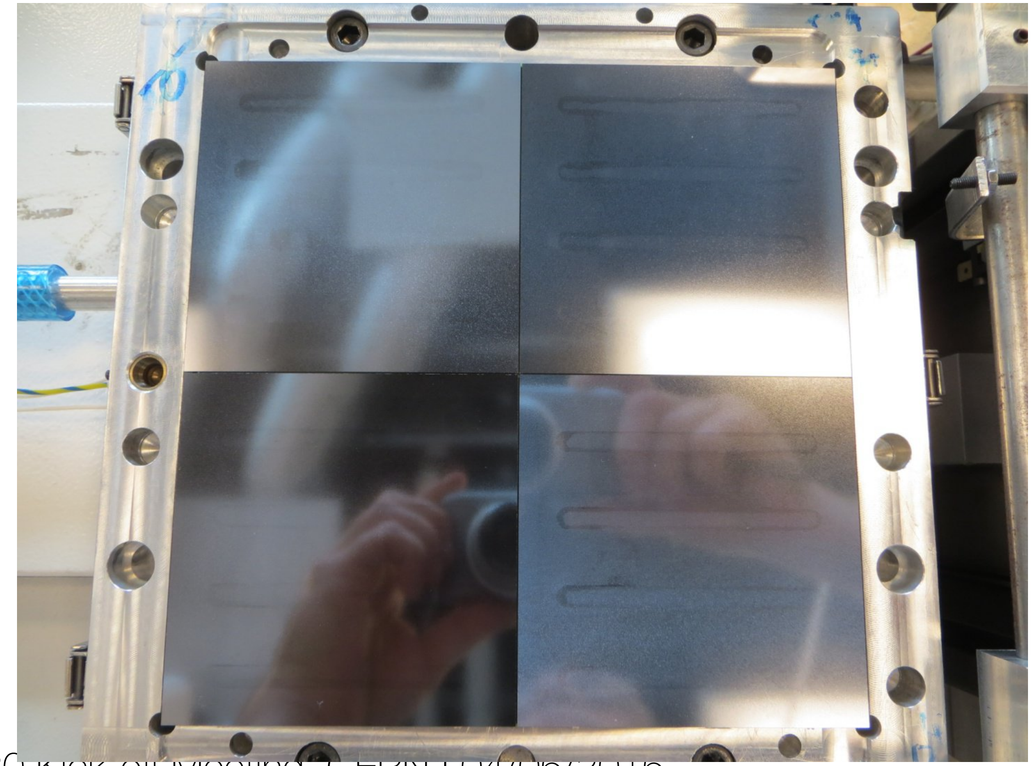




Second step : 4 wafers per PCB



1: Deposit glue on the PCB



2: Move the plate with the 4 wafers over the glue dots

Alignment is fundamental :

– PCB = 180.3 mm maximum
– Wafer = 90 mm

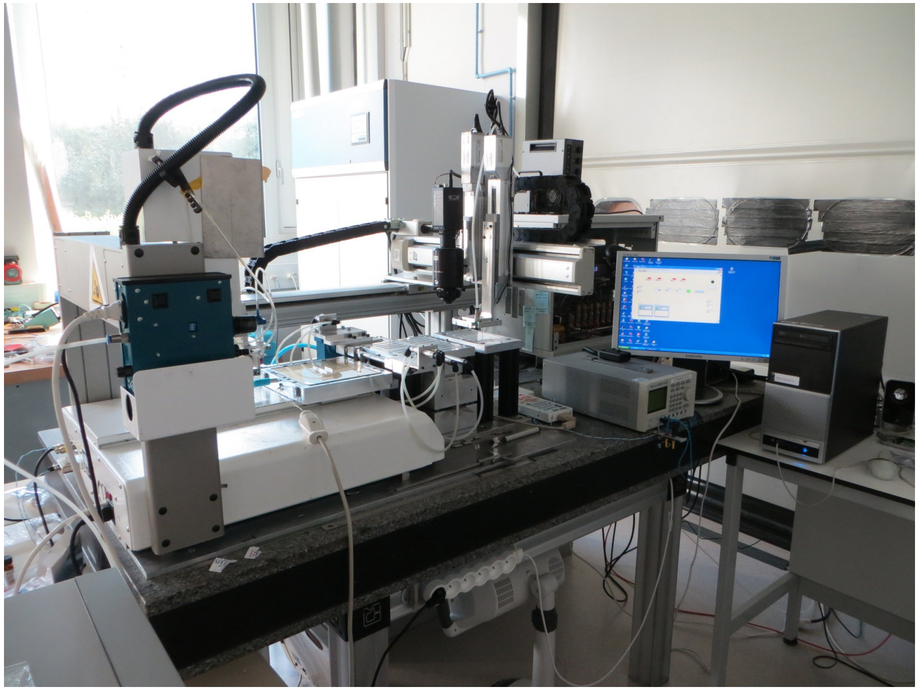
Gluing and positioning automated process

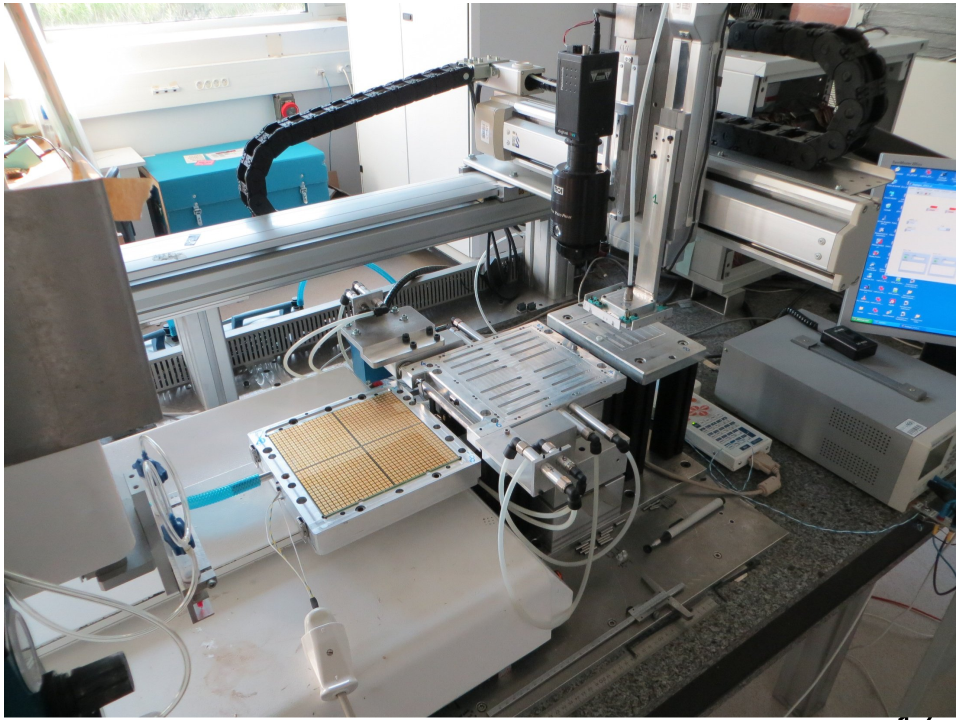
1st version of software (Labview) for the gluing robot implemented.

Second robot for positioning, alignment, and handling has been assembled and its software being developed.

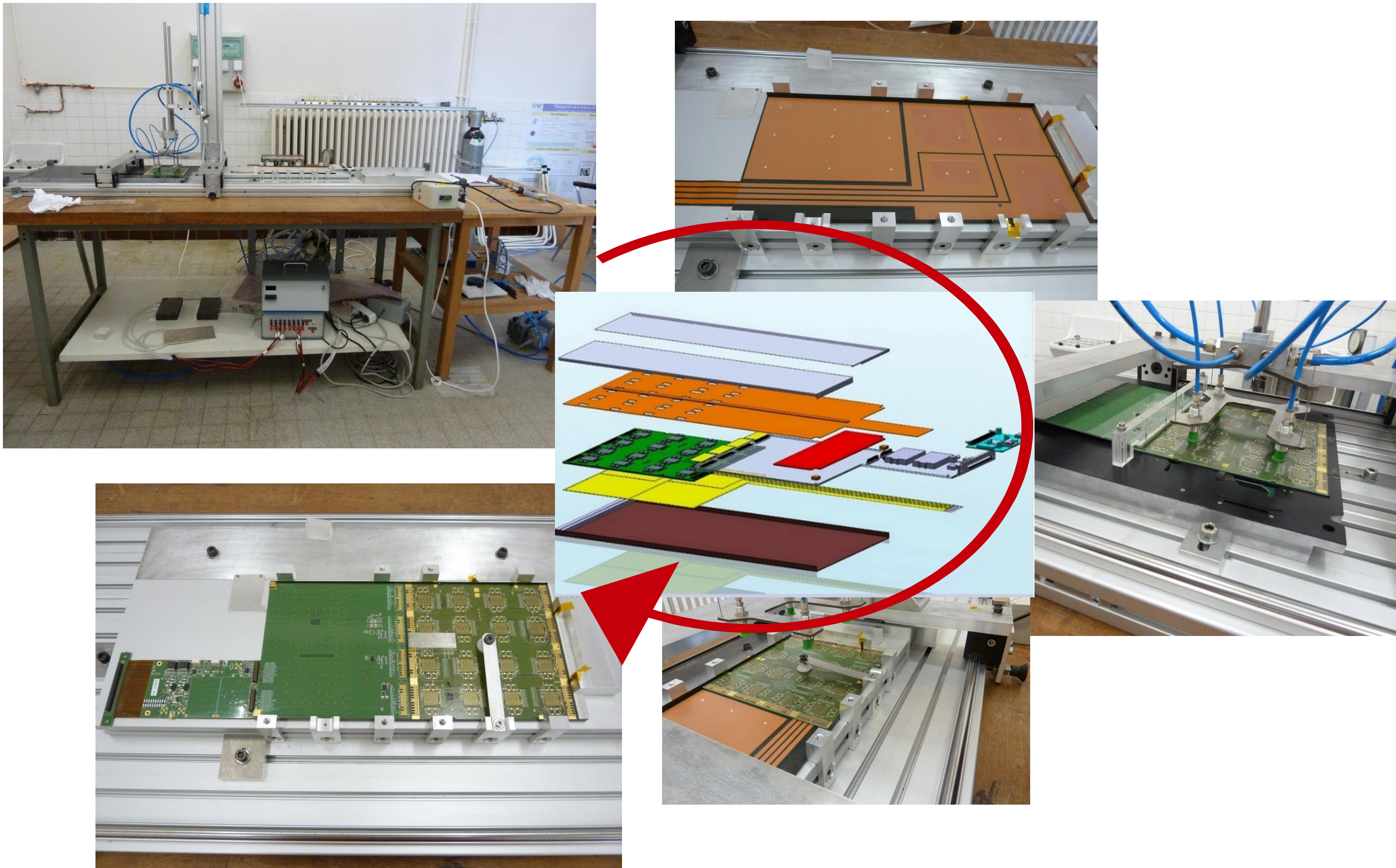
The leakage current after gluing has been checked on each wafer and compared to previous measurements (before gluing)

Full set-up to be completed, documented & tested on small (2015) & larger sets (2016)





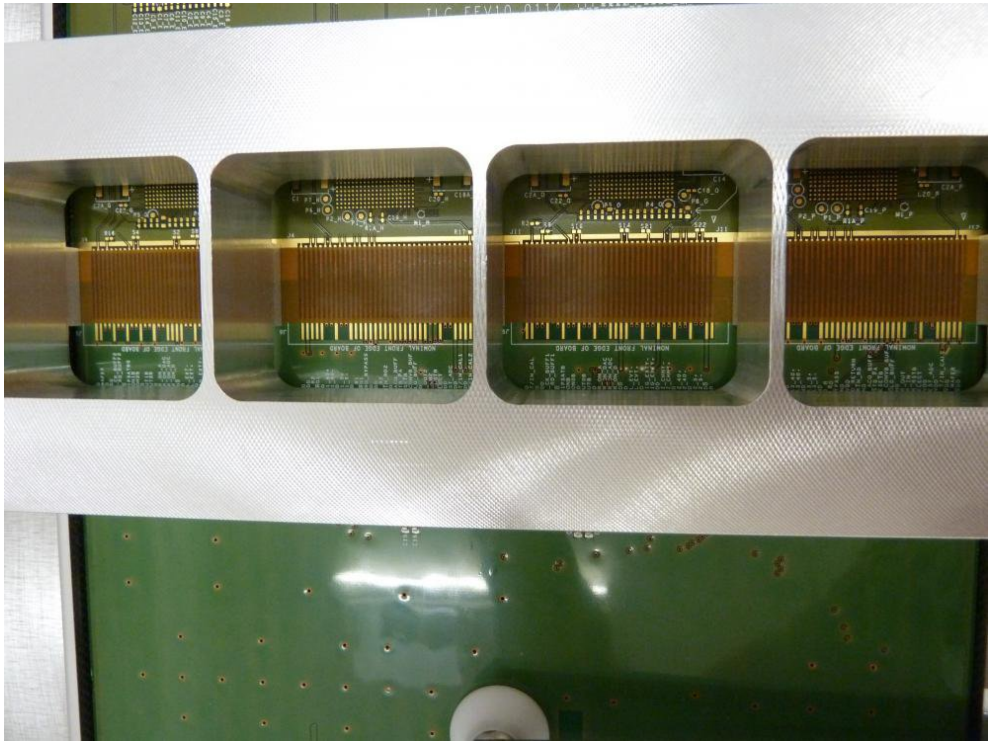
Assembly bench for SiW-ECAL layers



Plus interconnection connection & readout validation

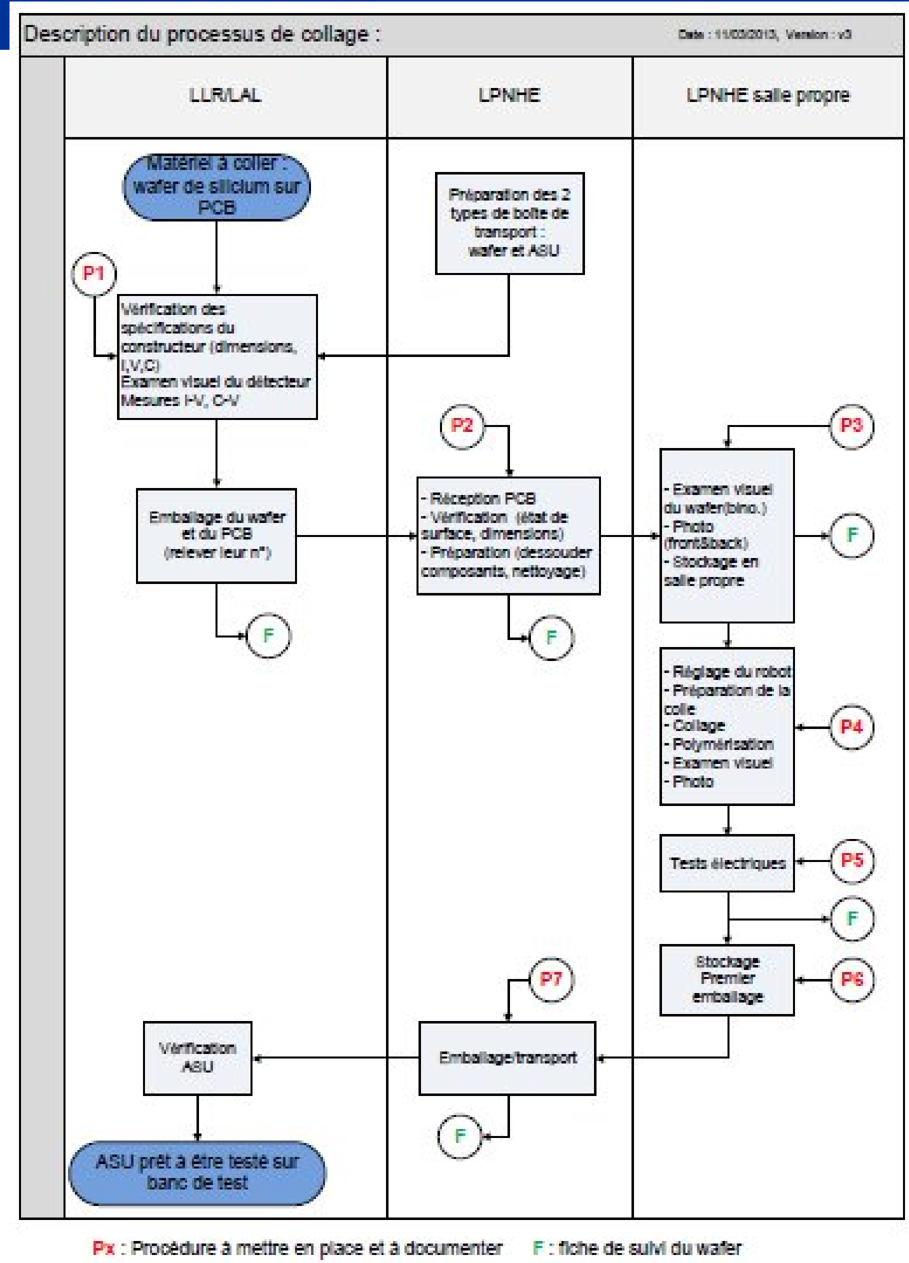
Electric connection

6.1 Interconnection – Placing the frame



Quality Insurance

- Task flow has been completed
- Reception and gluing procedures for 1 and 4 silicon sensors are written
- each operation on PCB is monitored (follow up)
- Each gluing test is registered



Industrialisation

- First contact with EOLANE, company able to propose an industrial gluing process for mass production (LLR/LPNHE).
- EOLANE says the company has capabilities to dedicate one of its production lines to our gluing process.
- EOLANE is studying the compatibility of its know-how to the material (glass then silicon), to the large dimension of PCB, to the repeatability of the alignment, to the quality of the glue and its heat treatment.

éolane

First year of AIDA-2020

Complete the test benches:

- Mostly procedural: to be completed with a small production
- Improve automation
- (Small) improvements for secure handling of critical parts (wafers)

Small production (D14.3.1)

CMS–HGCAL

Task 14.3.1'.2'

Such a calorimeter could be also a viable option in a hadron collider environment, such as CMS.
A dedicated test set-up is needed to test the signal characteristics of irradiated Si wafers operated at temperature at or below -35 degrees C.

Background

The challenge of High $\mathcal{L}$ LHC

- Preserve the sensitivity for the 125 GeV Higgs boson including for rare production and decay channels while exploring the TeV scale (e.g. SUSY) in a very high pile-up environment

Phase 2 $\sqrt{s_{pp}}$ = 13-14 TeV $\int L\, dt = 3000\ fb^{-1}$

Run IV 2025-203x HL-LHC

LS3 ≡ phase 2 upgrades

- Operate at 5 x 10^{34} cm^{-2} s^{-1} with 25 ns beam crossings (<PU> ~140)

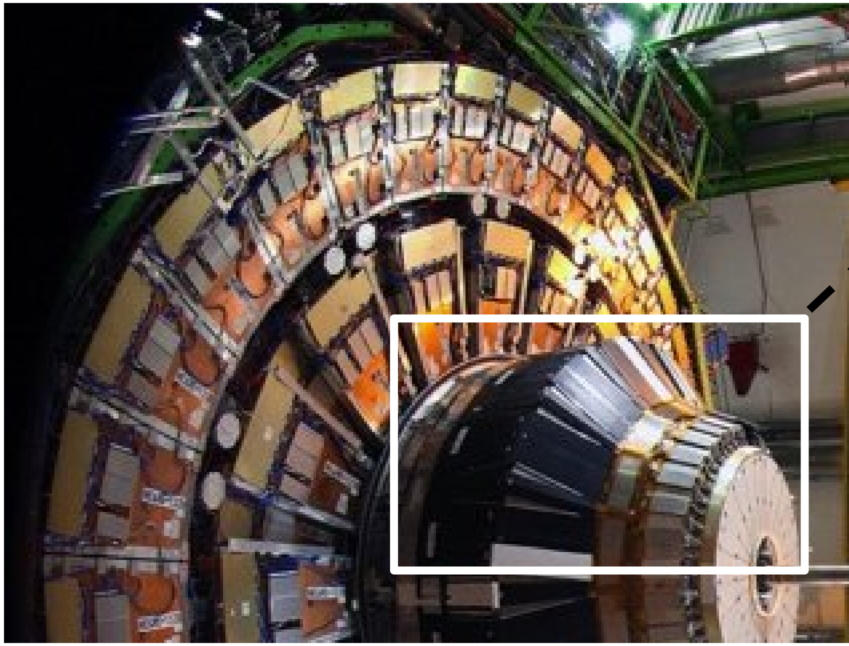
Forward **HGCAL:**

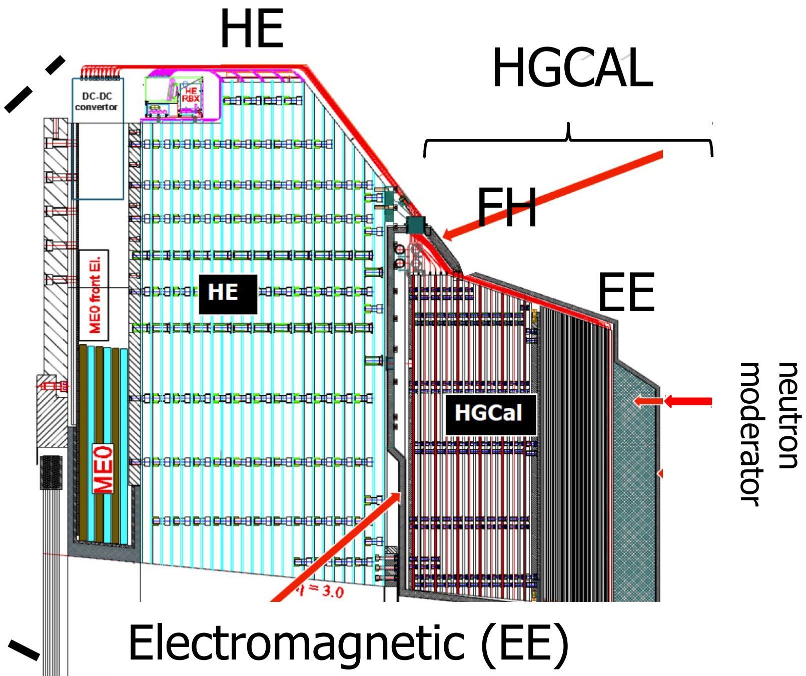
Aim for a dense and highly granular 3D sampling calorimeter inspired by CALICE (ILC), adapted to HL-LHC very high event rates

Exploit topology of deposits and shower tracking capabilities in a particle flow reconstruction both for trigger and offline analysis

HGCAL

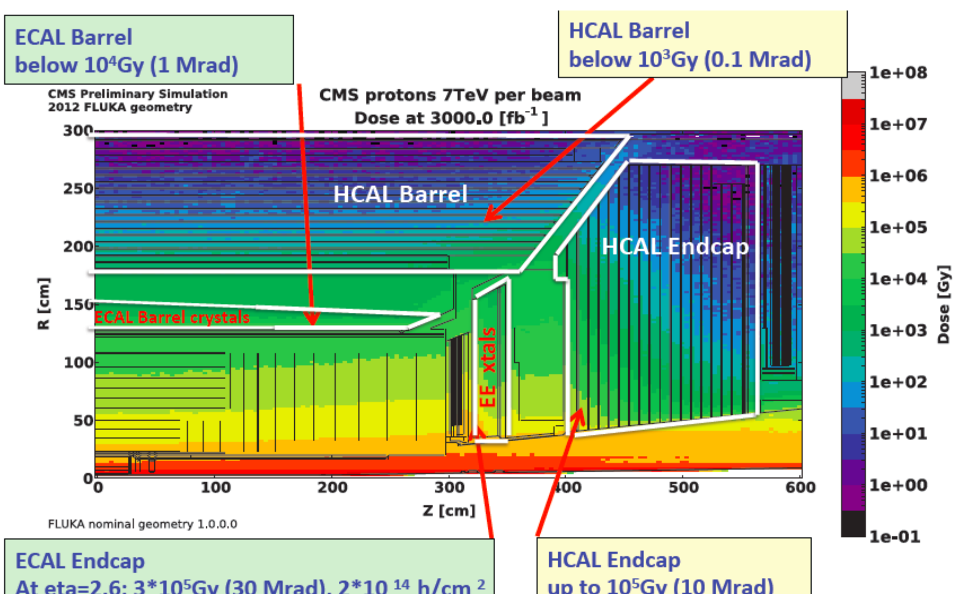
EE	Cu-W / Si	26 X_0 (1.5 λ)
FH	Brass / Si	3.5 λ
HE	Cu / scint. tiles	5 λ





Electromagnetic (EE)
26 X_0 28 layers
$10 \times 0.64\ X_0$ +
$10 \times 0.88\ X_0$ +
$9 \times 1.1\ X_0$

η dependent
- depletion of the Si
- cell size



Absorbed dose in the CMS cavern
after an integrated luminosity of 3000 fb-1

HL-LHC × 12 wrt LHC

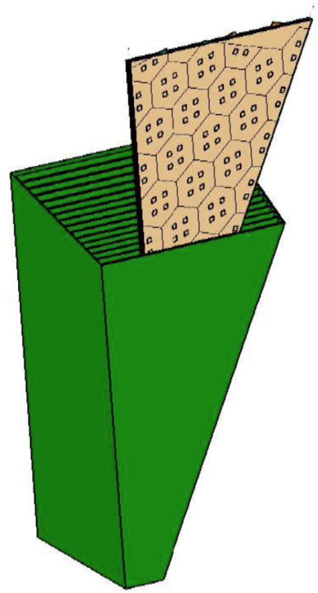
The HGCAL Mechanics (prelim)

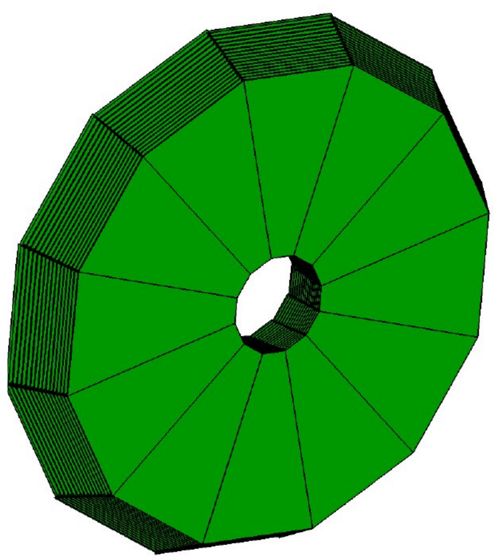
Petal/Wedge
Carbon Fibre Structure with embedded W Plates (3° tilt)

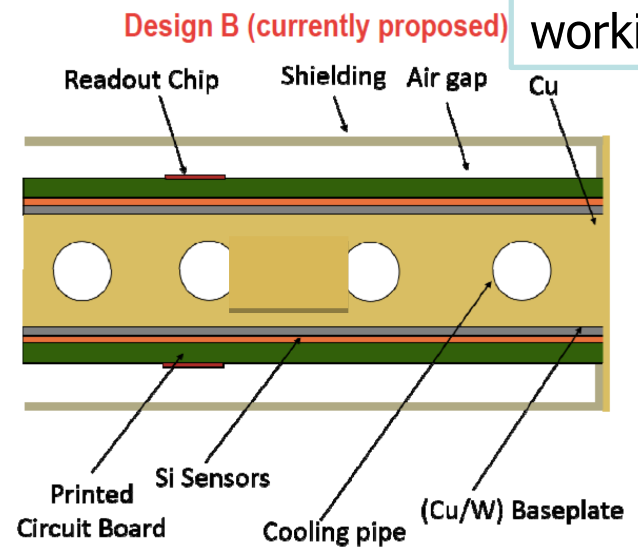
Wedges to be glued together to form a **monolithic structure**

Si readout
W + Cu absorbent
2 readout layers/cassette

C02 **cooling**
working temp: -30°C

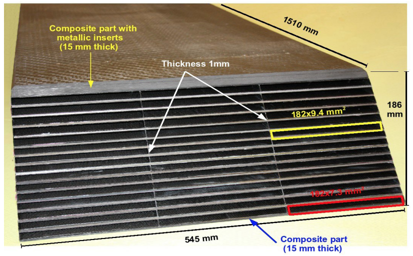




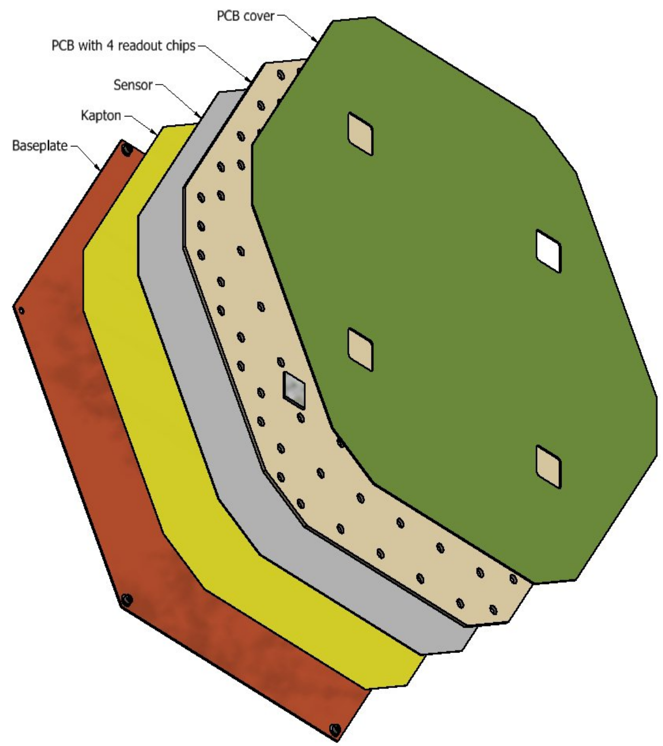


2 read-out layers per cassette sliding in each slot

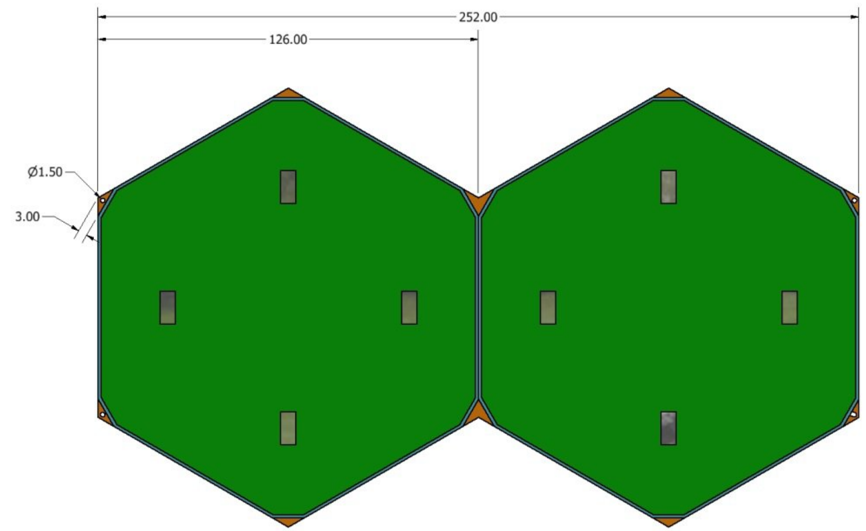
Building technique inspired by the R&D for CALICE (ILC), e.g. large prototype + demonstrators of a cassette have been made at LLR (in Si+Pb/W) and at FNAL

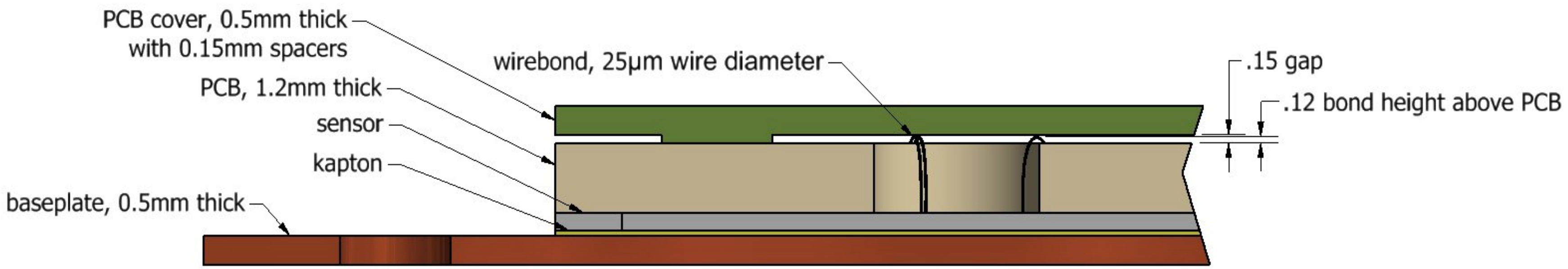


The HGCAL Readout Modules (prelim)



1 "module" = 2 × 6″ Wafers





CMS-HGCAL for HL-LHC

Moving fast:

- HGCAL has been officially approved 8th of May 2015 by CMS CB
- Jim Virdee appointed "interim HGC project manager"
- Groups are joining fast, collaboration is being set-up
- Plans:
  - Construction : 2019–2023
  - R&D phase: Q2 2015 → Q2 2019
    - TDR scheduled by the end of 2017
      - » TB of 1st prototype Fall 2015 @ FNAL
      - » TB of 1st stack (physical proto) Spring 2016 @ CERN

Plans for TB being elaborated…
(everything susceptible to change)

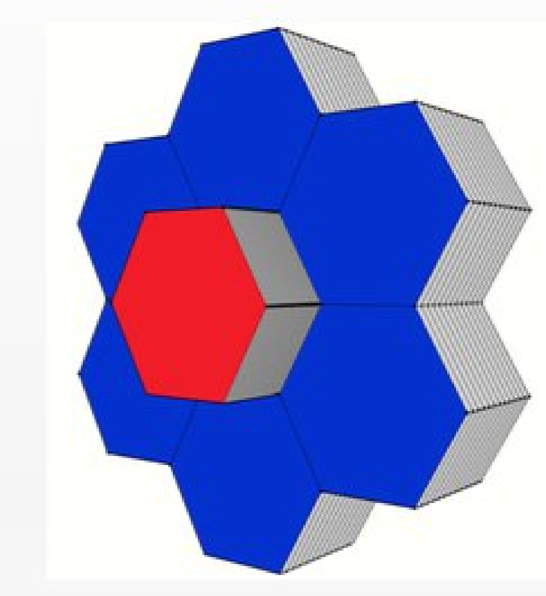
Plans

- *Once we have approval by the collaboration we will need to start an extensive test program for HGC.* ✔
- *Validate many characteristics of HGC that we have derived from CALICE data or from simulations.*
- *The first small-scale prototype detector will be an EE module with an FH behind.*
- *Will use this to obtain data that we need for the TDR.*

Courtesy of R. Russack

1st Prototype Concept

- *Small EE-section.*
  - 28-layers of 6" sensors



Tentative schedule:

- 300mμm Wafer prod for EE in oct.
- complete FH by mid-march → TB in 2016

CMS R&D

Important (final ?) decision: use of SKIROC2 from CNRS-Omega for the 1st test

- → to a close collaboration HGCAL – SiW-ECAL, e.g.
  - common chips characterisation, DAQ, common beam test & analysis
  - adaptation of CALICE test benches ?
  - chip production (SK2a) & testing (WP14.4)

Design of the test module and the final readout electronics is on-going:

- the design of the cooled set-up will follow (CERN, Imperial Coll.)
  - MS14.4: «Design specifications of test stations for irradiated silicon sensors and LHC oriented front-end electronics» due M12.

Forward Calorimetry
Task 14.3.2

«Infrastructure for very compact Tungsten based calorimetry
Calorimeters in the forward regions at a Linear Collider must be compact and equipped with fast readout and data acquisition. A design of such calorimeters exists; sensors and front-end ASICs were developed. Single sensor planes were successfully tested in test beams. The next step is a multilayer prototype to validate Monte-Carlo simulations with test-beam data. An available mechanical frame can house up to 30 thin absorber planes. For up to 10 instrumented sensor planes, readout ASICs will be produced and integrated into the readout system. »

Task description (from AIDA-2020 proposal)

Infrastructure for very compact tungsten based calorimetry

Calorimeters in the forward regions at a Linear Collider must be **compact** and equipped with fast readout and data acquisition.

A design of such calorimeters exists; sensors and front-end ASICs were developed. Single sensor planes were successfully tested in test beams.

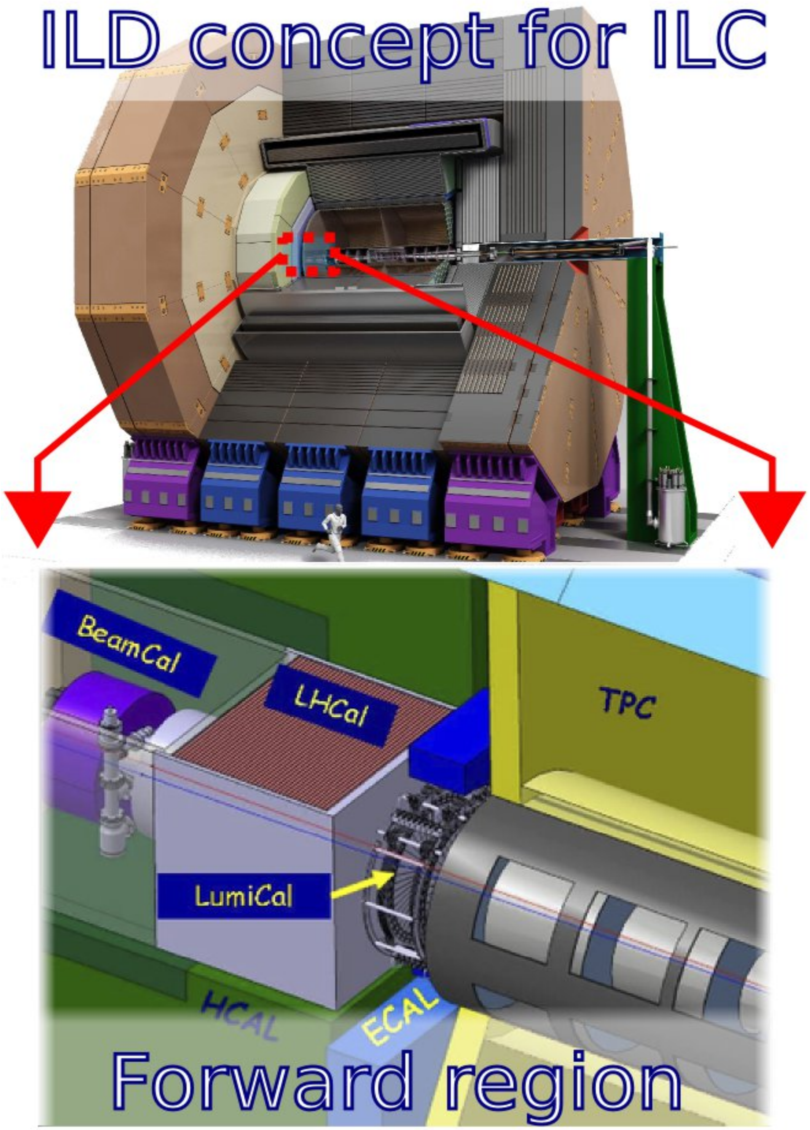
The next step is a multilayer prototype to validate Monte-Carlo simulations with test-beam data. An available mechanical frame can house up to 30 thin absorber planes. For up to 10 instrumented sensor planes, readout ASICs will be produced and integrated into the readout system.

Deliverable
(from AIDA-2020 proposal)

D14.4 Very compact calorimeters (AGH-UST)

Development of a flexible mechanical frame to be completed with thin precise absorber plates with a total depth of 30 radiation lengths, validation in beam tests.

Motivation for this work



Development of the very forward region calorimeters (BeamCal and LumiCal) with specific requirements:

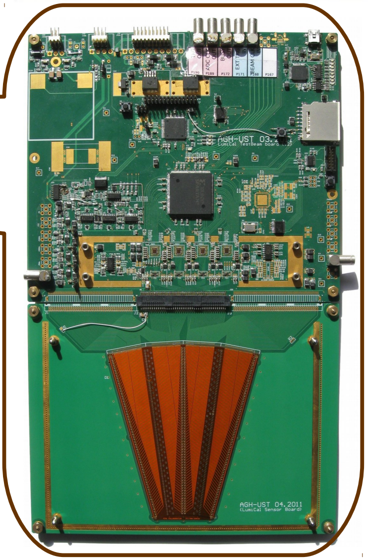
- Compact (small Moliere radius)
- Fast readout
- Radiation hard (BeamCal)

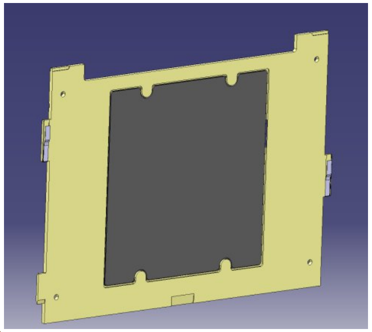
for the measurement of luminosity and the beam monitoring in future Linear Collider

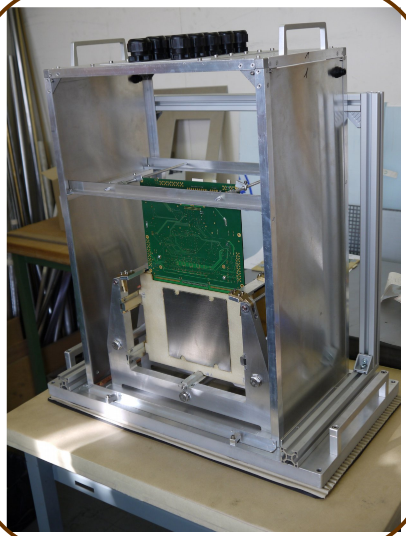
Infrastructure for forward calorimeter
Present status and the goal in AIDA-2020

LumiCal/BeamCal calorimeter infrastructure comprises:

- Detector modules:
  - Sensor modules for BeamCal/LumiCal
  - Readout ASICs
  - Back-end electronics
- Absorber layers
- Precise mechanical frame
- Data acquisition system (EUDAQ software is used)







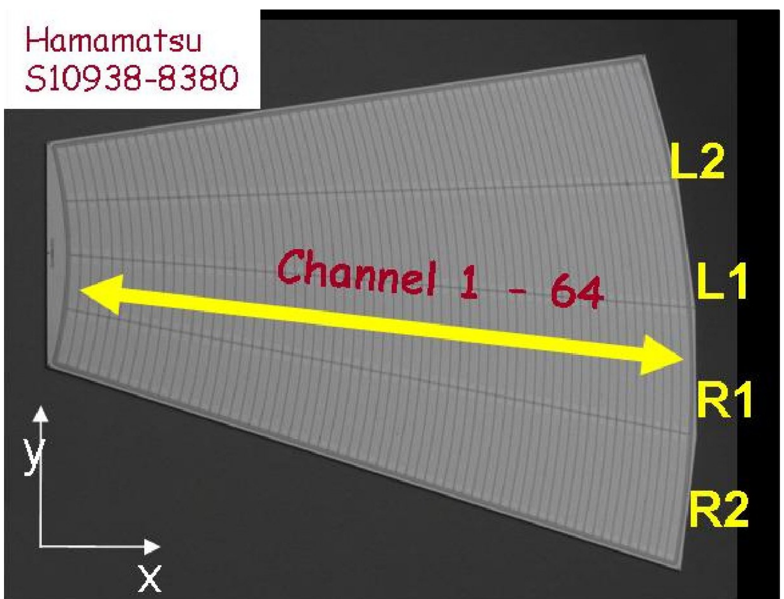
Present calorimeter prototype is not compact enough... (large Moliere radius)

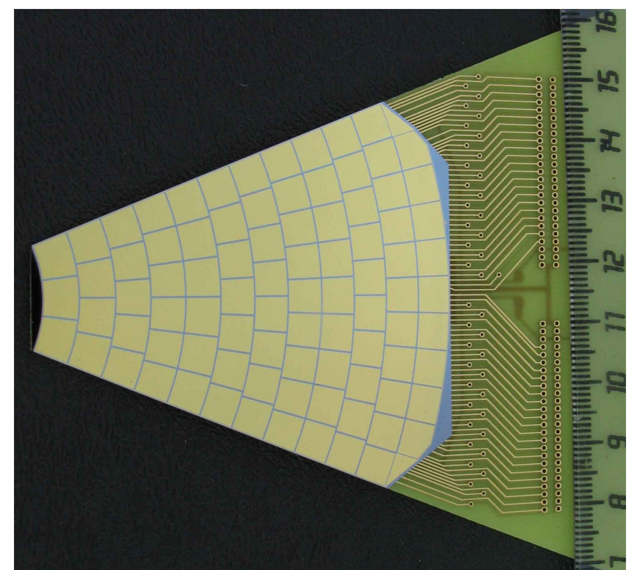
The goal is to build a new compact calorimeter infrastructure

Calorimeter infrastructure components
Sensors

LumiCal
• standard *p* in *n* Si sensors
• 300 um thick, pad pitch 1.8 mm
• Azimuthal/radial segmentation 48 sectors / 64 pads
• 40 tiles available (each 4 sectors)
• joint effort (IFJPAN, DESY, TAU)

BeamCal
• compensated GaAs sensors
• 500 um thick
• 30 sensors available
• DESY, JINR collaboration

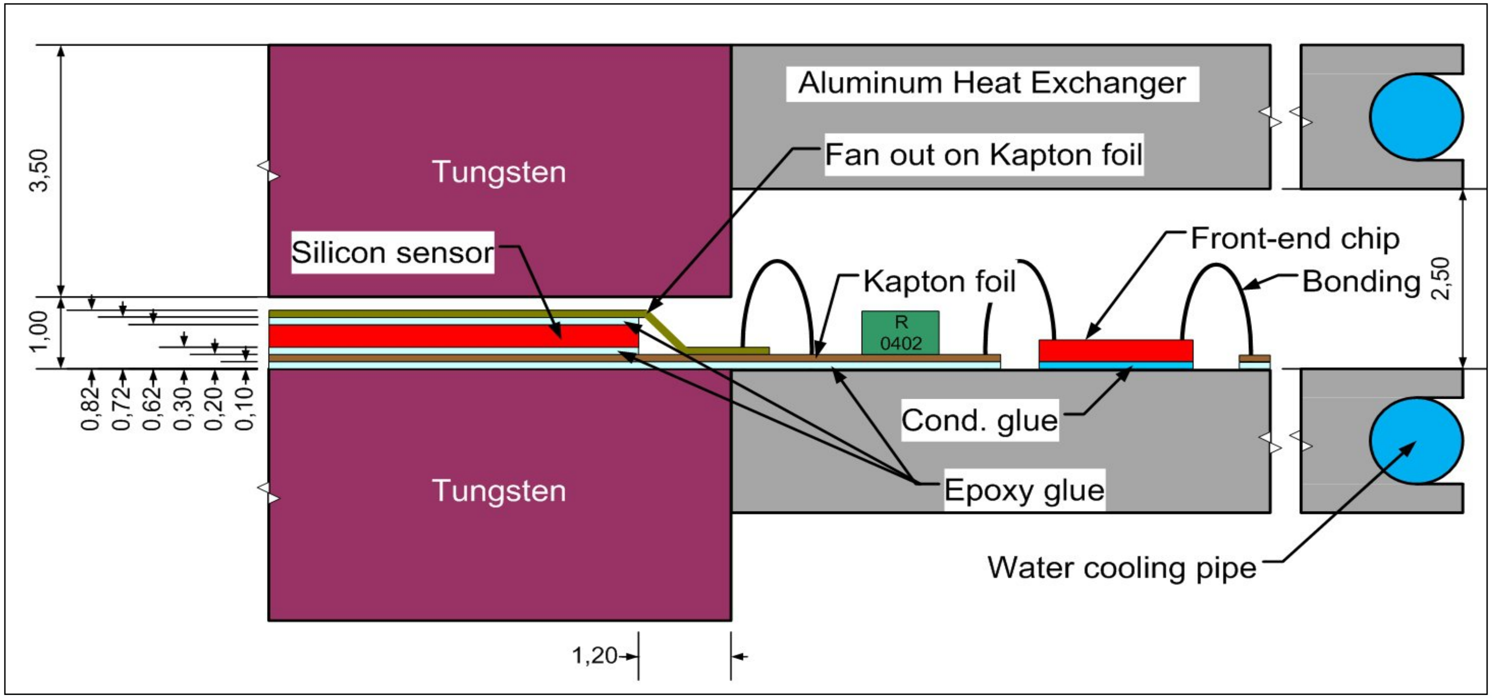




Existing sensors will be used for new infrastructure

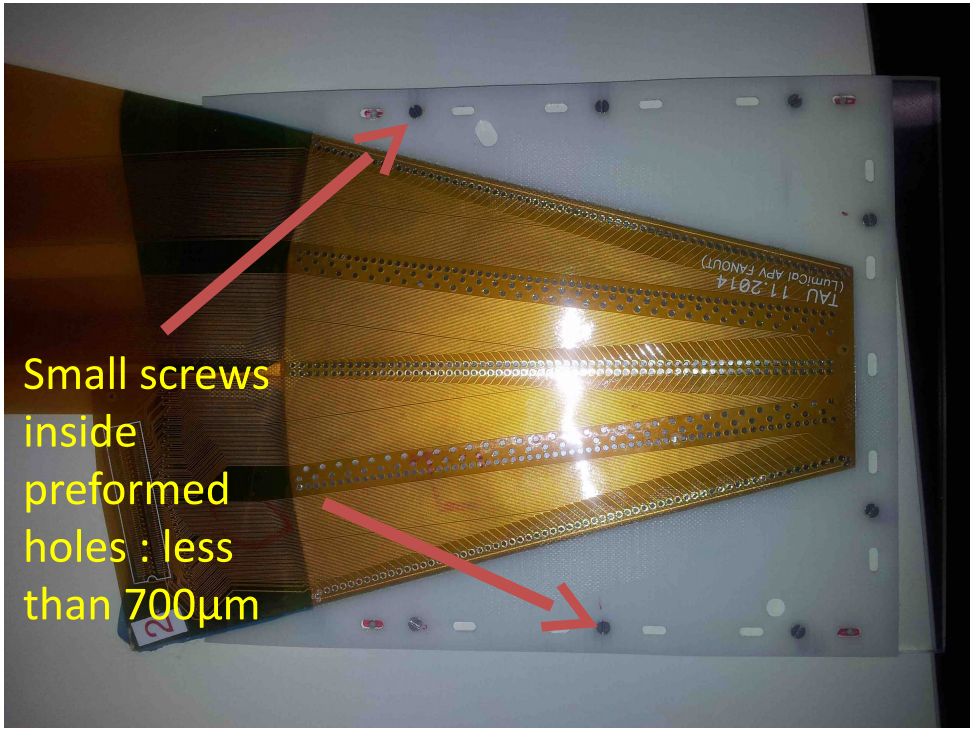
Calorimeter infrastructure components
Sensor module

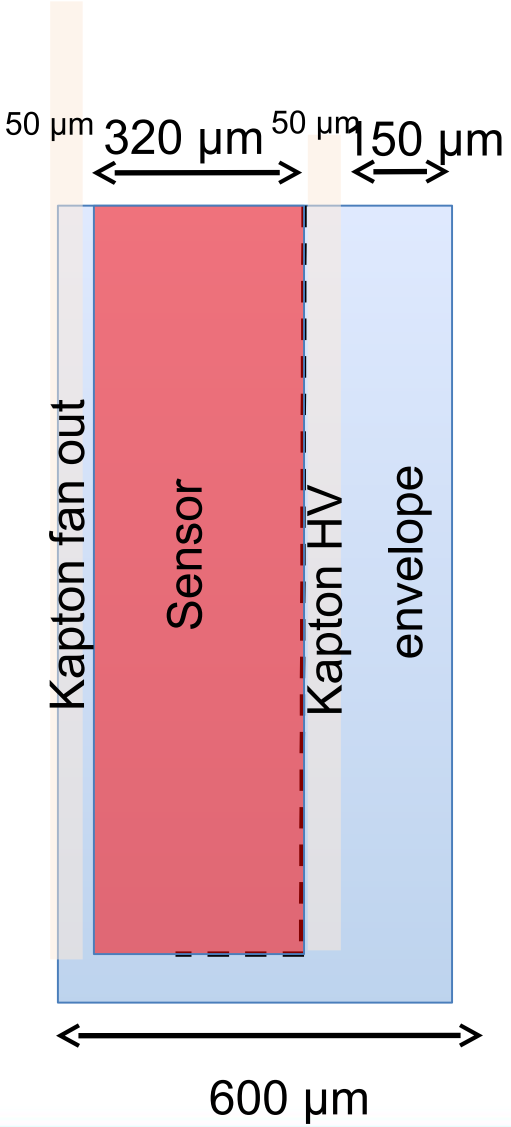
- Presently the sensor is glued to standard PCB what makes the module much too thick...
- The goal is to build a thin (< 1 mm) sensor module comprising mechanical envelope, sensor, and Kapton. TAU (with CERN) have started to work on it.



Calorimeter infrastructure components
Sensor module...

- First prototypes of thin envelope and Kapton foils have been already produced in cooperation between TAU and CERN

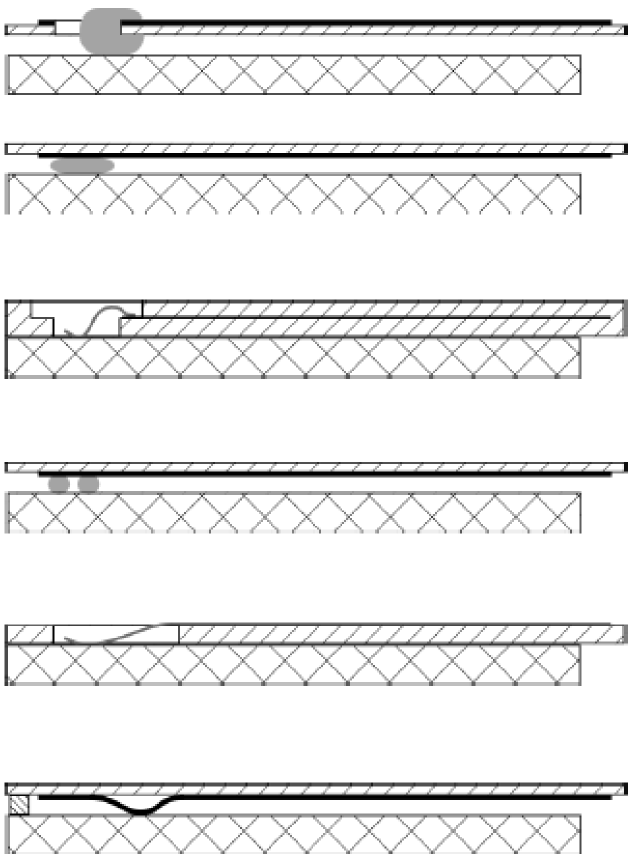


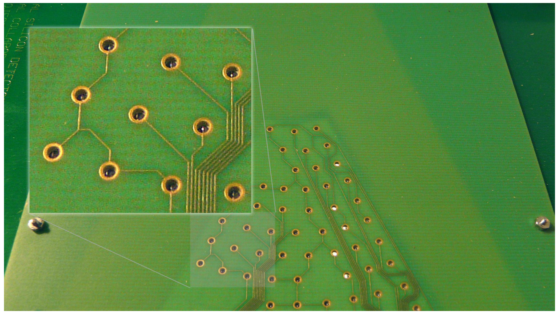


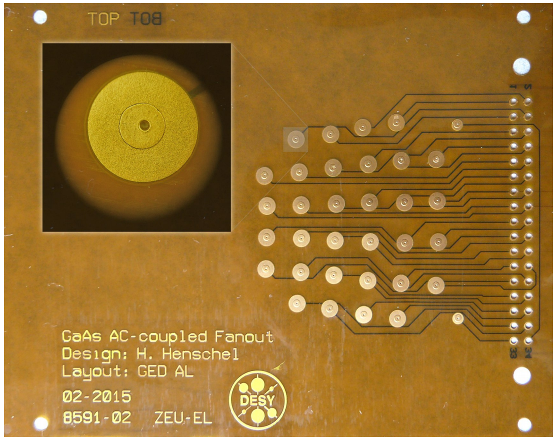
Calorimeter infrastructure components
Sensor module – connecting technologies

- Wire-bonding has various advantages but does not help in making the sensor module thin

- conductive glue
- flat loop wire bonding
- bump bonding
- tab ('tape automated') bonding
- spring loaded contact

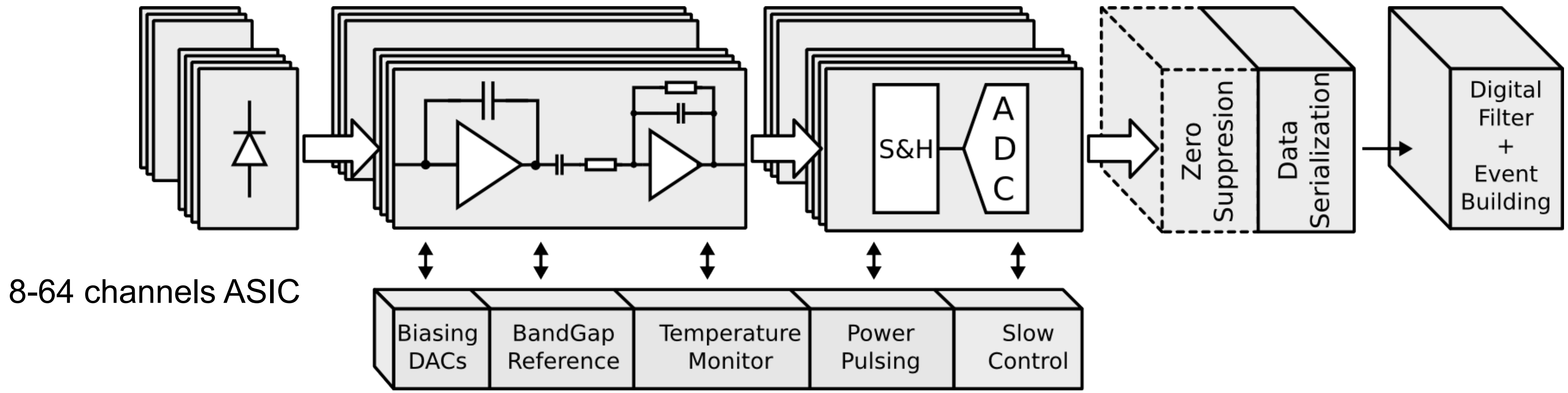






Alternative connecting technologies are studied at DESY

Calorimeter infrastructure components
Readout ASICs



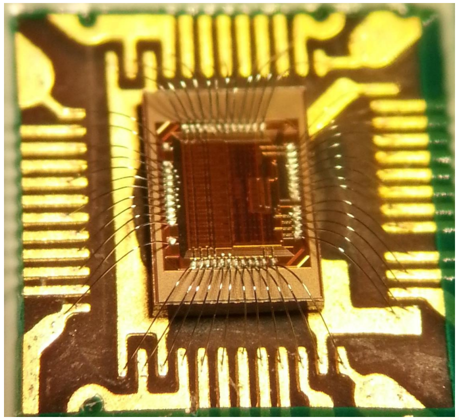
Main features/goals for new readout ASICs:

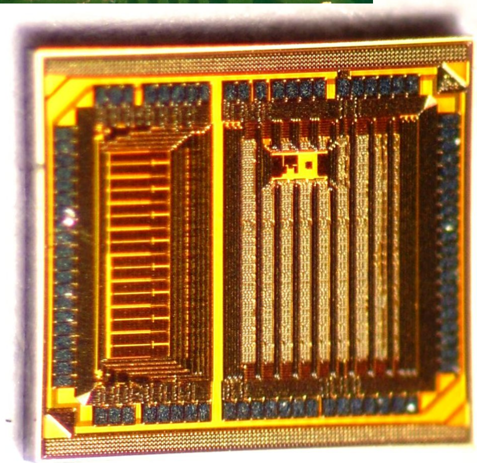
- System on Chip (SoC) type ASICs
  - New multichannel ASICs will comprise all readout functionalities to minimize number of external components – to enable construction of highly COMPACT calorimeter. The readout module should be small and <4.5mm thick (presently ~1 cm)
- Advanced CMOS technologies
  - CMOS 130 nm is used to decrease power consumption by factor of ~10 (compared to existing ASICs in AMS 0.35um) and to improve radiation hardness
  - AGH-UST has started the design...

Calorimeter infrastructure components
Readout ASICs...

Front-end ASIC features:

- 8 channels
- Cdet ≈ 5 ÷ 50pF
- 1st order shaper (Tpeak ≈ 50 ns)
- Variable gain, two modes:
  - calibration - MIP sensitivity (~4fC)
  - physics - input charge up to ~5 pC
- Power pulsing
- Power consumption
  - peak ~1.5 mW/channel
  - average < 15 uW/channel
- Developed at AGH-UST





ADC ASIC features:

- 8-channel 10-bit SAR ADC
- Max. sampling freq. ~40MSps
- Power pulsing
- Power consumption
  - peak ~1mW/channel
  - average ~10 uW/channel

ENOB ~ 9.3 bits

FOM ~50 fJ/conv.

Developed at AGH-UST

First prototypes of 8-channel front-end and 10-bit ADC ASICs were designed and fabricated within AIDA project in IBM CMOS 130 nm

We are moving to TSMC 130 nm. The front-end and ADC will be redesigned and all biasing DACs/interfaces added to eliminate use of external elements

Calorimeter infrastructure components
Readout board and back-end electronics

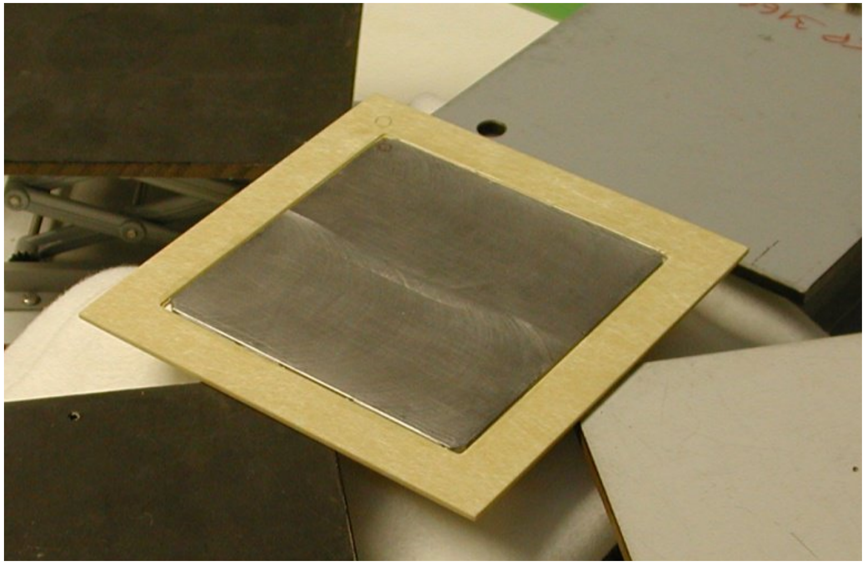
- A thin (<4.5 mm) readout board need to be built
- Readout will collect and process the digital data from the ASICs and will transmit it to an external DAQ system
- The idea is to have a FPGA chip as a core processing unit of the readout board, similarly as it was done in the existing readout
- The design has not yet started but will be done in collaboration between TAU, DESY, IFJPAN, and AGH-UST

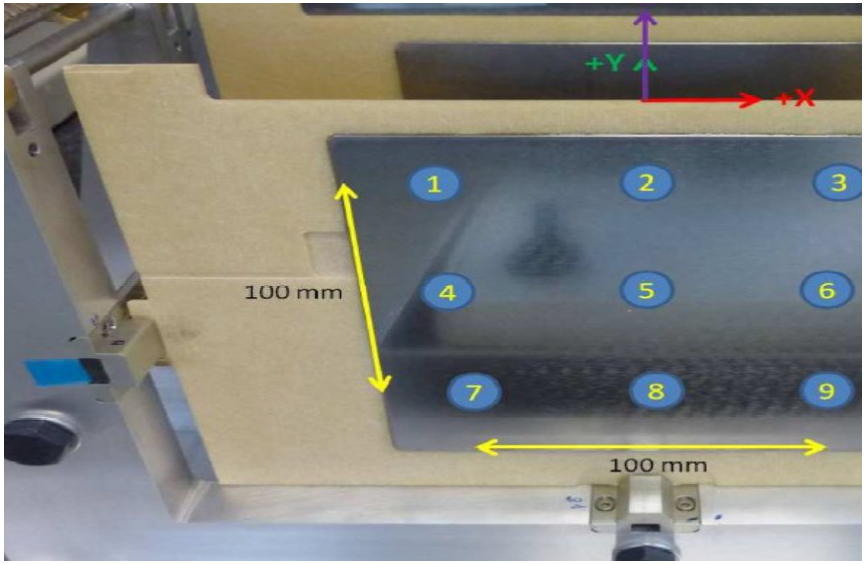
MS14.5: «Design and test of ASICs and readout board prototype for the test infrastructure» due M24.

Calorimeter infrastructure components
Absorber layers

Prototype tungsten plates

- 3.5 mm thick (one radiation length)
- Tungsten plates flatness required on front/back side - 10/50um
- 11 prototype plates produced in two companies. Four of them fulfill flatness specifications
- Joint effort CERN, AGH-UST, IFJPAN

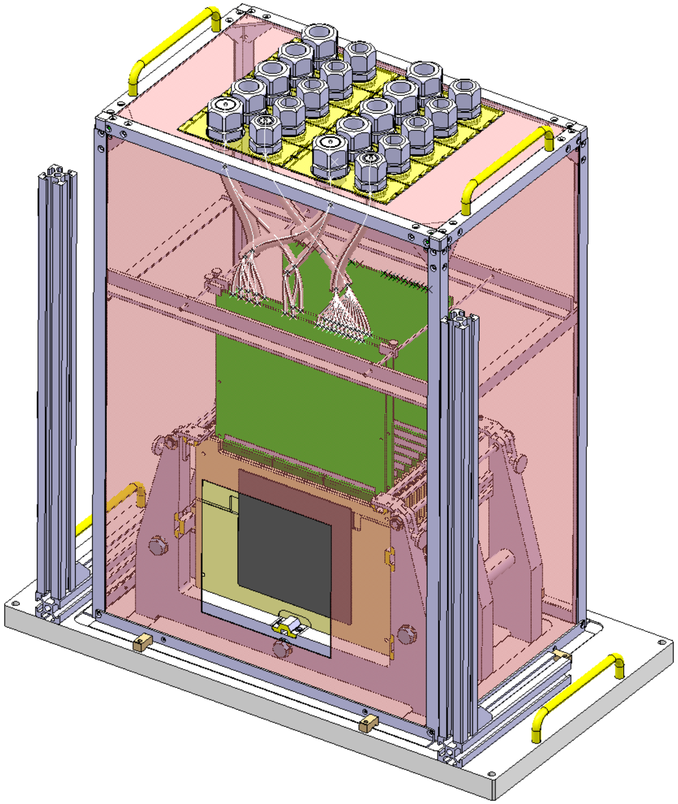


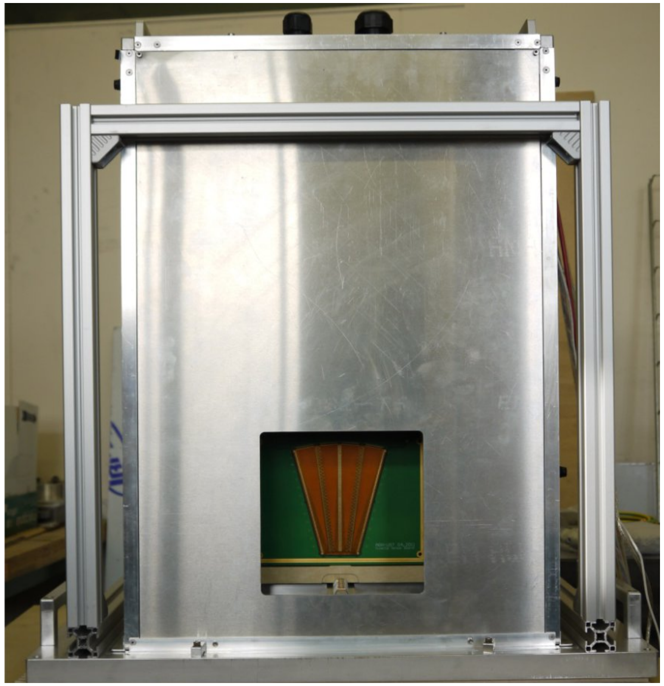


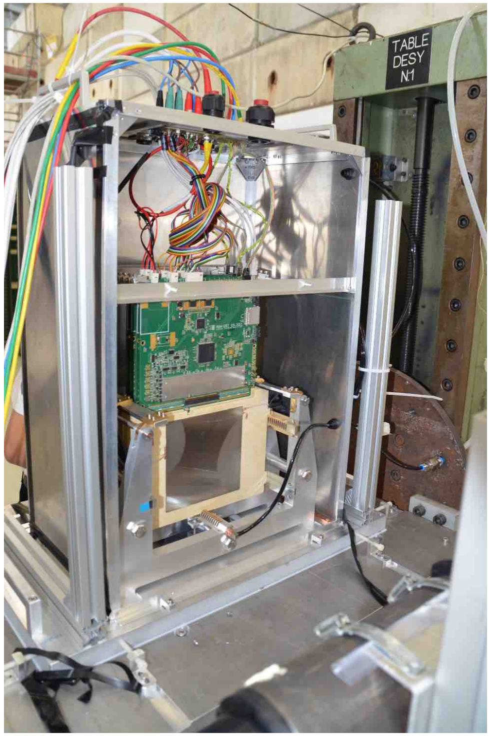
The existing tungsten plates will be used for new infrastructure. Possible DESY-JINR effort for new precise tungsten plates.

Calorimeter infrastructure components
Precise mechanical frame

- **Precise mechanical frame can hold up to 30 sensor-absorber layers**
- **Various configurations of detector modules and absorber plates are possible**
- **The frame was developed at CERN**



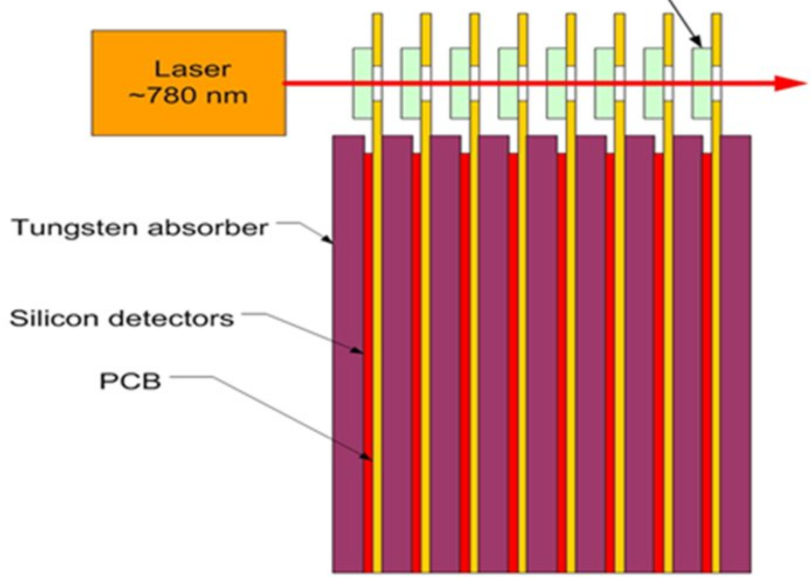




The existing frame will be used for new infrastructure

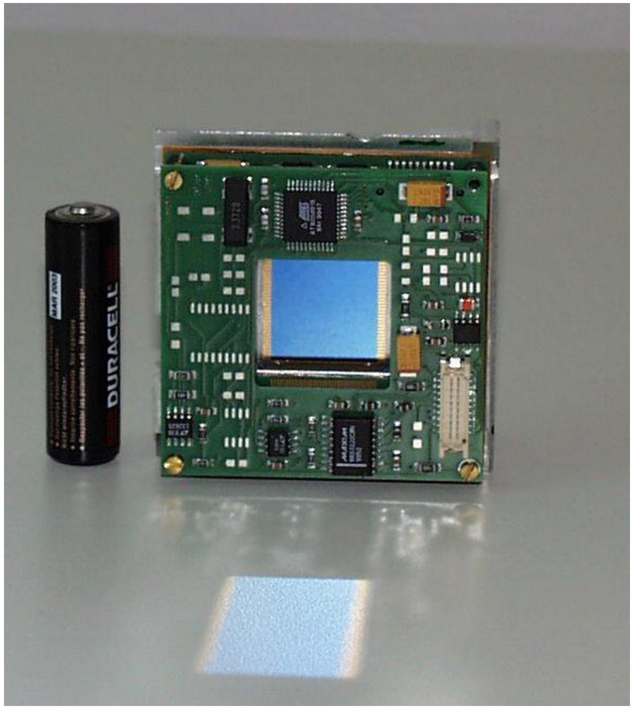
Possible addition to calorimeter infrastructure Position monitoring system

The system based on infra-red laser and semi-transparent 2D silicon sensors is studied at IFJPAN. Existing ALMY solution for CMS is the reference for this study.



Precision X, Y measurement of silicon sensors position

Prototype sensors received from MPI



ALMY sensors:

- high light transmission value ~ 80%
- simultaneously position measurements in X and Y directions
- good spatial reconstruction resolution of the laser spot (~ 1 μm)

Summary

- Infrastructure for a **compact** forward calorimeter is being developed within the AIDA-2020,
- It will use some components (sensors, tungsten plates, mechanical frame) of previously created infrastructure, developed within AIDA and EUDET,
- Main works in AIDA-2020 are focused on development of new, crucial for the compactness, components:
  - thin (<1 mm) sensor module,
  - readout ASICs,
  - thin (<4.5 mm) readout board,

and their integration into the new calorimeter infrastructure, to be used as test-beam equipment

Deliverables & Milestones

Milestone number	Milestone	Related WPs	Est. date	Means of verification	Del. date
MS14.3	Assembly and QA chain demonstration for highly granular silicon calorimeters	14.3.1	M12	2-3 operational layers produced	31/05/16
MS14.4	Design specifications of test stations for irradiated silicon sensors and LHC oriented front-end electronics	14.3.1	M12	Report to StCom	31/05/16
MS14.5	Design and test of ASICs and readout board prototype for the test infrastructure	14.3.2	M24	ASICs date sheet and readout board prototype	31/05/17

Deliverable (number)	Deliverable name *(short description of deliverable)*	WP	Lead Participant	Type	Del. Month	Delivery Date
D14.3	Advanced Assembly chain for Si calorimeters *(prototypes assembly and technical documentation of process)*	14.3.1	CNRS	DEM	M36	31/05/18
D14.4	Very compact calorimeters *(infrastructure description and test results)*	14.3.2	AGH-UST	DEM	M48	31/05/19
D14.5	Common running of calorimeter prototypes *(technologies embedding Central DAQ standards from WP5 and performance results)*	14.2.1	DESY	DEM	M36	31/05/18