WP4: microelectronics and interconnections

- WP Coordinators: Christophe de la Taille, Valerio Re

- Goal : provide chips and interconnections to detectors developed by other WPs

- Task 1: Scientific coordination (CNRS-OMEGA, INFN-UNIBG)
- Task 2 : 65 nm chips for trackers (CERN)
  - Fine pitch, low power, advanced digital processing
- Task 3 : SiGe 130nm for calorimeters/gaseous (IN2P3)
  - Highly integrated charge and time measurement
- Task 4 : interconnections between 65 nm chips and pixel sensors (INFN)
  - TSVs in 65 nm CMOS wafers, bonding of 65 nm chips to sensors, exploration of fine pitch bonding processes

- **Task 4.2 65 nm microelectronics**

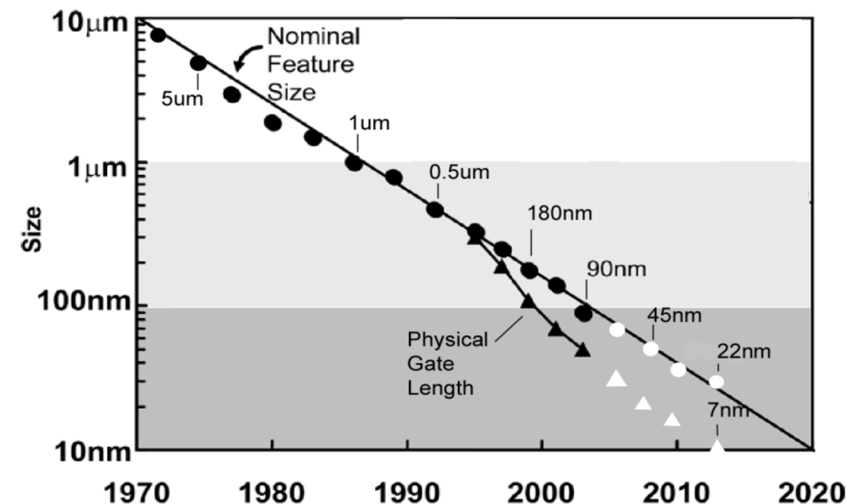
(CERN, IPASCR, CNRS-CPPM, CNRS-OMEGA, INFN-MI, INFN-PV, INFN-TO, UBONN, AGH-UST)

- Deliver CLICPIX and ATLAS/CMS pixel chips for WP6 and WP7
- Deliver full wafers for the interconnection Task 4.4
- Share expertise on TSMC 65 nm CMOS selected by CERN for HEP
- Coordinate developments with CERN RD53 international R&D program on micro-electronics for pixels

Low Power 65 nm CMOS

- Mature technology:
  - Available since ~2007
- High density and low power
  - High density vital for smaller pixels and increased data buffering during bunch trains
  - Low power tech critical to maintain acceptable power for higher pixel density and much higher data rates
- Long term availability
  - Strong technology node used extensively for industrial/automotive
- Significantly increased density, speed, and complexity compared to previous generations!

- **Access: CERN frame-contract with TSMC and IMEC**
  Design tool set, Shared MPW runs, Libraries, Design exchange within HEP community



The **Low Power (LP)** flavor **(V_{DD} = 1.2 V)** is less aggressive than other variants of the process (thicker gate oxide, smaller gate current, higher voltage), and more attractive for mixed-signal chips where analog performance is an essential

Task 4.2 65 nm chips and wafers

Coordination : CERN

- The main goal of this task is to accomplish the design and organise the fabrication of 65 nm CMOS chips for the readout of silicon pixel sensors that will be made available by WP6 and WP7.
- 65 nm CMOS generation as a baseline technology for detector readout integrated circuits in various applications at HL-LHC upgrades and CLIC, with extreme requirements in terms of data rates, radiation levels and pixel size
- This task plans to design and fabricate a chip according to the ATLAS/CMS HL-LHC upgrade requirements, and a chip tailored to the CLIC vertex detector specifications. The goal is to fabricate these chips in an engineering run, which will provide full wafers for testing and interconnection with sensors in Task 4.4.
- The designers' network will also comprise activities that are related to 65nm CMOS circuit blocks for other HEP experiments and detectors (calorimetry in ILC and CMS, particle tracking in LHCb, etc.).

RD53 engineering run

- RD53 has the scope of developing a pixel readout chip for the extreme data rates and radiation levels of the Phase II upgrades of ATLAS and CMS
- RD53 is planning to submit a “full size” prototype chip in 2016 with > 1 cm^2 area
- This will be also be “the chip for AIDA-2020 WP4” (at least the first version of it)
- The chip will be fabricated in a full engineering run (≈1 MEuro) or in an MLM run (≈0.7 MEuro) paid by RD53 institutions (many are also part of AIDA-2020)
- Possible cost sharing with other projects (MPA,…)?
- 65 nm chips for pixels in photon science will also be developed by groups involved in AIDA-2020; possible synergies (both technical and financial) could be exploited (based also on AIDA experience)

WP4.3 : SiGe 130 nm microelectronics

(CNRS-IPNL, CNRS-OMEGA, DESY, AGH-UST)

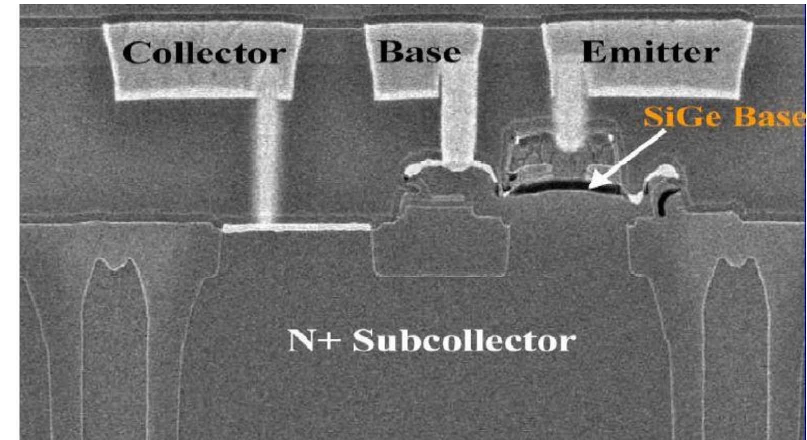
Coordination: CNRS-OMEGA

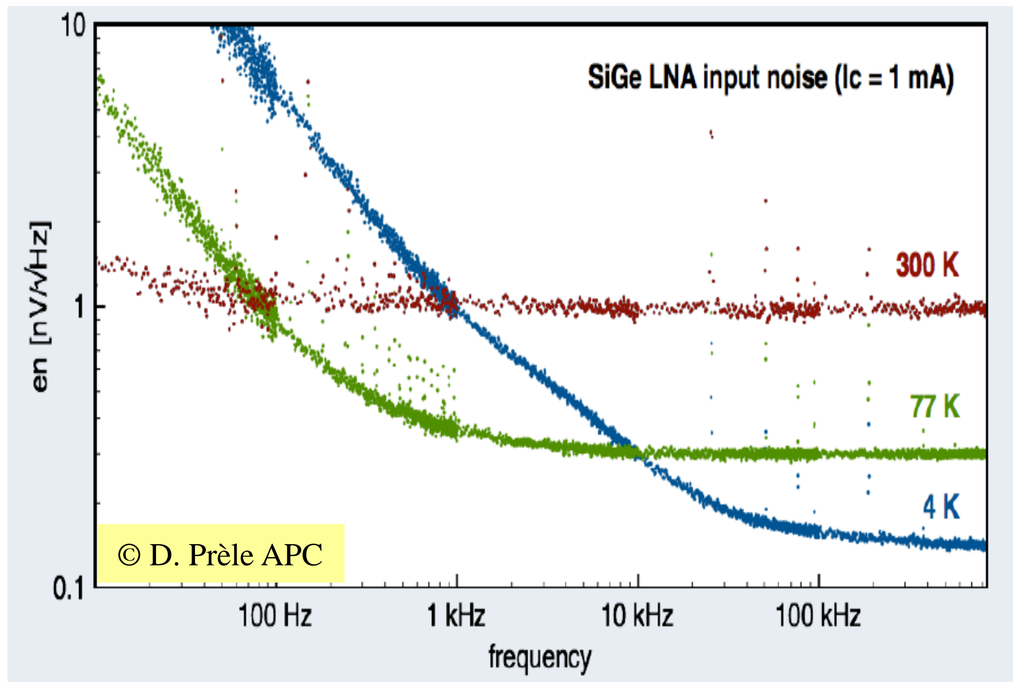
- Select best SiGe 130/180 nm process for high speed/high dynamic range ASIC design to upgrade current SiGe 350 nm AMS process
- Deliver SPIROC3 SiPM readout for calorimeter readout of WP14
- Deliver RPC high timing readout chip for WP13
- Share expertise within SiGe HEP community
- Study for LHC run 2, ILC…

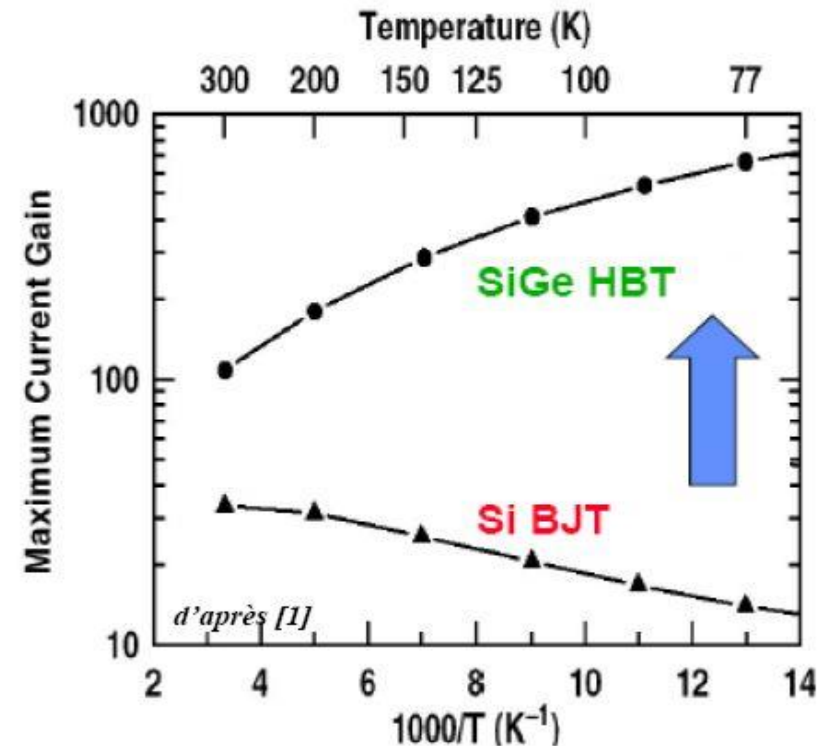
SiGe technology

Ωmega

- Faster bipolar transistors for RF telecom
  - Better mobility and FT
  - Better current gain (beta)
  - Better Early voltage
  - Interesting improvement at low T
  - Very low 1/f nosie
  - Compact CMOS (0.25 or 0.35µm) for mixed-signal design



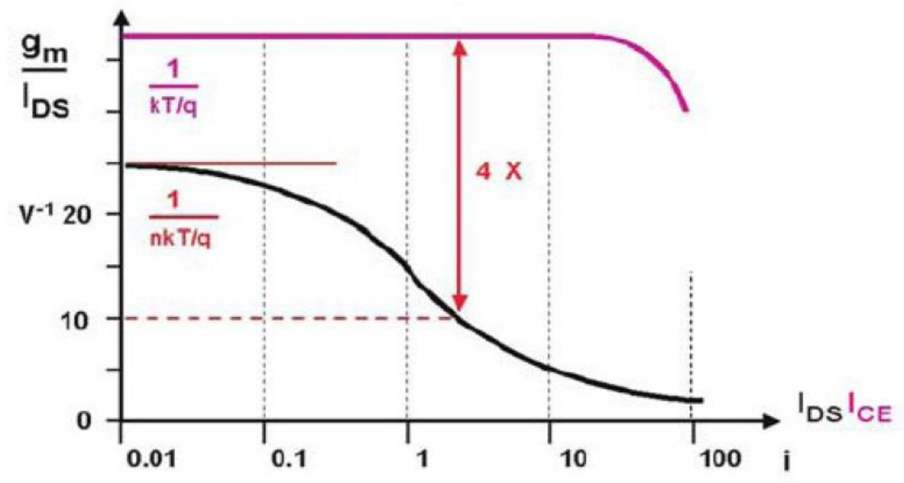


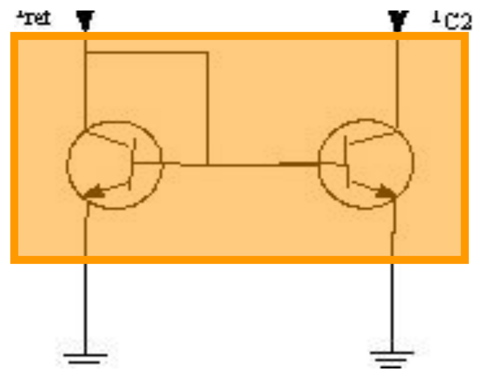


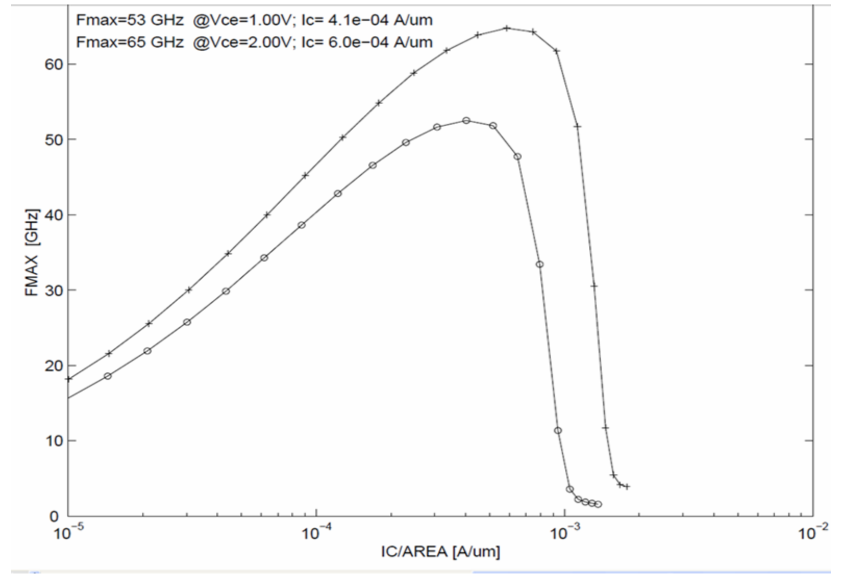
Power and speed with SiGe

Ωmega

- BJT : best g_m /I ratio (1/U_T)
  - Large transconductance with small devices
- Speed goes as $F_T = g_m / 2\pi C$
  - C~10 fF g_m typ mA/V
  - F_T ~60 GHz for SiGe 0.35µm
  - Interesting for fast preamps
- Not forgetting 100V Early voltage and matching performance (A~mV*µm)
- $V_{BE}=V_T Ln(I_C/I_S)$
- Large swing : V_{CEsat} ~3 U_T







RF and HPA Applications and Technology

Front-End Modules

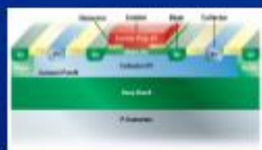
RF SOI and SiGe Power Amplifiers

- Power Amplifiers
- Antenna Switch
- PA Controllers

mmWave

High Performance SiGe

- Optical Fiber Networks
- Automotive Radar
- 60 GHz WiFi, Backhaul MW
- Light Peak and Thunderbolt



High Performance Analog

Complementary BiCMOS

- Line Drivers DSL, HomePlug, ATE
- HDD PreAmp
- OpAmps, DAC, ADC

RF and Tuners

RF CMOS and SiGe BiCMOS

- Cell Phones, WiFi TxRx
- Basestation, Specialty Wireless
- TV, Satellite, STB Tuners

Best-in-class SiGe, RF CMOS, RF models and Design Enablement

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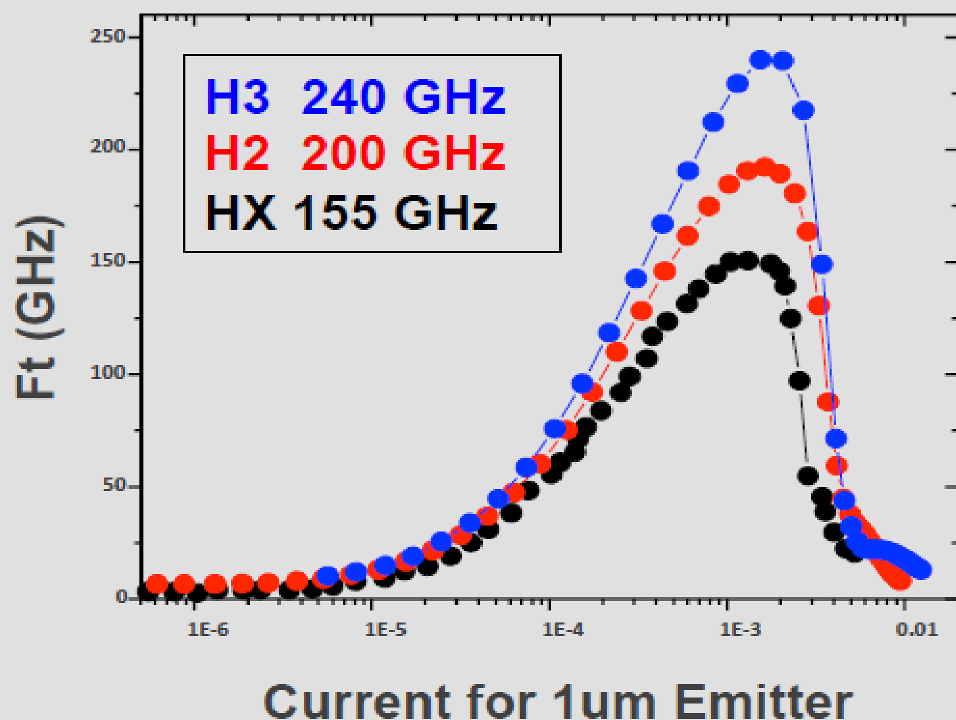
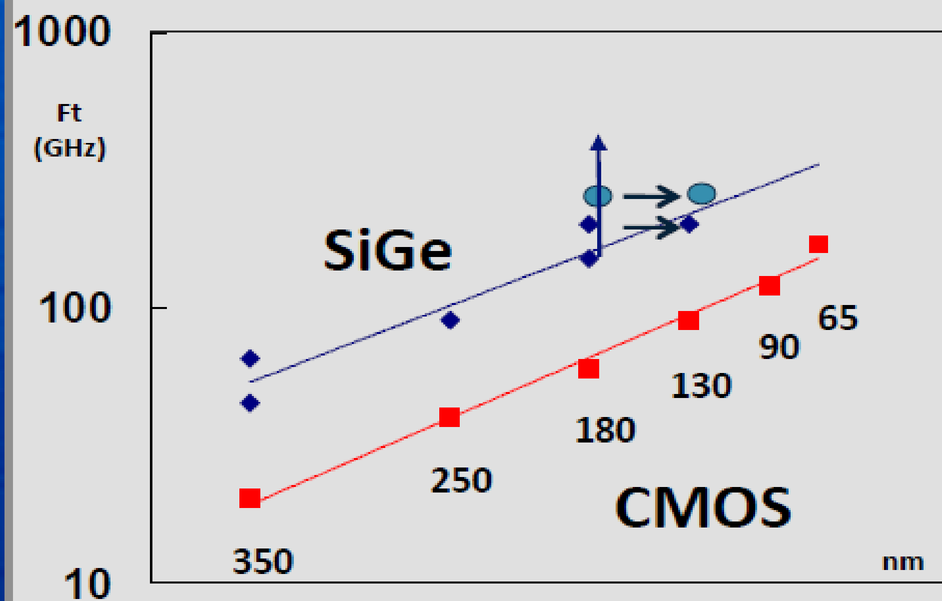
High Performance SiGe





NEW

- **SBC18H3:** PDK for 0.13um version (SBC13)
- **SBC18H4:** 1st successful Shuttle (11 customers)
- **SBC18H5:** Target for >400 GHz Fmax

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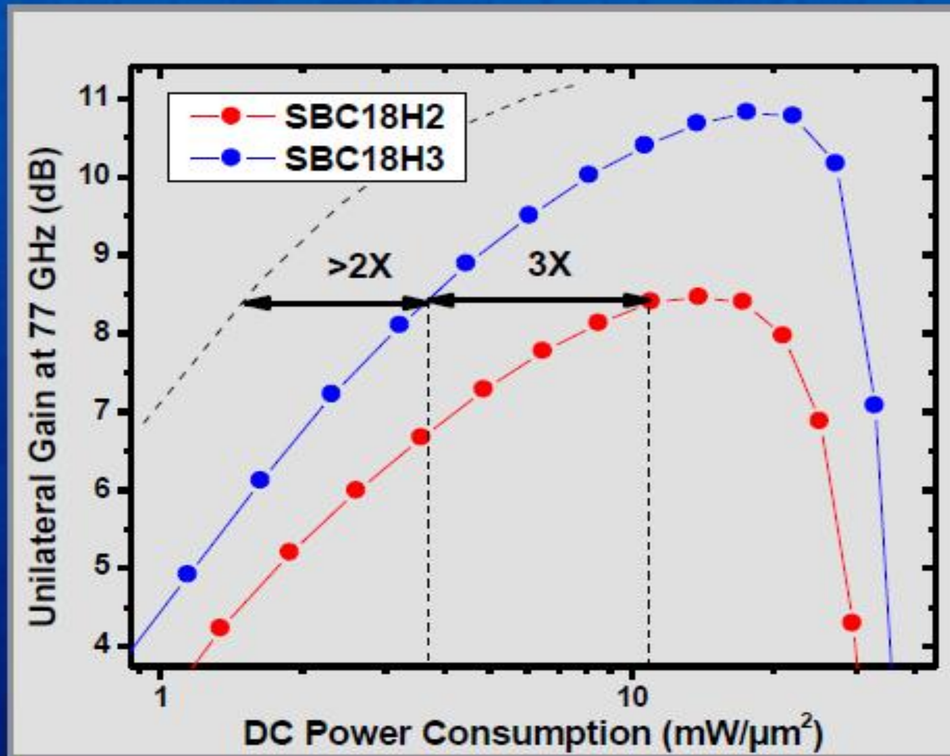
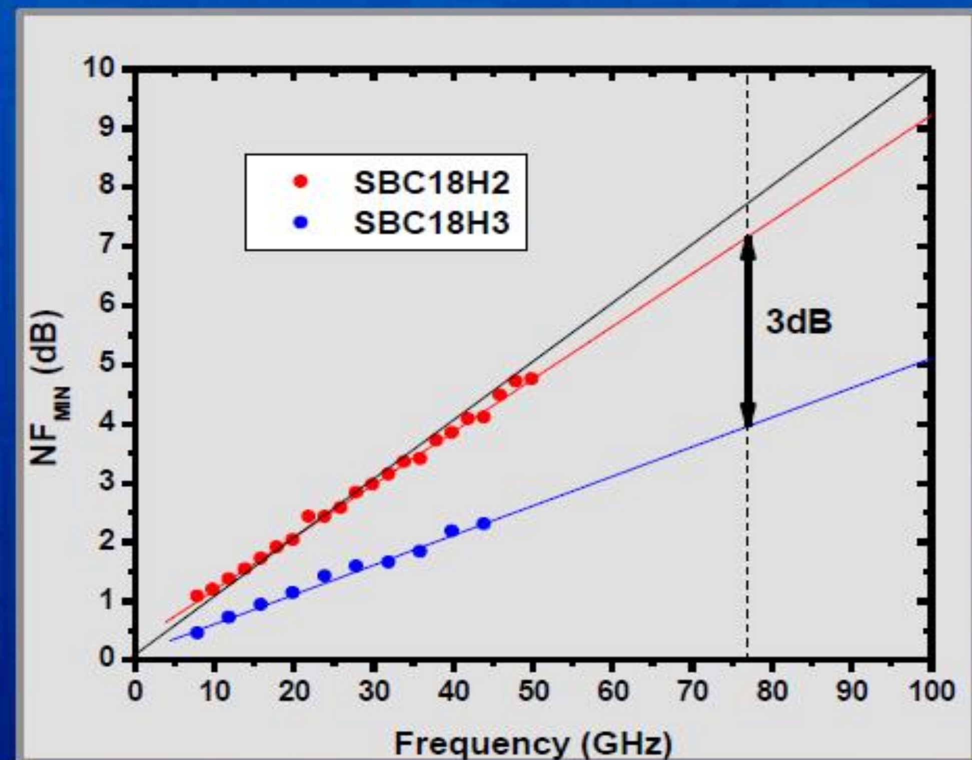
SBC18H3



Ft = 240 GHz, Fmax = 280 GHz



Minimum Noise Figure of 2 dB at 40 GHz

Best in Class SiGe Speed/Power

Best in Class Noise

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0.13um RF CMOS and SiGe BiCMOS

	TS13	TSBL13	SBL13	SBC13	
1.0 V CMOS	Option	No	No	No	
1.2 V CMOS	Yes	Yes	Yes	Yes	
2.5 V CMOS	Option	No	No	No	
3.3 V CMOS	Yes	Yes	Yes	Yes	
Vt Options	Std/Low/Hi	Std/Low/Hi	Std/Low/Hi	Std/Low/Hi	
SiGe NPN Ft	No	90/67/37	90/67/37	200/75	GHz
SiGe NPN BVceo	No	2.4/3.5/6.0	2.4/3.5/6.0	2/3.5	GHz
Triple Well	Option	Option	Option	Option	GHz
Native FET	Option	Option	Option	Option	
MIM Cap	1,1.5, 2	2	2.8, 5.6	2.8, 5.6	fF/um2
Poly Resistor	256/320/1K	310/1K	310/1K	310/1K	ohm/sq
Metal Layers	6, 7, 8	6, 7	6	6	
Metal Material	Cu	Cu	Al	Al	
Top Metal (um)	3.3 or 3.3 / 3.3	3.3	3	3	um

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Task 4.4 Interconnections and TSVs

(CERN, INFN-GE, INFN-PV, INFN-PG, CNRS-CPPM, CNRS-LAL, MPG-MPP, UBONN, UNIGLA)

- Produce through-silicon vias on wafers from Task 4.2
- Connect chips with TSVs to detectors from WP7
- Test radiation hardness of interconnections

Task 4.4 Interconnections and TSVs

Coordination: INFN

- Interconnection of the 65 nm CMOS readout chips developed by Task 4.2 to the silicon pixel sensors provided by WP6 and WP7.
- Connection to the backside of the 65 nm chips by through-silicon vias (TSVs) across the substrate of 300 mm CMOS wafers
- This task takes advantage of activities and results that were previously achieved by the FP7 AIDA project. Participants in AIDA WP3 explored diverse flavours of 3D integration. The goal is to exploit this experience, and to apply it to more advanced pixel detector systems using the new generation of 65 nm CMOS front-end integrated circuits
- Possible synergies with imaging applications (based on previous AIDA experience)

Bonding and TSV technologies

- Industrial bonding techniques have to be qualified, so that requirements of future HEP experiments can be addressed in terms of pixel readout cell pitch and geometry and of interconnection density.
- Qualify processes with the potential of achieving a bonding pitch of the order of 20 μm, sizeably smaller as compared to existing pixel devices where bump bonding of 50 μm pitch has been used.
- Etching TSV in fully processed 65 nm CMOS wafers for peripheral backside interconnections: the baseline TSV technology will be "via last"
- Desirable to explore processes for relatively fine pitch TSVs in thinned CMOS wafers, which will also include chip backside processing steps.
- The network will be open to evaluate other alternatives, e.g. "via middle" TSVs etched in the CMOS wafers before the fabrication of the metal interconnections.
- Depending on the requirements from WP6, selected bonding and TSV technologies may be also applied to wafers with High-Voltage CMOS pixel sensors.

Task 4.4 stages

1) Select the technologies that can be reliably adopted to achieve TSVs in 65 nm readout chips and their bonding to pixel sensors.

2) Define design rules for bonding pads and for TSVs in CMOS chips together with Task 4.2.

3) after the fabrication of the 65 nm engineering run, TSVs will be processed in selected CMOS wafers. Bonding with sensors will be performed using both chips without TSVs and with TSVs.

4) chip-sensor assemblies will be fully qualified, checking their electrical performance and studying their radiation hardness properties at the extreme levels foreseen by the innermost tracking layers of future experiments.

AIDA WP4 funding

Task 4.2: 349 kEuro

Task 4.3: 285 kEuro

Task 4.4: 337 kEuro

The accomplishment of the WP4 goals relies on funds that participating institutions are willing to spend using money from other projects

For the 65 nm ATLAS/CMS chip, this is already handled in the frame of RD53

AIDA WP4 budget

Beneficiary short name* (all costs in €)	Institute/Lab	Task	Task Leader*	Person - months	Monthly personnel costs	Personnel direct costs*	Travel direct costs	Equipment and consumables	Other direct costs*	Sub-contracting cost	Material direct costs	Total direct costs	Total indirect costs*	Total costs (direct +indirect)	EC requested funding	
CNRS	OMEGA	4,1	Yes	4,00	8.191,17	32.764,68	4.000,00	0,00	0,00	0,00	4.000,00	36.764,68	9.191,17	45.955,85	8.000,00	
INFN	BG	4,1	Yes	0,00	0,00	0,00	0,00	0,00	0,00	0,00	0,00	0,00	0,00	0,00	8.000,00	
CERN		4,2	Yes	11,00	7.300,00	80.300,00	2.000,00	90.000,00	0,00	0,00	92.000,00	172.300,00	43.075,00	215.375,00	85.000,00	
INFN	PAVIA	4,2	No	4,00	5.800,00	23.200,00	2.000,00	34.000,00	0,00	0,00	36.000,00	59.200,00	14.800,00	74.000,00	28.000,00	
INFN	TORINO	4,2	No	4,00	5.800,00	23.200,00	2.000,00	34.000,00	0,00	0,00	36.000,00	59.200,00	14.800,00	74.000,00	28.000,00	
INFN	MILANO	4,2	No	4,00	5.800,00	23.200,00	2.000,00	34.000,00	0,00	0,00	36.000,00	59.200,00	14.800,00	74.000,00	28.000,00	
CNRS	CPPM	4,2	No	10,00	8.191,17	81.911,70	2.000,00	4.000,00	0,00	0,00	6.000,00	87.911,70	21.977,93	109.889,63	40.000,00	
CNRS	OMEGA	4,2	No	8,00	8.191,17	65.529,36	2.000,00	5.000,00	0,00	0,00	7.000,00	72.529,36	18.132,34	90.661,70	20.000,00	
AGH-UST	AGH-Krakow	4,2	No	10,00	3.000,00	30.000,00	2.000,00	10.000,00	0,00	0,00	12.000,00	42.000,00	10.500,00	52.500,00	30.000,00	
IPASCR		4,2	No	14,00	2.400,00	33.600,00	2.000,00	0,00	0,00	0,00	2.000,00	35.600,00	8.900,00	44.500,00	20.000,00	
UBONN		4,2	No	10,00	6.000,00	60.000,00	2.000,00	78.000,00	0,00	0,00	80.000,00	140.000,00	35.000,00	175.000,00	70.000,00	
CNRS	OMEGA	4,3	Yes	30,00	8.191,17	245.735,10	10.000,00	5.000,00	0,00	0,00	15.000,00	260.735,10	65.183,78	325.918,88	150.000,00	
CNRS	IPNL	4,3	No	12,00	8.191,17	98.294,04	2.000,00	2.000,00	0,00	0,00	4.000,00	102.294,04	25.573,51	127.867,55	55.000,00	
AGH-UST	AGH-Krakow	4,3	No	14,00	3.000,00	42.000,00	2.000,00	10.000,00	0,00	0,00	12.000,00	54.000,00	13.500,00	67.500,00	40.000,00	
DESY	DESY1	4,3	No	10,00	5.500,00	55.000,00	5.000,00	42.000,00	0,00	0,00	47.000,00	102.000,00	25.500,00	127.500,00	30.000,00	
DESY	Heidelberg	4,3	No	0,00	0,00	0,00	0,00	0	0,00	0,00	0,00	0,00	0,00	0,00	10.000,00	associate partner
INFN	PAVIA	4,4	Yes	20,00	5.800,00	116.000,00	10.000,00	150.000,00	0,00	0,00	160.000,00	276.000,00	69.000,00	345.000,00	135.000,00	
INFN	GENOVA	4,4	Yes	4,00	5.800,00	23.200,00	2.000,00	24.000,00	0,00	0,00	26.000,00	49.200,00	12.300,00	61.500,00	22.000,00	
INFN	PERUGIA	4,4	Yes	4,00	5.800,00	23.200,00	2.000,00	24.000,00	0,00	0,00	26.000,00	49.200,00	12.300,00	61.500,00	22.000,00	
CNRS	CPPM	4,4	No	7,00	8.191,17	57.338,19	2.000,00	2.000,00	0,00	0,00	4.000,00	61.338,19	15.334,55	76.672,74	22.000,00	
CNRS	LAL	4,4	No	8,00	8.191,17	65.529,36	2.000,00	2.000,00	0,00	0,00	4.000,00	69.529,36	17.382,34	86.911,70	22.000,00	
UBONN		4,4	No	4,00	6.000,00	24.000,00	2.000,00	24.000,00	0,00	0,00	26.000,00	50.000,00	12.500,00	62.500,00	22.000,00	
CERN	Uppsala	4,4	No	0,00	0,00	0,00	0,00	0,00	0,00	0,00	0,00	0,00	0,00	0,00	30.000,00	associate partner
UNIGLA		4,4	No	6,00	6.000,00	36.000,00	2.000,00	42.000,00	0,00	0,00	44.000,00	80.000,00	20.000,00	100.000,00	40.000,00	
MPG-MPP		4,4	No	4,00	5.500,00	22.000,00	2.000,00	24.000,00	0,00	0,00	26.000,00	48.000,00	12.000,00	60.000,00	22.000,00	
						0,00					0,00	0,00	0,00	0,00		
						0,00					0,00	0,00	0,00	0,00		
						0,00					0,00	0,00	0,00	0,00		
						0,00					0,00	0,00	0,00	0,00		
Totals:				**202,00**		**1.262.002,43**	**65.000,00**	**640.000,00**	**0,00**	**0,00**	**705.000,00**	**1.967.002,43**	**491.750,61**	**2.458.753,04**	**987.000,00**	

AIDA WP4 deliverables

- D4.1 CMOS 65 nm engineering run *(availability of the run with the "ATLAS/CMS" and CLICPIX pixel chips)* (CERN)

  M36 (April 30, 2018)

- D4.2 BICMOS SiGe engineering run *(availability of run with SiPM calorimeter-WP14 and gas detectors-WP13 chips)* (CNRS)

  M36 (April 30, 2018)

- D4.3 Through Silicon Vias production *(fabrication of TSV in wafers of deliverable 4.1)* (INFN)

  M42 (October 31, 2018)

AIDA WP4 milestones

MS4.1	Architectural review of deliverable chips in 65nm run	M14 (June 2016)
MS4.2	Final design review of 65nm	M30 (October 2017)
MS4.3	Test report of deliverable D4.1	M46 (February 2019)
MS4.4	Selection of SiGe foundry	M14
MS4.5	Final design review of deliverable chips in SiGe run	M30
MS4.6	Test report of deliverable D4.2	M46
MS4.7	Selection of TSV process	M14
MS4.8	Final design review of deliverable D4.3	M30
MS4.9	Test report of deliverable D4.3	M46