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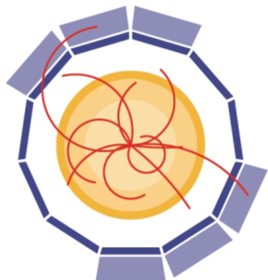
Bonn: 65 nm CMOS and interconnections

WP 4 Session

Fabian Hügging on behalf of
U Bonn Group



AIDA 2020

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RD53 Working Groups & Bonn participation

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WG	Domain
WG1	Radiation test/qualification: M. Barbero, CPPM
	Coordinate test and qualification of 65nm for 1Grad TID and10^{16} neu/cm^2 Radiation tests and reports. Transistor simulation models after radiation degradation Expertise on radiation effects in 65nm
WG2	Top level: (M. Garcia-sciveres, LBNL)
	Design Methodology/tools for large complex pixel chip Integration of analog in large digital design Design and verification methodology for very large chips. Design methodology for low power design/synthesis. Clock distribution and optimization.
WG3	Simulation/verification framework: T. Hemperek, Bonn — coordinated by Bonn
	System Verilog simulation and Verification framework Optimization of global architecture/pixel regions/pixel cells
WG4	I/O : To be started — Bonn participation
	Development of rad hard IO cells (and standard cells if required) Standardized interfaces: Control, Readout, etc.
WG5	Analog design / analog front-end: V. Re, Bergamo/Pavia
	Define detailed requirements to analog front-end and digitization Evaluate different analog design approaches for very high radiation environment. Develop analog front-ends
WG6	IP blocks: (J. Christiansen, CERN) — Bonn participation
	Definition of required building blocks: RAM, PLL, references , ADC, DAC, power conversion, LDO, , Distribute design work among institutes Implementation, test, verification, documentation

WG3 – Simulation Test Bench

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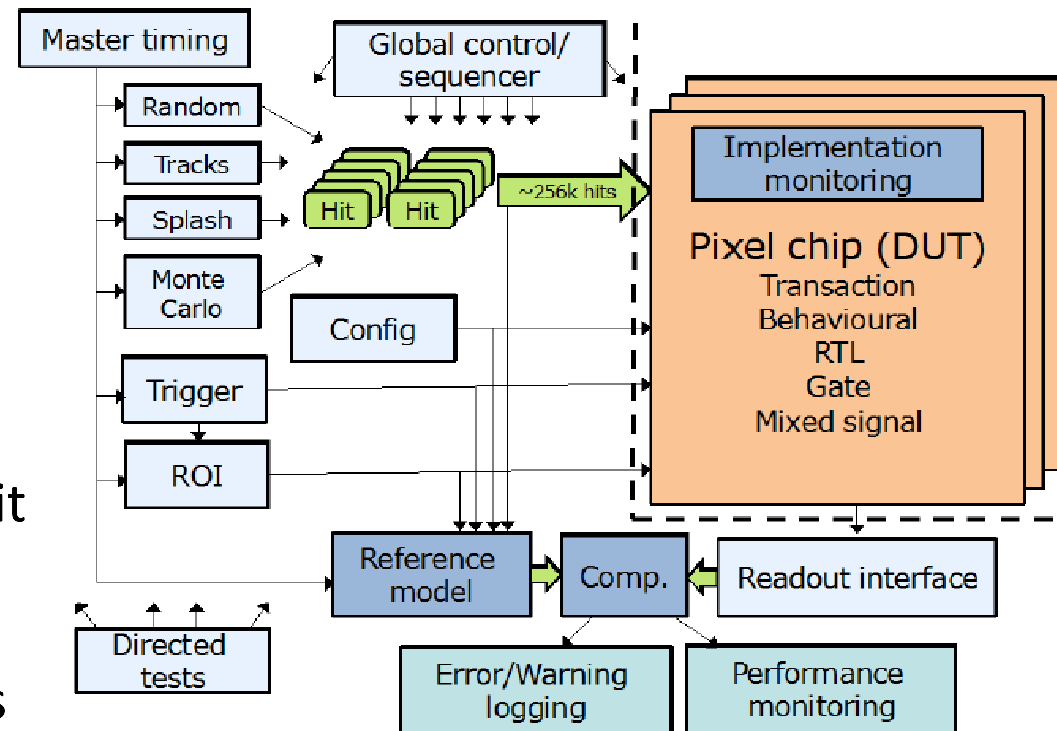
- Convener: **T. Hemperek, Bonn**
- Verification framework customized for complex pixel chips based on system Verilog and UVM (industry standard for ASIC design and verification)
- High abstraction level down to detailed gate/transistor level
- Benchmarked using FEI4 design
- Internal generation of appropriate hit patterns
- Integration with ROOT to import hits from detector simulations and for analyzing results.



WG4 – I/O & IP Development

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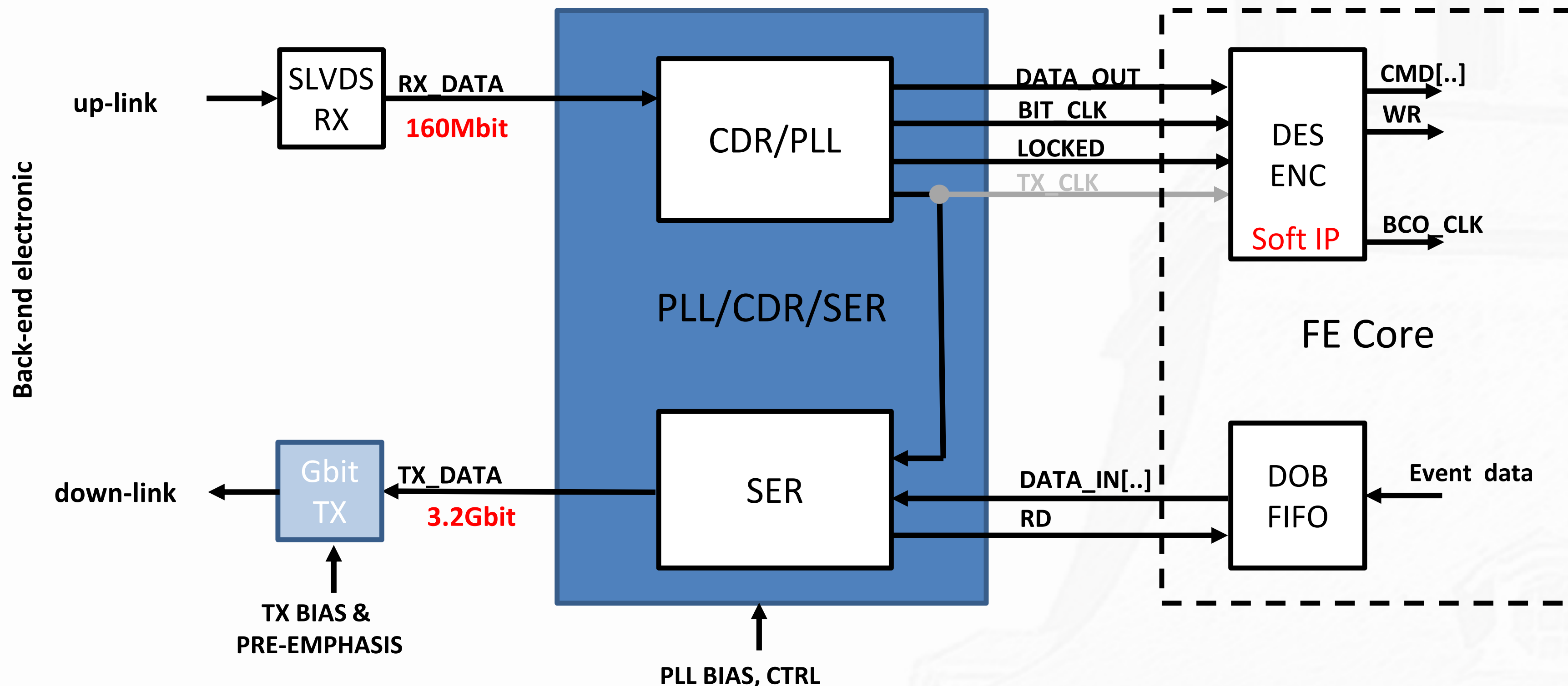
- FE interface
  - One up-link, combining CLK and CMD → needs clock/data recovery (CDR)
  - One (or more) high speed (> 2Gbps) down-links → serializer (SER) and Gbit driver (TX)
  - Bit rates and encoding schemes currently under discussion



WG6 – IP Blocks

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- Ambitious plan to design and maintain a broad variety of full custom blocks in a common IP/design repository
  - Definition of specifications
  - Integration into the design flow
- Time line
  - Prototyping/test of IP blocks: 2014/2015
  - IP blocks ready 2015/2016

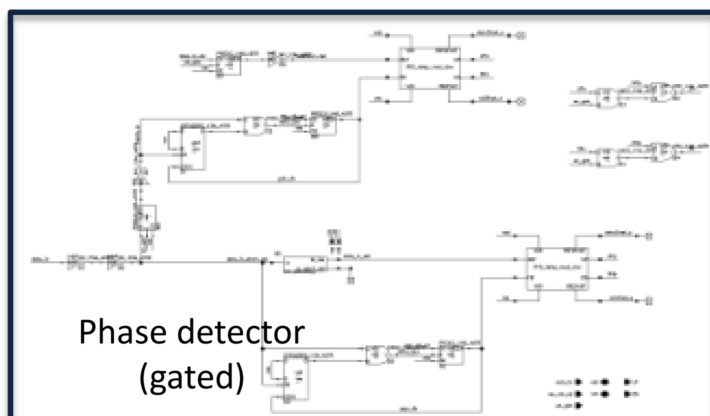
- **Bonn Contributions**
  - Organization of PLL / CDR / SER development
  - Participation in the Gbit link driver design
  - Linear regulator / shunt regulator (M. Karagounis, former Bonn group member now FH Hamm-Lipstadt)
  - Various digital IP (soft cores)

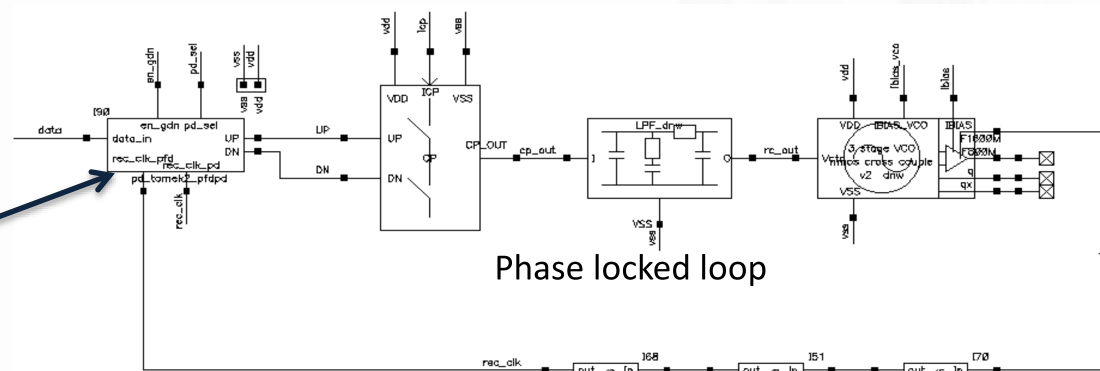
Country	DE		FR	NL	IT - INFN						US	FR	UK	US	CZ
Group	Bonn	CERN	CPPM	NIKHEF	Bari	Pav/Berg	(Milano)	Padova	Pisa	Torino	LBNL	LPNHE	RAL	Santa Cruz	(Prague)
ANALOG: Coordination with analog WG															
Temperature sensor.			O			(P)				(P)					(P)
Radiation sensor			(P)			(P)				O ?					(P)
HV leakage current sensor.			O							(P)					(P)
Band gap reference		O	O	(P)		O							(P)		
Self-biased Rail to Rail analog buffer	(P)		(P)	(P)									O		(P)
MIXED															
8 – 12 bit biasing DAC		(P)			O										(P)
10 - 12 bit slow ADC for monitoring		O	O		O										
PLL for clock multiplication	O	(P)		(P)				(P)	(P)	(P)			(P)	(P)	
High speed serializer (~Gbit/s)	O	(P)		(P)					(P)				(P)	(P)	
(Voltage controlled Oscillator)				(P)				O	(P)	(P)					
Clock recovery and jiter filter	O	(P)							(P)				(P)		
Programmable delay	O	(P)							(P)				(P)		
DIGITAL															
SRAM for pixel region	(P)	(P)					O							(P)	
SRAM/FIFO for EOC.	(P)	(P)					(P)		(P)					O	
EPROM/EFUSE	(P)	O	(P)												
DICE storage cell / config reg	(P)		O				(P)		(P)					(P)	
LP Clock driver/receiver	(P)					O							(P)		
(Dedicated rad hard digital library)	(P)	(P)	(P)						O			(P)	(P)		
(compact mini digital library for pixels)	(P)	(P)	(P)						O			(P)	(P)		
IO: Coordination with IO WG															
Basic IO cells for radiation	(P)	O													
Low speed SLVS driver (<100MHz)	(P)	(P)				O			(P)	(P)					(P)
High speed SLVS driver (~1Gbits/s)	(P)	(P)				O			(P)	(P)					(P)
SLVS receiver	(P)	(P)				O			(P)						(P)
1Gbits/s drv/rec cable equalizer															
C4 and wire bond pads	(P)	O													
(IO pad for TSV)	O		(P)									(P)		(P)	
Analog Rail to Rail output buffer	O		(P)									(P)		(P)	
Analog input pad	O											(P)			
POWER															
LDO(s)		(P)	(P)	O					(P)	(P)			(P)		
Switched capacitor DC/DC		(P)									O				(P)
Shunt regulator for serial powering				O											
Power-on reset															
Power pads with appropriate ESD	(P)	O													
SOFT IP: Coordination with IO WG															
Control and command interface		(P)			(P)				O			(P)			
Readout interface (E-link ?)		(P)			(P)				O			(P)			

IP Design in Bonn – Clock Data Recovery

- Clock Data Recovery (CDR) – recovering clock signal from randomized data

- Implementation: Phase-locked-loop with special phase detector (gated)





Piotr Rymaszewski

- Prototype RD53 CDR/SER submission foreseen for May/June 2015

Bonn/CPPM TSV project

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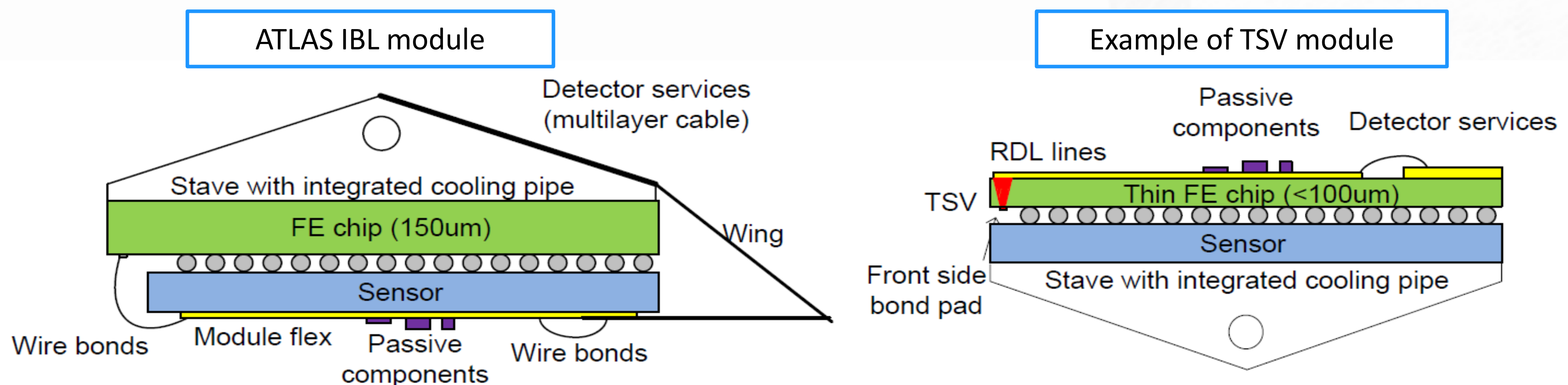
- The goal of the project is to develop modules for ATLAS pixel detector at the HL-LHC using a via last TSV process
  - Post-processing technology applicable on existing FE electronics
  - Dead area at the chip periphery can be reduced

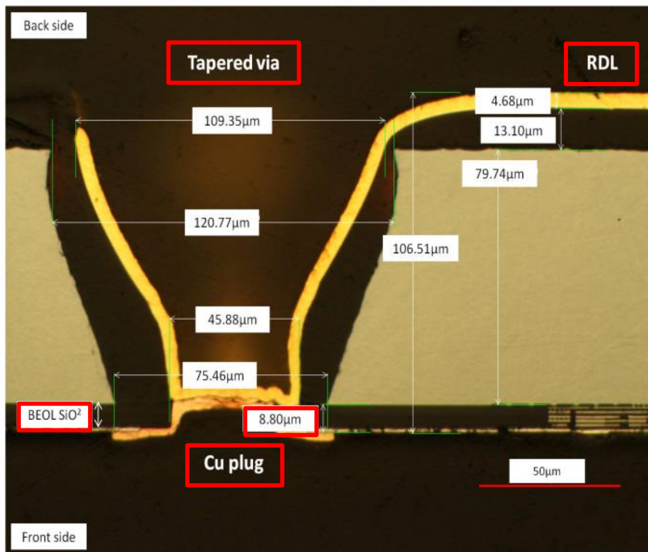
  → Compact, low mass hybrid pixel modules with minimal modification to the FE layout and using standard CMOS technology
  → no wire bonds needed if combined with new fley hybrid interconnection methods
  → Potential for 4 side abuttable modules using dedicated sensor layout

- Modules with TSV can be used for the outermost detector layers at the HL-LHC to provide full detector coverage over the large area



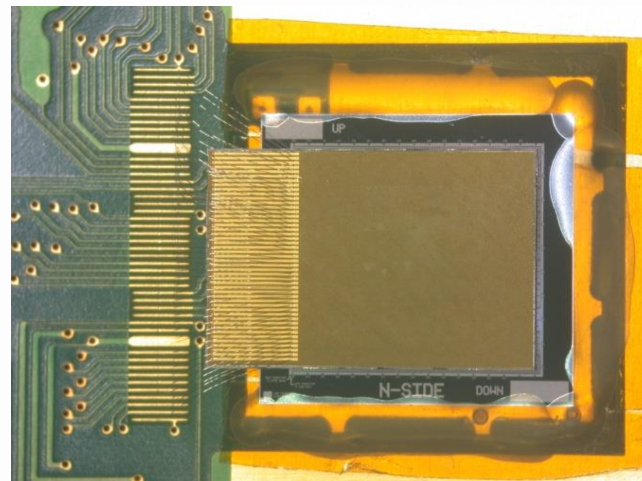
Via last TSV at IZM

- Process: IZM via last tapered TSV
- Demonstrator single chip modules built with:
  - FE-I2/3 ATLAS pixel readout chip 90µm thin, with tapered profile TSV and RDL
  - Planar n-in-n sensor
  - Standard flip chip process (no handle wafer for thin chip handling used, unconnected pixels expected along the chip perimeter)
- No loss in performance wrt modules without TSV

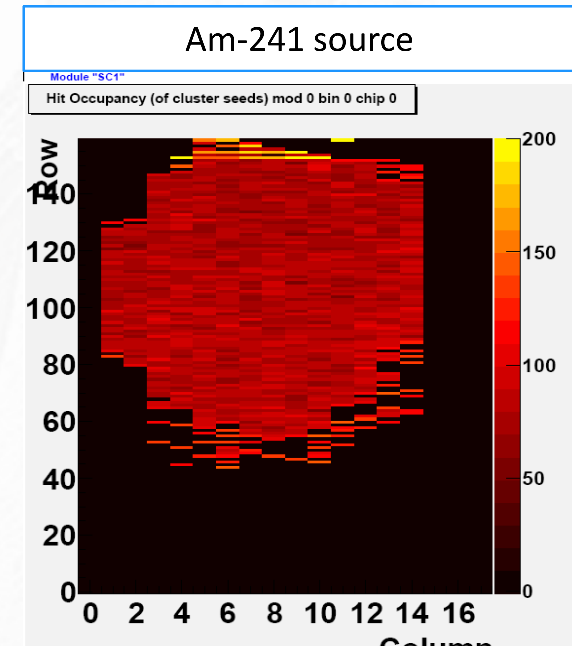


http://iopscience.iop.org/1748-0221/7/08/P08008/

Module on board

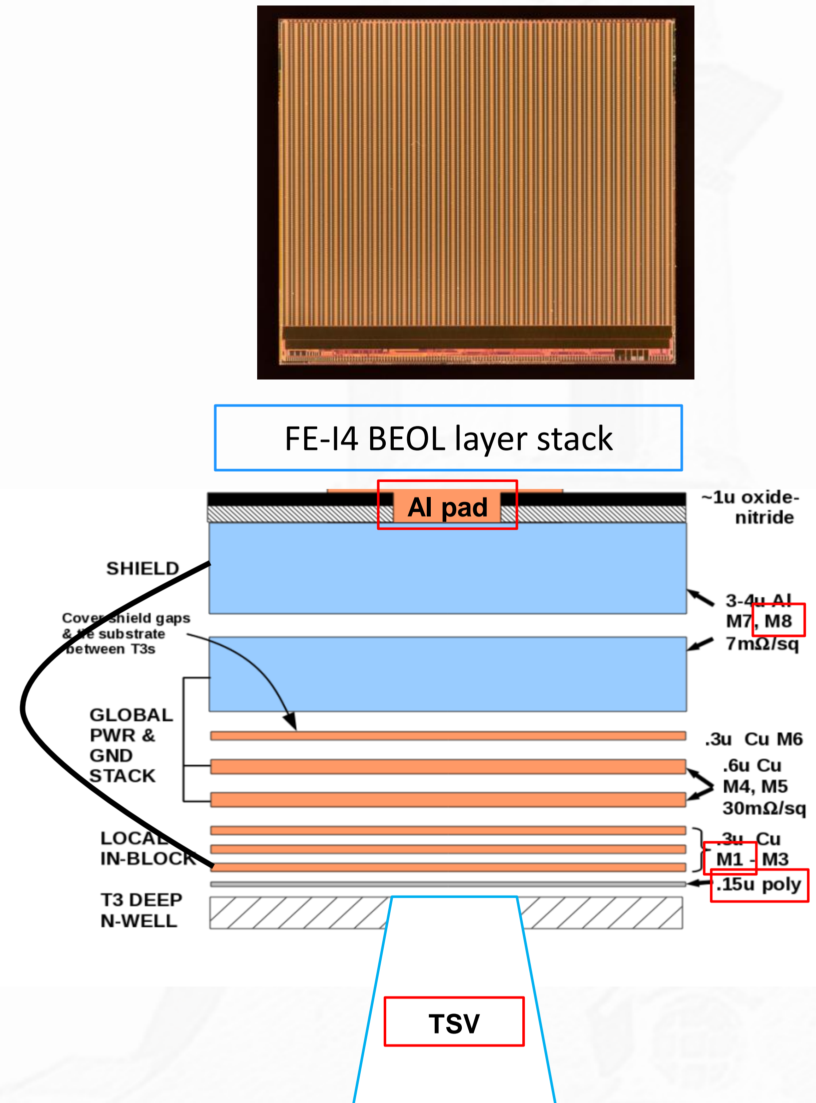


Am-241 source



Ongoing: FE-I4B modules with TSV

- Status
  - Three tested FE-I4B wafers at IZM
  - in process right now → expect 1st structures by fall 2015
- FE wafer processing
  - UBM deposition on the front side
  - FE wafer thinned to approx. 150-200µm
  - Vias etching in the peripheral IO pads, diameter of 60-80µm
  - Via passivation, and metallization
- No front side processing needed
  - Metal layers in the pad
  - M8 connected to M1
  - Between silicon and M1 thin layer of BEOL SiO2 and poly-Si → can be etched from the back side



TSV for FE-I4B w/ IZM Berlin: process flow & goals

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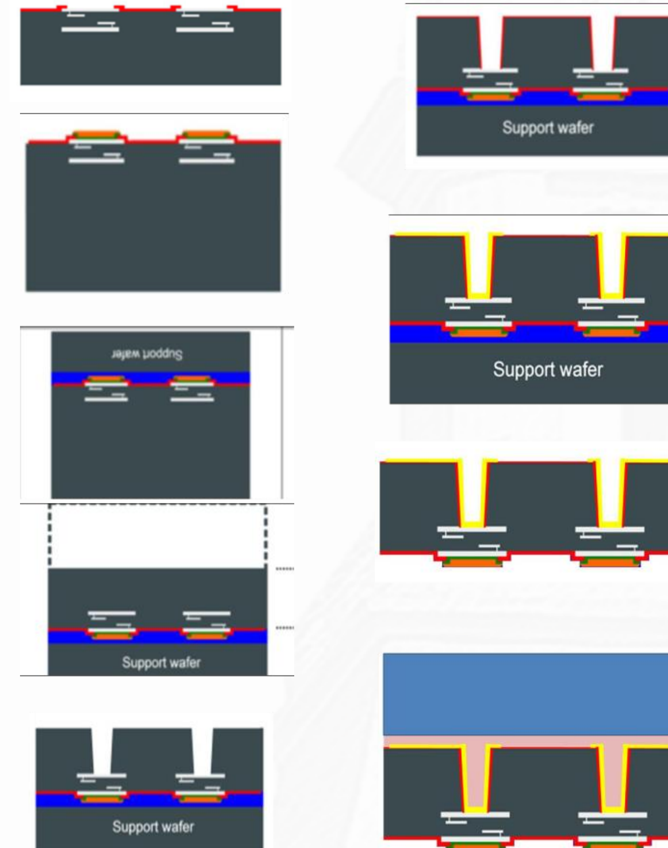
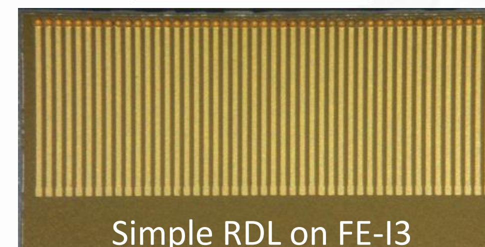
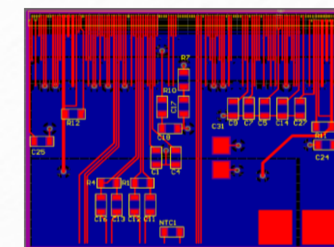
- Bump bonding of thin (<100µm) FE-I4B with TSV to sensors cannot be done without handle wafer
  - FE-I4B area = ~4cm^2 → prohibitive bending of the FE during reflow
- IZM developed a flip chip method to bump bond 150µm FE-I4 to sensors used for the entire IBL module production
  - Laser releasable polymeric bonding interface
- Method needs to be demonstrated on FE-I4 wafers with TSV and RDL
  - RDL patter on backside
  - TSVs are not completely closed

  → constraints on the polymeric glue thickness and the uniformity of the deposition







2 layer RDL on FE-I4 backside

Conclusions

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- For 65nm CMOS main Bonn contribution to WP4 is our strong participation to RD53:
  - leading of WG3 and strong participation to I/O WG and IP design WG
  - General timeline of RD53:
    - Radiation hardness conclusions – early 2015
    - Analog, I/O and IP prototype tests chips – now to end of 2015 (multiple submissions)
    - First medium size (1 x 1 cm^2) full matrix submission planned for summer 2015
    - Full or half-size prototype(s) – 2016 (wafer run order in CERN frame contract process)
    - Test, design iteration and refinements – 2017
    - Hand over to ATLAS and CMS for final chip designs – 2018
- For interconnections we continue our collaboration with IZM and CPPM for a via last TSV process on ATLAS Pixel FE wafer:
  - demonstrated with good results on FE-I2/3 assemblies
  - currently in process with FE-I4 wafers → expect results by end of 2015
  - plan to move on with 65nm CMOS wafers from RD53

BACKUP

Bonn 65nm CMOS Design Activities previous to RD53

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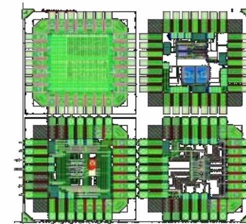
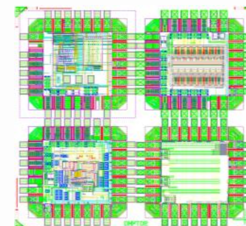
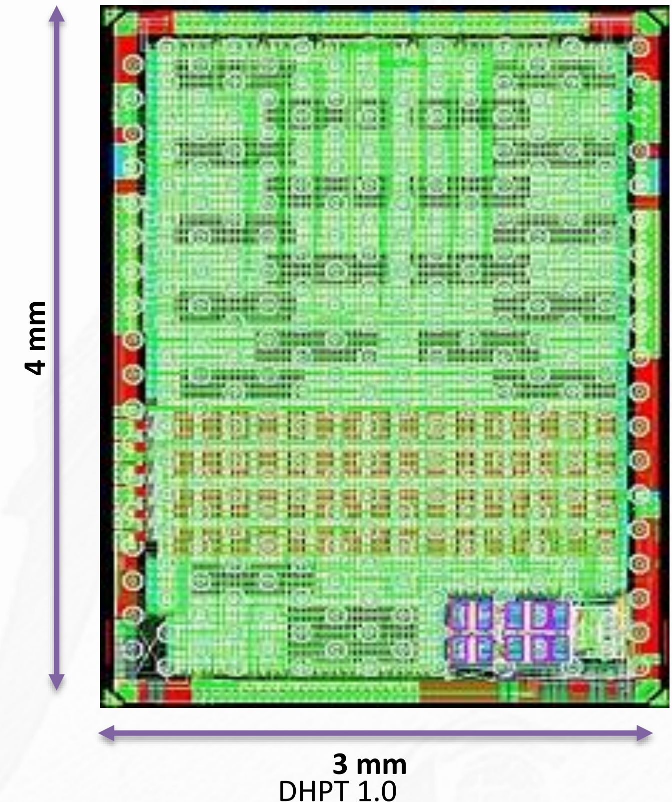
- Data handling processor (DHP) for the Belle 2 DEPFET pixel vertex detector
  - Manly digital with full-custom blocks
  - PLL (1.6 GHz)
  - High speed serial link (1.6 Gbps)
  - LVDS IO
- IP blocks for future pixel chips
  - Low power analog front-end (CSA + discr.)
  - Low power, small area ADC
  - SEU test structures
- Chip submissions
  - DHPT 0.1, four chiplets, Oct. 2011
  - DHPT 0.2, four chiplets, June 2012
  - DHPT 1.0, Oct. 2013
    - 14 mm^2 MPW
    - C4 bumps



DHPT 0.1



DHPT 0.2



DHPT 1.0

DHPT 0.2 – Pixel Analog FE Measurements

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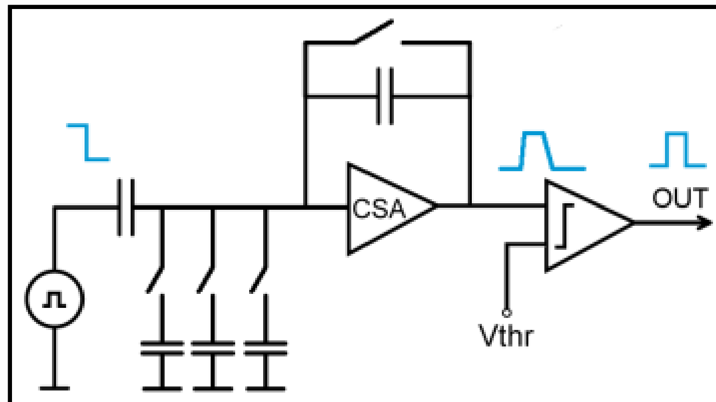
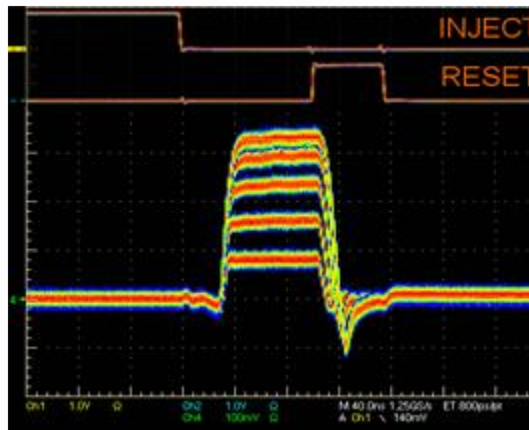
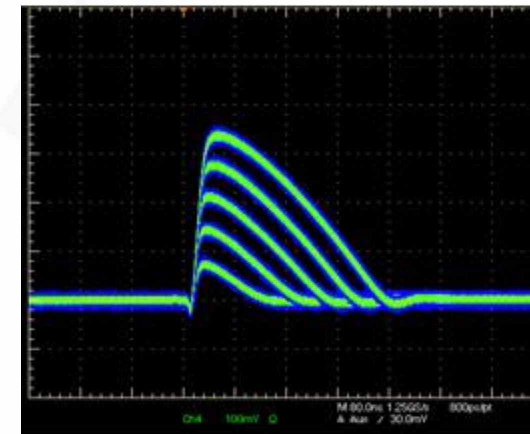


CSA with switched reset



CSA with continuous reset



CSA	Comparator	[e⁻]	P [µW]
Continuous	Continuous	144	10.4
	Dynamic	183	10.6
Switched	Continuous	113	14.6
	Dynamic	157	14.8

DHPT 0.1 – PLL & High Speed Link Driver

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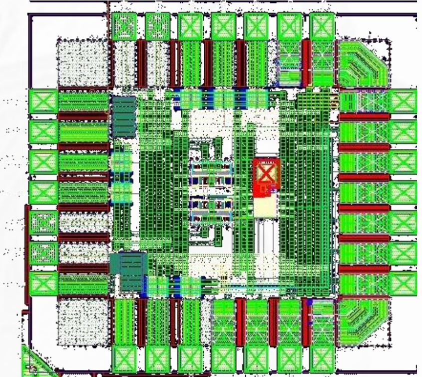
- 1.6 GHz PLL, 80 MHz input clock
- Pseudo random bit sequence generator (8 bit LFSR) for bit error rate tests
- Current mode logic (CML) driver
- Programmable pre-emphasis (first order FIR filter)
  - Needed to compensate the high frequency attenuation of the data cable



PLL_CML Test Chip,
T. Kishishita

320 MHz
CML driver
TXO_P
TXO_N
320 MHz
800 MHz
1.6 GHz
80 MHz
PLL
LFSR
50 Ω
50 Ω
CML driver
TX1_P
TX1_N
pre drv.
I_0
I_1
del
2
dt
a
b

Gbit Link Test Setup

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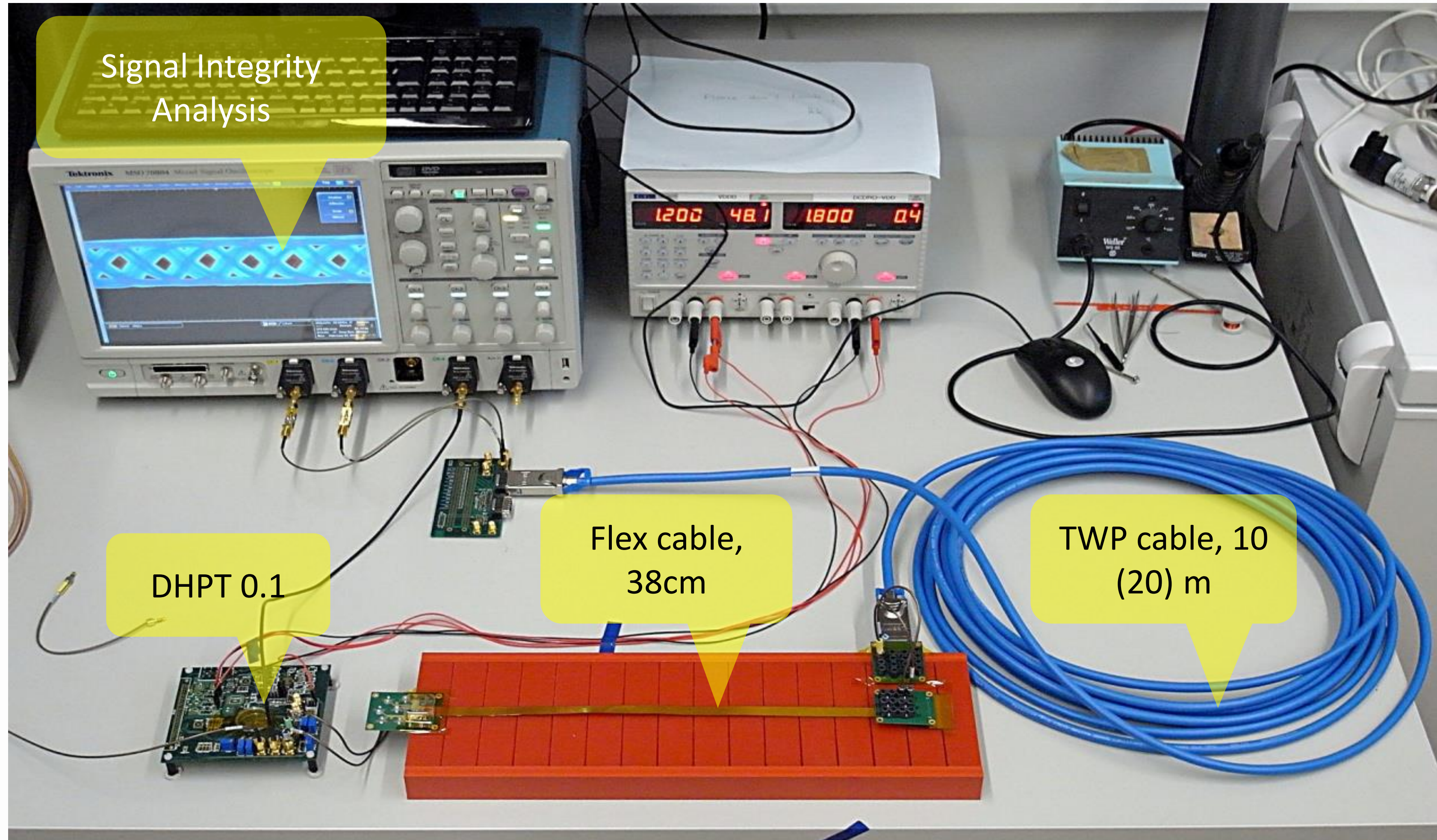

DHPT 0.1 – Signal Integrity Analysis

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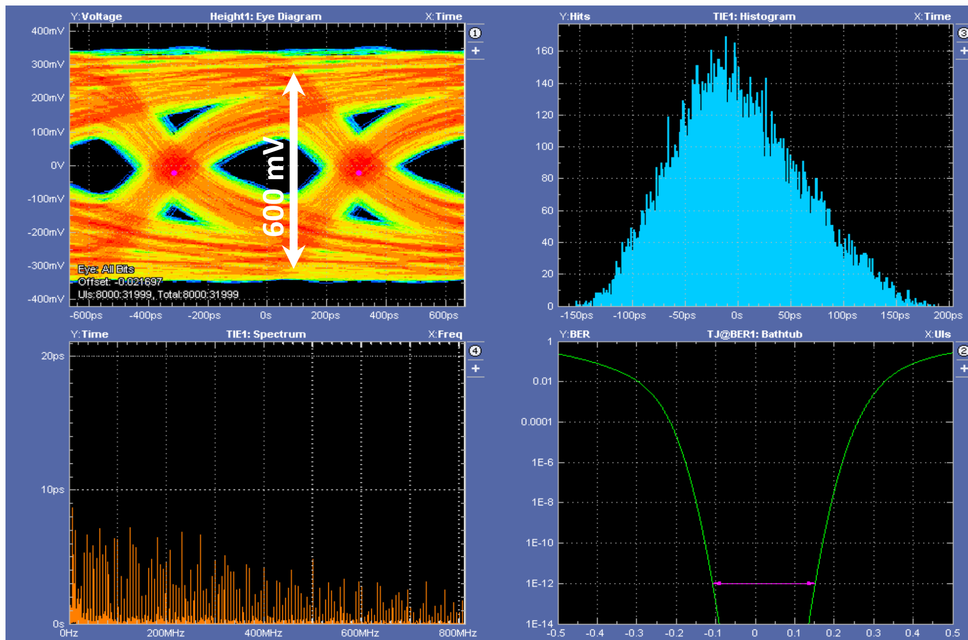
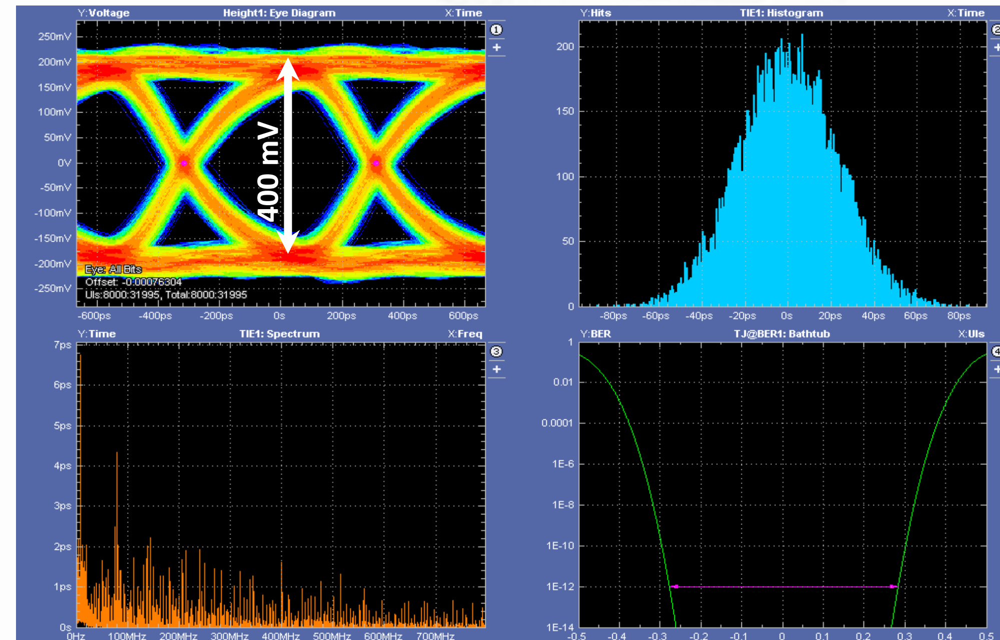
- 1.6 Gbps, 8bit LFSR sequence
- 10m Infiniband cable (LEONI, AWG 26)



Preemphasis off



Preemphasis on (600ps, max. I_{boost})

Tapered TSV on ATLAS FE-I2/3 wafers

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- TSV formed in the peripheral bond pad
- TSV formation is a back side processing
  - TSV etched from the back side until the BEOL SiO2 stack
- Front side processing step needed to connect TSV bottom to Al pad on the front side → Cu plug (only for FE-I3)
  - No metal layers in the pad
  - ~9µm thick BEOL SiO2 stack technically difficult to etch from the back side through the TSV opening on the bottom