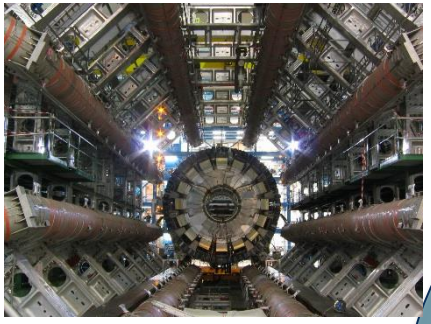
WP4 -3 task
SiGe ROC chips for HEP

OMEGA microelectronics laboratory
Ecole Polytechnique & CNRS IN2P3
http://omega.in2p3.fr

Organization for Micro-Electronics desiGn and Applications

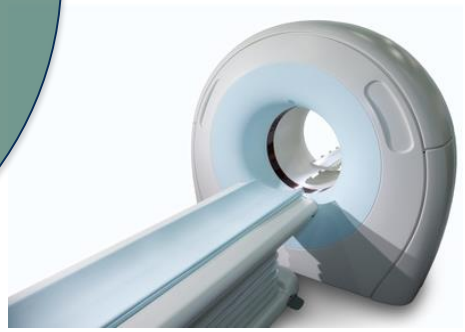
Omega microelectronics lab



Research,
Institute

Education
School

Industry,
company



WP4 SiGe

- OMEGA coordinates SiGe run for WP4.3
  - Long experience with SiGe
  - Building consortium of « SiGe fans » (FNAL, IFIC, INFN…)
  - Interest for ATLAS Lar, CMS muons, ILC, PET…

- 3 milestones
  - Mid 2016 : choice of SiGe 130nm foundry (MS22 for M14 : june 2016)
  - October 2017 : final design review of chips in SiGe run (MS64 for M30)
  - February 2019 : test report of the chip in SiGe run (MS96 for M46)

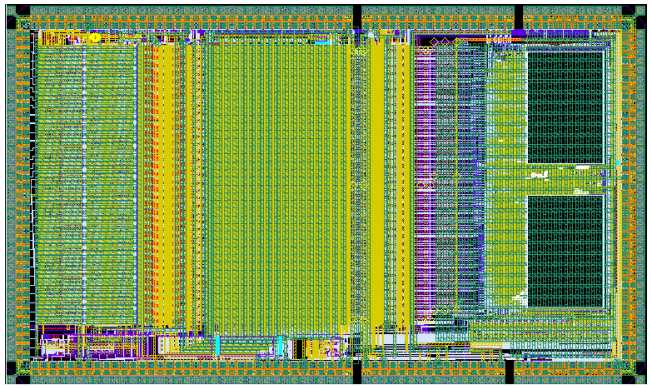
- 1 deliverable : submission of an engineering run in SiGe before april 2018 (D4-2 for M36)
  - SPIROC3 for WP14 SiPM of CALICE AHCAL
  - PETIROC for WP13 RPCs of CMS upgrade
  - chips of other labs of the consortium

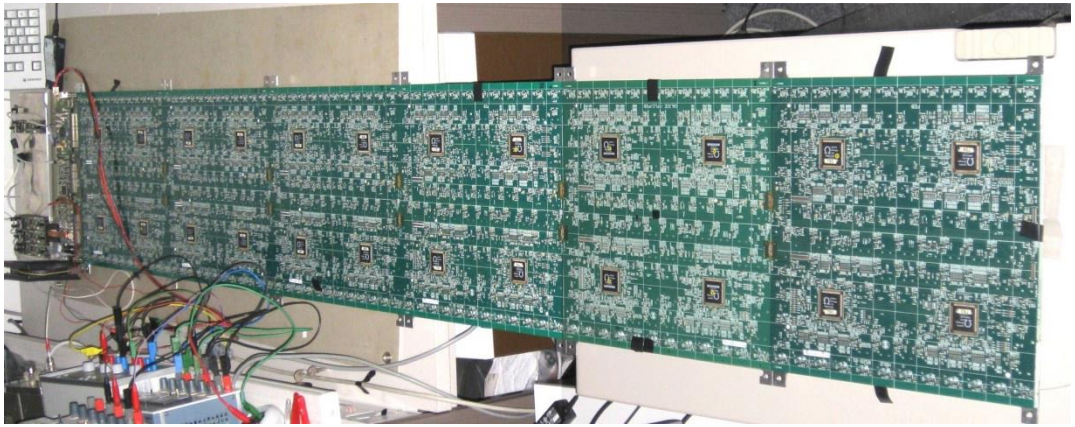
SPIROC for SiPM readout in SiGe 350 nm

- SPIROC : Silicon Photomultiplier Integrated Readout Chip
  - Developed to read out the sipm of the analog hadronic calorimeter for CALICE (ILC)
  - DESY collaboration (EUDET project)
  - Chip embedded in detector : low power !

$(0.36m)^2$ Tiles + SiPM + SPIROC (144ch)

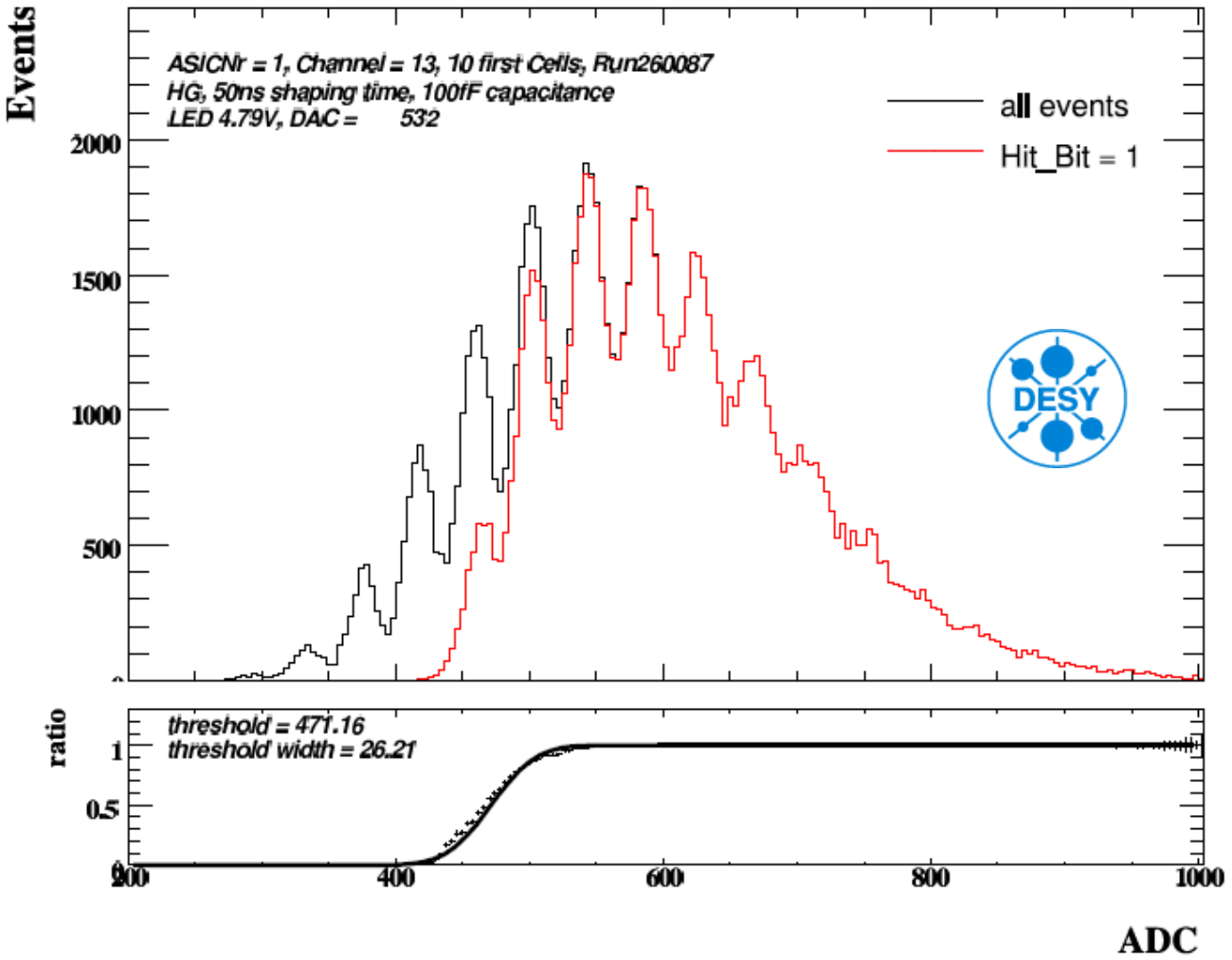
- 36 channels autotrigger 15bit readout
  - Energy measurement : 15 bits in 2 gains
  - Autotrigger down to ½ p.e.
  - Time measurement to ~1ns
  - Power dissipation : 25µW/ch (power pulsed)





SPIROC2 in SiGe 350nm performance

SiPM SPECTRUM with Autotrigger

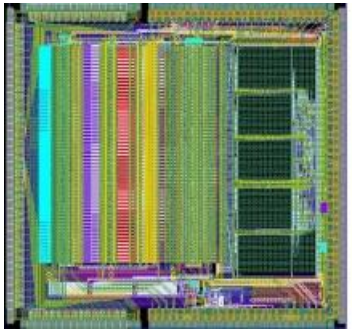


SPIROC3 in SiGe 130nm

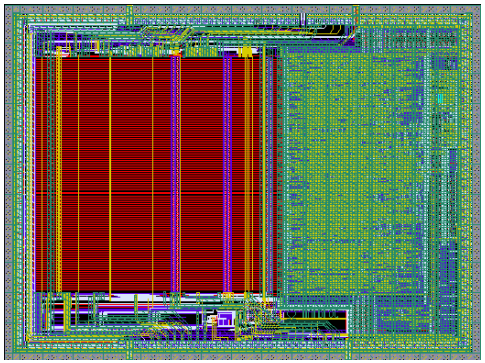
3rd generation of ILC ROC chip

SPIROC3 to readout the AHCAL of CALICE :

- 36 **Independent channels (= Zero suppress)**
  → **Digital part much more complicated**
  (36 address pointers, ReadOut, BCID, SCA management)
- New TDC with no dead time
- **New Slow Control** (Triple voting) using I2C **link**



SDHCAL 2nd gen.
HARDROC2
SiGe 350nm
4.7mm X 4.3 mm
20mm2



SDHCAL 3rd gen
HARDROC3
SiGe 350nm
6.3mm X 4.7 mm
30mm2

SiGe GHz Front End

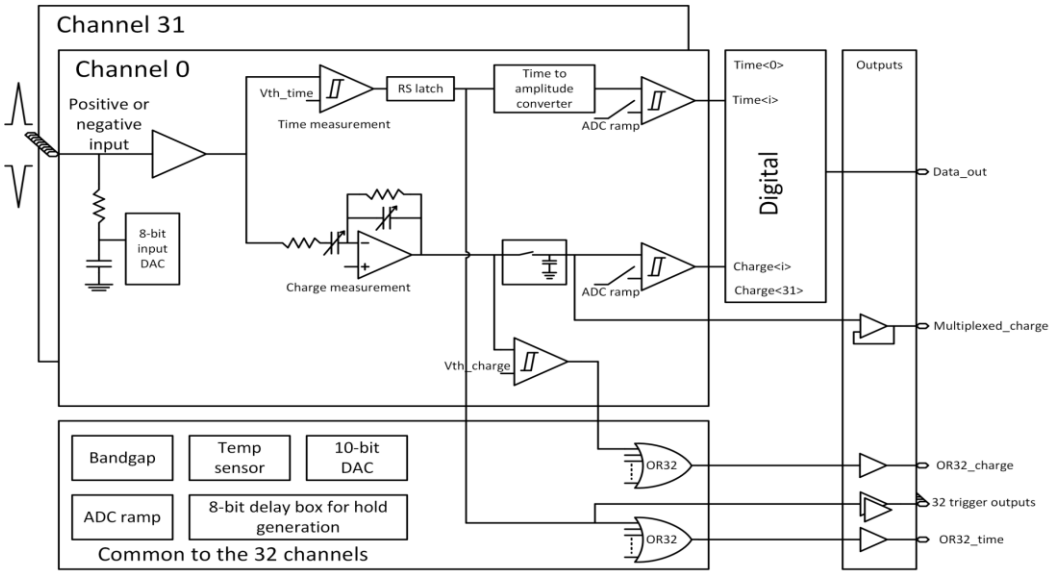
- R&D of 10GHz GBW preamps for applications where fast timing or high timing resolution is needed (TOF PET MRI, preclinical, particle physics…)
- 3 architectures in 0.35µm SiGe technology integrated and tested

Testboard #3	**RF (Common Emitter)**	**Common Base**	**Super Common Base**
With 100pf/50 Ohm injector (SiPM emulation)		Vb_cb : 400 #DAC	Vb_scb : 1023 #DAC
Noise floor (pedestal)	185-187 #DAC / 1.196V	216-224 #DAC / 1.259V	340-342 #DAC / 1.514V
Signal value @ 10pe	235 #DAC / 1.300V	137 #DAC / 1.085V	115 #DAC / 1.038V
Signal amplitude @ 10pe (signal minus pedestal)	50 #DAC / 110mV	83 #DAC / 174mV	226 #DAC / 476mV
Gain (mV/pe)	**10.4mV/pe (5 #DAC/pe)**	**17.4mV (8.3 #DAC)**	**47.6mV/pe (22.6 #DAC/pe)**
Jitter - threshold 1 pe @10pe	**13ps RMS**	**6ps RMS**	**8ps RMS**
Jitter - threshold 3 pe @10pe	**8ps RMS**	**6ps RMS**	**8ps RMS**
With 100nF DC block (for voltage gain & BW meas.)	**18mV injection**	**18mV injection**	**7mV injection**
Signal Value	267 #DAC / 1.371V	41 #DAC / 0.884V	192 #DAC / 1.2V
Signal amplitude (signal minus pedestal)	81 #DAC / 175mV	179 #DAC / 375mV	150 #DAC / 320mV
Voltage gain (before 50 ohm bridge => factor of 0 .5)	**4.86 V/V**	**10.4 V/V**	**22.5 V/V**
Bandwidth, after discriminator (Δt 10% T50% meas.)	**Δt : 150ps / 660MHz**	**Δt : 360ps / 280MHz**	**Δt : 400ps / 250MHz**

⇒ **Need to test these structures in new SiGe 130 nm**

PETIROC from 350nm to 130nm

- 32 ch SiPM GHz readout ASIC, dual polarity, 100 fC-400 pC, 6 mW/ch
- 32 trigger outputs and multiplexed data output
- Embedded 10 bit ADC and 50 ps TDC
- Dual threshold : first photons and energy



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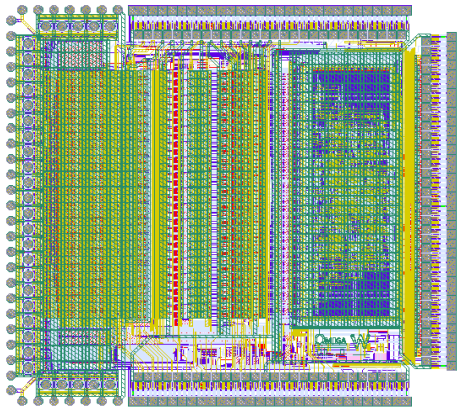

New PETIROC in SiGe 130nm to readout RPCs for CMS muon upgrade with new TDC

→ increase digital speed and complexity

→ decrease power dissipation

Conclusion

- SiGe is an interesting technology for high speed, low power, large dynamic range readout chips

- A large family of ROC ASICs has been realized by OMEGA over the last 10 years in AMS SiGe 350 nm. They are used by many groups (ATLAS, CALICE, …..

- A new SiGe 130nm technology is now being investigated to enhance analog and digital performance of SoC