AIDA-2020 KICK-OFF meeting
WP4
Task 4.3
Microelectronics

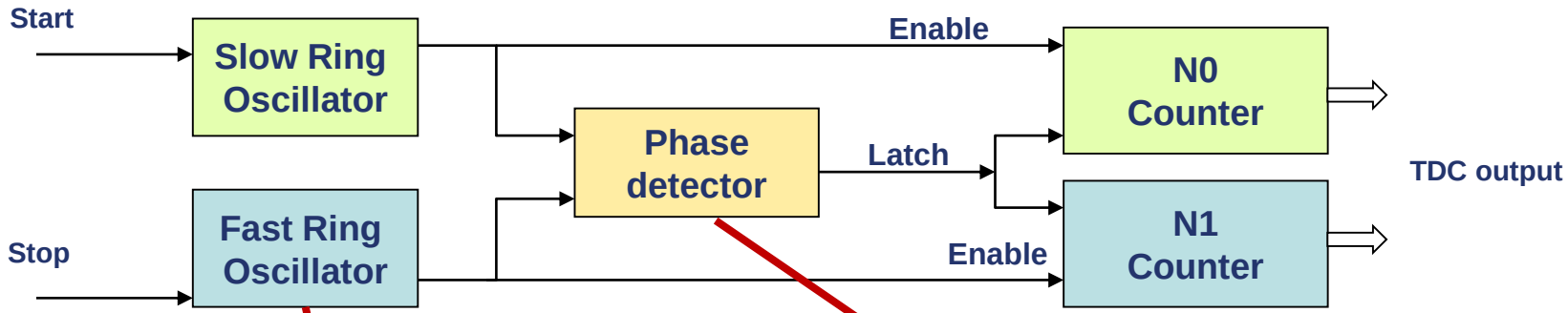
"Timing Readout – TDC Design"

Université Claude Bernard Lyon 1

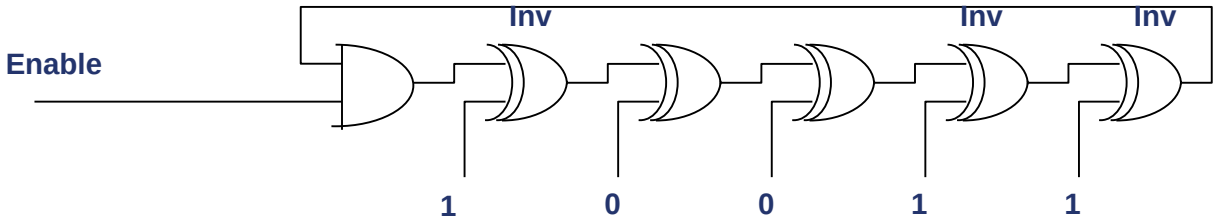
Université Blaise Pascal

TDC Architecture

130 nm IBM process



The basic element can be an XOR cell



- D Flip-Flop
- Custom Flip-Flop

First Test Results

Oscillators:

- Period Range ~[2.8 ns , 3,1 ns] pour 20°C < Temp < 60°C
- Tuneable range (LSB) : ~ 200 ps over 512 code (0.4 ps/code)
- Good agreement with simulations

Custom Flip-Flop:

- Minimum set-up time = 15 ps (including generator jitter)

Phase detector with custom Flip-Flop (S-curves):

- 6 ps width
- RMS resolution = 1 ps (including generator jitter)

- Over a dynamic range of 1ns all the steps are well separated
  - LSB = 65 ps
  - DR = 1 ns

Expression of Interest

May 2014:

The microelectronics group of IPN Lyon (MICHRAU) is currently working on a Digital Vernier TDC architecture based on ring oscillators. We developed an original technique which allows to control and to adjust the TDC resolution to a few ps.
This architecture has already been tested successfully on FPGAs (10 ps RMS resolution over a range of 1 ns, paper to be published on "digitally controlled ring oscillators in FPGA for ring oscillator Vernier TDCs" and http://stacks.iop.org/0957-0233/25/035101). We measured that the main limitation is the jitter and especially the cumulated jitter inherent to this kind of non regulated ring oscillators.
An ASIC version has been designed in IBM 130nm process and it will be tested this summer to check if the jitter can be reduced with a well controlled layout and also to measure which resolution and binning can be achieved for the whole TDC. This design is based on standard cells except one custom flip-flop with very low setup time. The goal is to obtain a binning of 10 ps and a RMS resolution as low as 3ps.

Expression of Interest

This work could be then continued within the AIDA-2020 work-package in microelectronics as described below:

- ***Reducing the jitter as much as possible by working on low jitter digitally controlled ring oscillators and then design a better TDC using this architecture.***
- ***Exploring other architectures, based on the same principle of digitally controlled chain. For instance we could try to use the architecture based on the Wave Union delay-chain TDC that has been realized on FPGA with resolutions of about 10 ps associated with our digitally controlled delay chain in order to further improve the resolution.***
- ***We could implement a multiple phase detector in order to reduce the measurement range which will also result in reducing the cumulative jitter impact and the dead time.***
- ***The final aim is to integrate the best structure of the TDC* with the 10 GHZ GBWP Front End that will be designed by OMEGA in 130 nm technology.**

These designs are in collaboration with WP13 on Gas Detectors (Task 13.2.2)

Architecture limitations

Main limitations:

- Dead Time
- Cumulated Jitter
  - Power supply
  - Transistor Noise

Work in progress :

- Study of cumulated Jitter origin in Ring Oscillators
- Noisy MOS transistor identified
- Increase XOR jitter/noise performance

- Jitter due to power supply : as a function of noise frequency on Vdd
  - In open Loop : 20 fs/mV/XOR

$$J_{XOR}(RMS) = \frac{LSB^{\frac{3}{2}}}{K * \sqrt{T_0 * 2 * N_s}}$$

- K : fraction of LSB
- T_0 oscillation frequency
- N_s : number of stage in the RO
- T_0 = 2ns, LSB = 20ps, K = 10, Ns = 9
- J_{xor} (RMS) = 47 fs
- $J_{xor\text{-}IBM}$ (RMS) = 82 fs

Summary

FPGA

ASIC V1

- Standard cell
- 1 custom cell

- New version in study
- Foundry submission Q3 2015 : could be 17th August 2015
- Continued Study with Aida funding

Involved people @ IPNL:

- E.Bechetoille
- M.Dahoumane
- C.Girerd
- H.Mathez

For a total of 12 mm over 4 years