WP 13.3.3

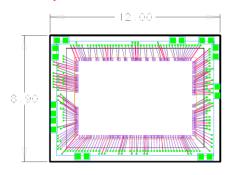
Development of a Multi Chip Module using HDI-technology and 3D- mounting of chips for MPGD readout

AIDA2020 Kick-off meeting 4.6.2015

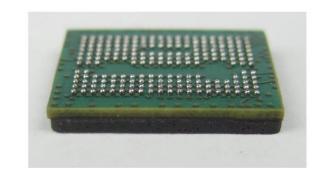
Leif Jönsson Lund University

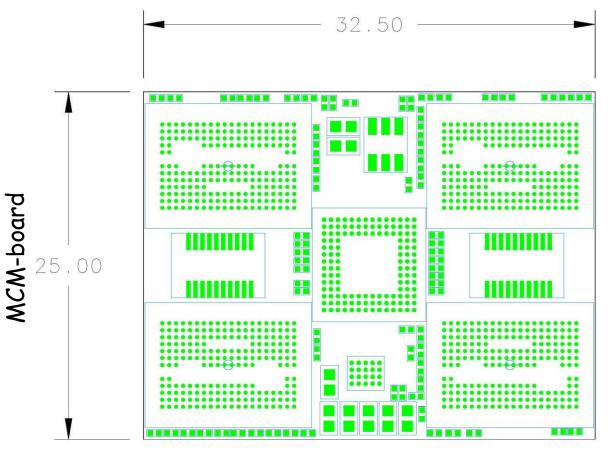
SALTRO16-chip - Carrier-board - MCM (Multi Chip Module) -board

Carrier-board and SALTRO16-chip





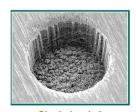




- The Carrier-board (8.9x12.0 mm2) with mounted SALTRO16-chip (6.2x8.7 mm2) is presently under test and debugging.
- 8 Carrier-boards will be mounted on an MCM-board (4 on top and 4 on bottom)
- The MCM-board will be designed in HDI-technology (High Density Interconnect)
- This gives a space occupancy of 6.4 mm2 per channel

Advantages of HDI (High Density Interconnect) technology

- Routing density higher both for signal and voltage supply
 number of layers can be decreased
- Laser drilling allows for a holes as small as 25 μm diameter with collars of 50 μm.
- The drilling can be performed to different depths depending on the energy in the laser beam.



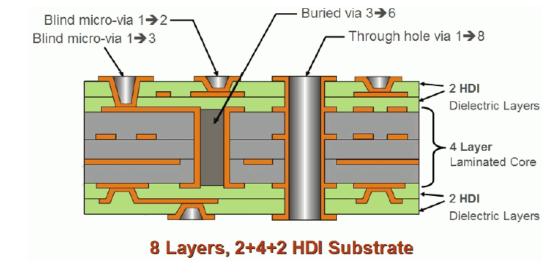


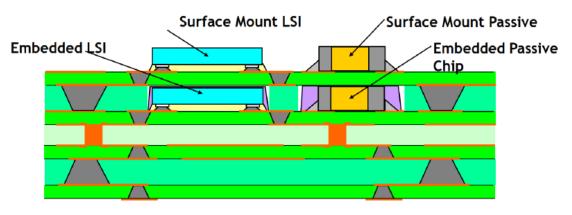
Single level via

Stepped via

- The core is a standard multilayer PCB.
- Onto this a thin prepreg layer (dielectrica +copper) is laminated.
- Together with sequencial laminate application vias can connect different layers.
- The prepreg layers can be as thin as $5 \mu m$.
- Due to via-in-pad techniques all routing can be performed in the inner layers such that essentially the whole surface can be used for mounting of components.

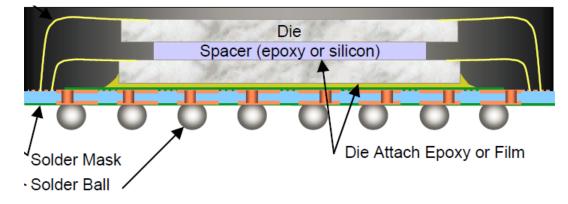
This technology also offers the possibility to create cavities in the PCB where electronic och mechanical components can be mounted and thus embedded into the PCB so that essentially the full surface is available for surface mounting of chips.





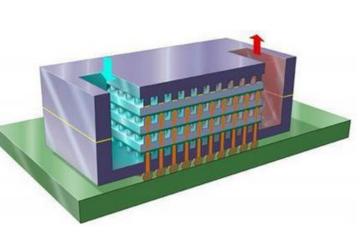
Stacking of chips and micro-channel cooling

- In order to achieve even higher channel density it is possible to stack chips on top of each other
- This would require a new Carrier-board and MCM-board



U. U. IMI

• Micro-channel cooling, developed by the semiconductor community for cooling of IC-chips, offers an interesing option, which will be further developed by WP 9.2. We hope to profit from this development.



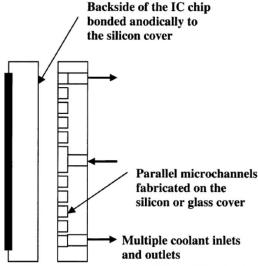


Figure 2 Schematic arrangement of an IC chip cooled with microchannels fabricated on a silicon or glass cover bonded anodically or glued to the backside of the chip (not to scale).

WP 13.3.3: Participants

CERN: Support for the use of the SALTRO16 chip (Lucie Linssen), (micro-channel cooling)

Lund: Development of the MCM-board in HDI technlogy and stacking of chips

Four-year planning

Year 1: design of the MCM-board in HDI-technology

Year 2: production, mounting and programming of the MCM-board

Year 3: debugging and tests of the MCM-board

Year 4: design of Carrier-board with stacked chips

Planning for the first year

Month 1-8: Design of the 1st vesion of the MCM-board

Month 9-10: Prototyping and debugging

Month 11-12: Design of the 2nd version of the MCM-board

Task 13.3 Tools to facilitate the detector development (CERN, ULUND)

1. Interfacing FE-chips specific to gas detectors to the Scalable Readout System (SRS)

The FE chip VMM128, GEMROC and TIMEPIX3 are interfaced to SRS by designing, prototyping and engineering in view of large production of chips.

2. Development of cheap, standard MPGD dedicated laboratory instruments

The development of MPGD dedicated laboratory instrumentation (remotely controlled compact HV power supply, picoamperometers and signal processing modules) proceeds through the following steps: collection of the user requirements, design, prototyping, prototype testing, final engineering and validation of the engineered instruments.

3. PCB development using HDI-technology and 3D-mounting of chips for MPGD readout

The development of MPGD dedicated PCB using HDI-technology and 3D chip mounting is performed by designing and prototyping followed by a test phase.

N	Milestone number 18	Milestone title	Lead beneficiary	Due Date (in months)	Means of verification
N	/IS94	PCB development using HDI-technology and 3D-mounting of chips for MPGD readout (Task 13.3)	27 - ULUND	44	Prototype

Finances for Lund (WP13)

1	JRA1
Person-months	11.00
Personnel cost	66,000.00
Non-personnel direct costs	18,000.00
Subcontracting	0.00
Direct costs (excluding access)	84,000.00
Indirect costs	21,000.00
Access cost	
Lump sum, flat-rate or unit cost	
Total costs	105,000.00
Requested EC contribution	45,000.00

Lund has to contribute 60.000 Euro over 4 years

Current financial resources:

Lund Univeristy: ~30.000 Euro/year = ~120.000 Euro over 4 years