WP4.2 65nm Microelectronics

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Access to TSMC technologies

Data and technical support

Institute should contact IMEC to sign an NDA

- IMEC has a list of CERN collaborating institutes
- IMEC will distribute the Mixed Signal design kit and provide users with design kit maintenance and technical support

No access fees. Pay-per-use scheme.

- A 7% fee is applied on the fabrication cost (prototyping, production).
- This fee covers part of the Mixed Signal Design Kit development and maintenance costs
- Projects that make use of the Mixed Signal Design Kit must seek fabrication services exclusively via CERN and IMEC service

Foundry services

Institute should contact CERN to inform about submission plans
CERN will make an effort to coordinate submissions to share prototyping costs
CERN will issue the purchase orders to IMEC
CERN will receive the fabricated chips and distribute them to designers

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TSMC Non Disclosure Agreement (NDA) *and Master Technology Usage Agreement (NDA-MTUA)*

3-party NDA: TSMC- IMEC – Institute

- Permitting the distribution of technology information from IMEC to institutes, including layouts of std. cell libraries
- Permitting institutes to exchange technical data and work in collaboration

Covers both 65nm and 130nm processes

Use restrictions:

- automotive applications
- medical applications except for medical imaging systems
- any military applications
- nuclear materials related to defense system or power systems
- aerospace application except fundamental scientific research and dosimetry

Sale of chips is permitted except for banned applications

Export control restrictions

- Comply with all applicable national export control laws, regulations, and rules
- Institutes that will receive silicon from CERN must sign and return to CERN a “Letter of Compliance Concerning Deep-Submicron Technology Circuits”

All NDAs issued by IMEC are identical. Neither IMEC nor the foundry are willing to negotiate 35+ times with all single Institutes

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TSMC 65nm supported process and metal stacks

Two metal stacks

6+1 metals (“CERN metal stack”)

4-thin, 1-thick, 1-UTM , RDL

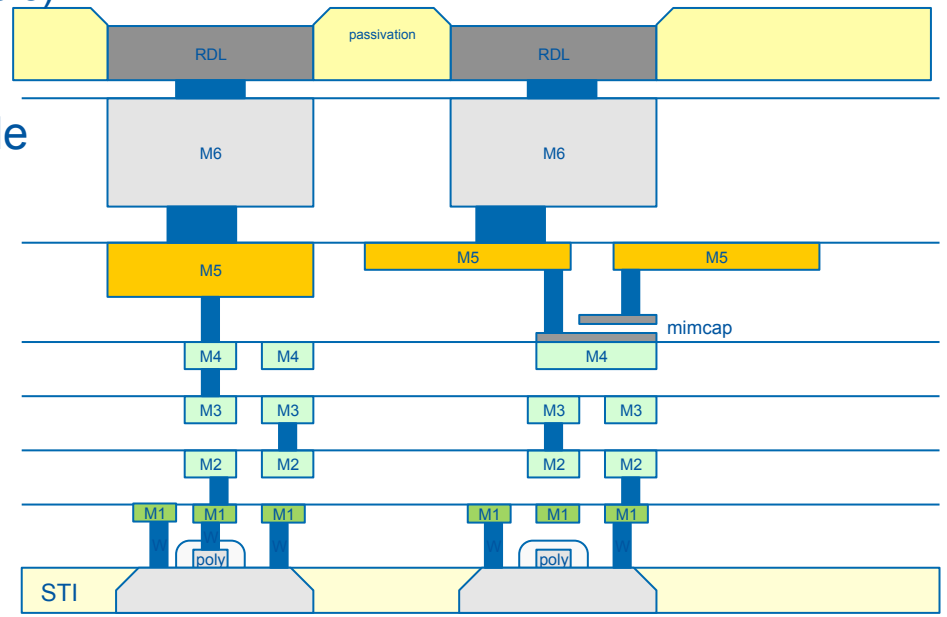
9+1 metals (compatible with IMEC mini@sic)

7-thin, 1-thick, 1-UTM , RDL

“Special” metal stacks can be made available

This will require a one-time-charge of 15-20KEuro + annual maintenance

Institutes can always get organized to share costs of special PDKs among themselves.



Two standard cell libraries

- 9-tracks, standard-Vt
- 7-tracks, high-Vt (Low Power)

Mixed-signal design kit is being distributed by IMEC to TSMC-IMEC NDA signatories

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Rad-hard IP Blocks in 65nm

- SRAM compiler
- I/O pad library
- Bandgaps
- Rad-hard to 200Mrad according to specifications
- Deliverables
  - Schematic (OA)
  - Layout (OA)
  - Abstract (OA)
  - .lib (Liberty) capacitance limits and timing if applicable
  - Verilog / Verilog-AMS models
  - Datasheet

Based on a slide from Sandro Bonacini

Foundry IP library

- Foundry provides a wide range of IP blocks
  - Electrical fuse blocks / NVM
  - PLLs
    - 100MHz – 1600MHz
    - Jitter enhancement
  - Specialty I/O
    - USB 2.0 / UTMI+
    - DDR2 (up to 800Mpbs), DDR1 (up to 533 Mbps)
    - Crystal oscillator, 32kHz
  - ROM compiler
  - Register File compiler
    - Single- and dual-port
  - SRAM compiler
    - Single-port and dual-port
    - Low-power and low-leakage

- Not made / not tested for radiation performance

Based on a slide from Sandro Bonacini

Soft IP blocks

- Portable RTL code
- I2C slave
  - 7- and 10-bit addressing modes
  - Synchronous design
- HDLC communication protocol
  - Average 7% (max 12%) bandwidth overhead
  - Non fixed latency
- 7b8b communication protocol
  - DC balanced
  - Fixed latency
  - Control characters available

Based on a slide from Sandro Bonacini

IP Block sharing

- During LHC-1 sharing of blocks was mostly within sub-detector groups or from CERN to outside institutes.
- Licensing was based on ‘gentlemen’s agreements’
- Significant duplication of effort

- RD-53 have agreement between member institutes but limited to RD-53 efforts
- For a more general purpose repository there is a need to solve the ‘engineer at the University of Saint-Genis’ problem
- Maybe a particular agreement is needed for AIDA members operating outwith the RD-53 framework?

Conclusions

- CERN will provide support and access to TSMC 65nm for AIDA members (provided they sign the NDA)
- Some budget is available to cover the cost of the AIDA engineering run (but this is far from the full cost)
- IP blocks are available but conditions may have to be defined for non RD-53 members
- The aim is to provide full wafers which can be used by the AIDA community for post processing

Thanks for your attention!