3D pixel design and simulations

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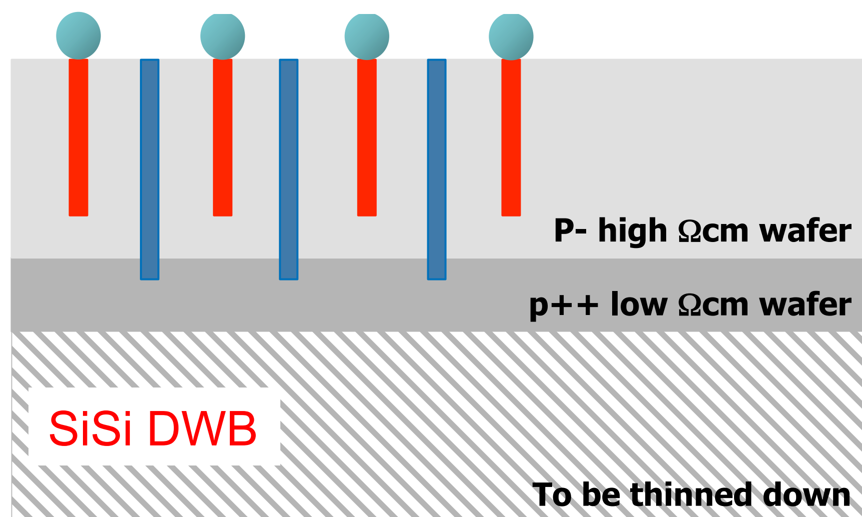
- D7.1 : Simulation of 3D pixel sensor cells [M18] Simulation of new sensor cells for thin 3D sensors with fine pitch, reduced column diameter and inter-column distance. Simulation of charge collection properties of 3D sensors with thinner substrates and determination of optimal thickness for pixel detectors working at HL-LHC. (Task 7.2)
- Work in progress and next steps

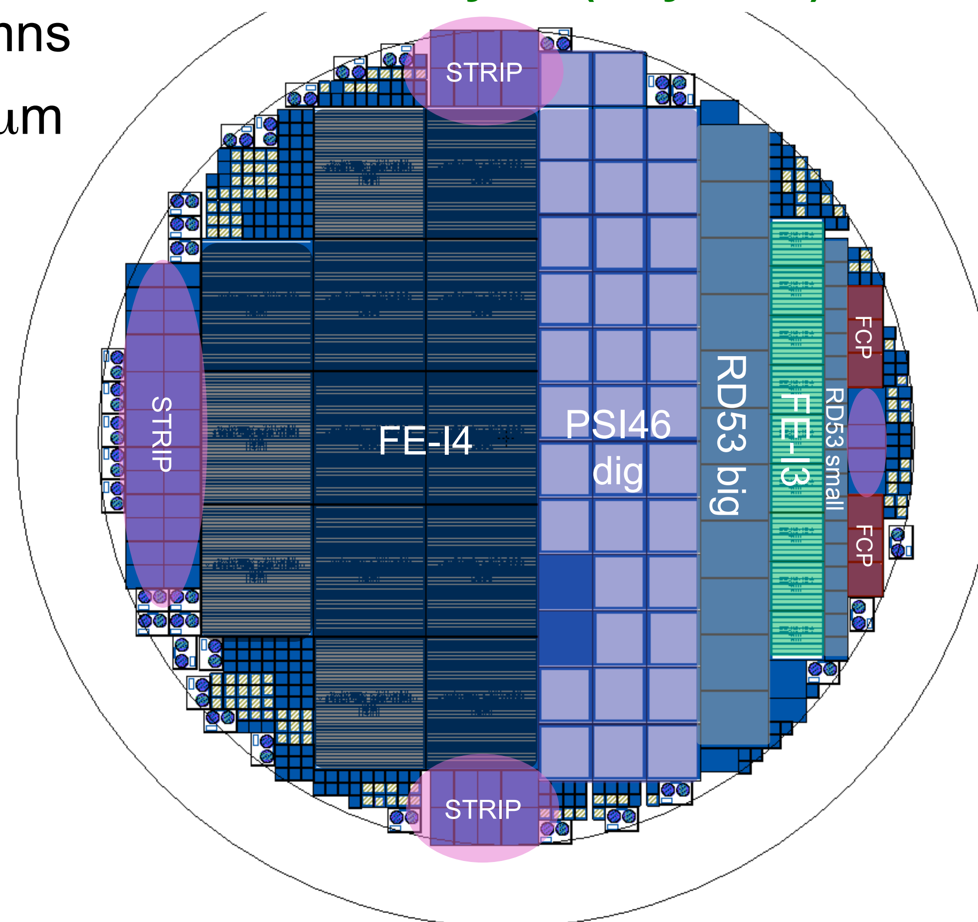
New thin 3D on 6” wafers @ FBK

- Single-sided process, with thin active layer: SiSi (or SOI)
- Passing-through Ohmic columns
- Non-passing-through junction columns
- Reduction of column diameter to 5 μm
- Holes (partially) filled with poly-Si
- Very slim or active edges

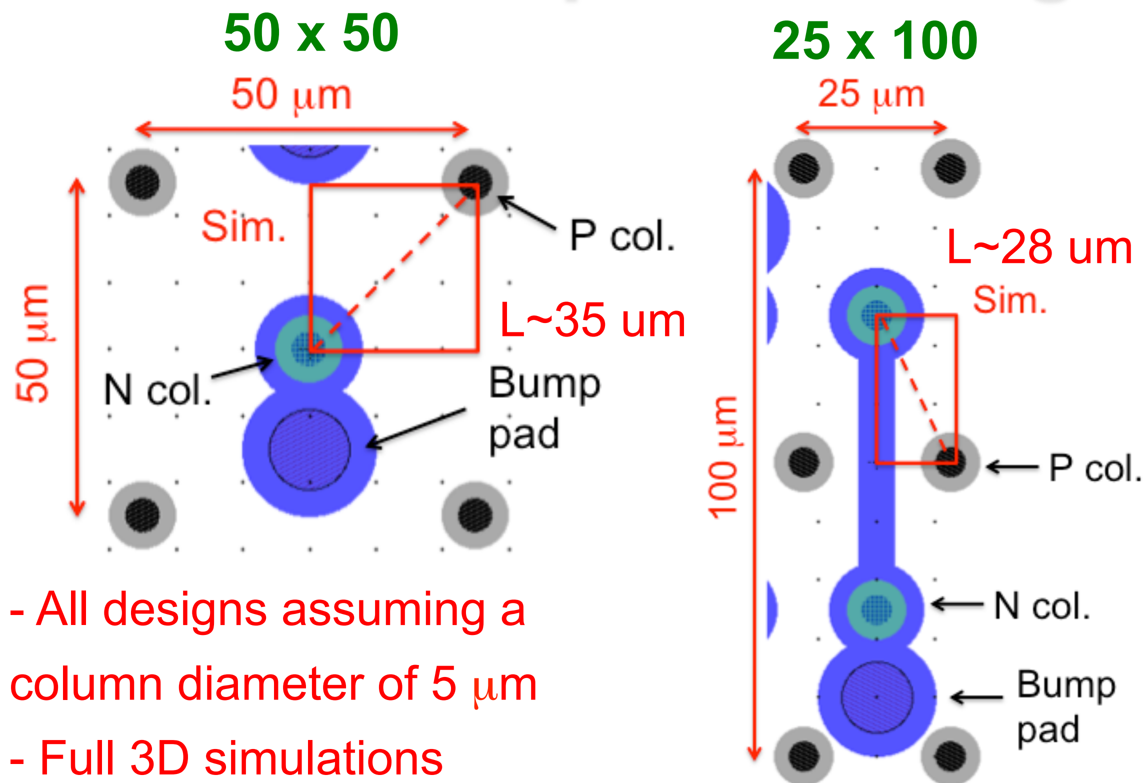
Schematic cross-section



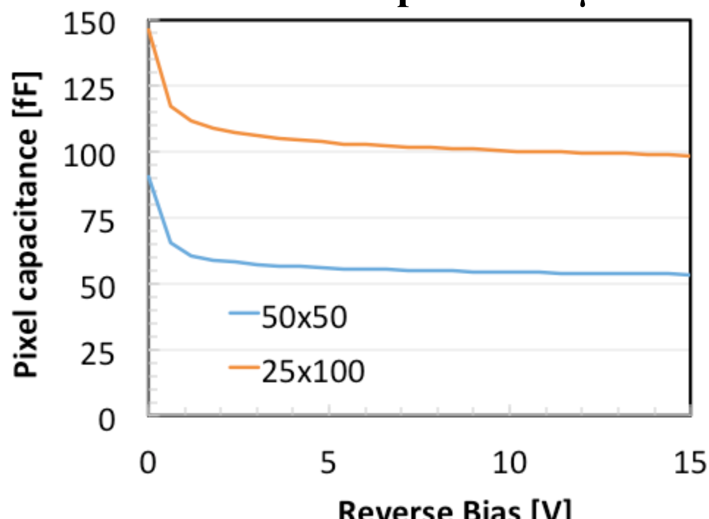
First wafer layout (May 2015)

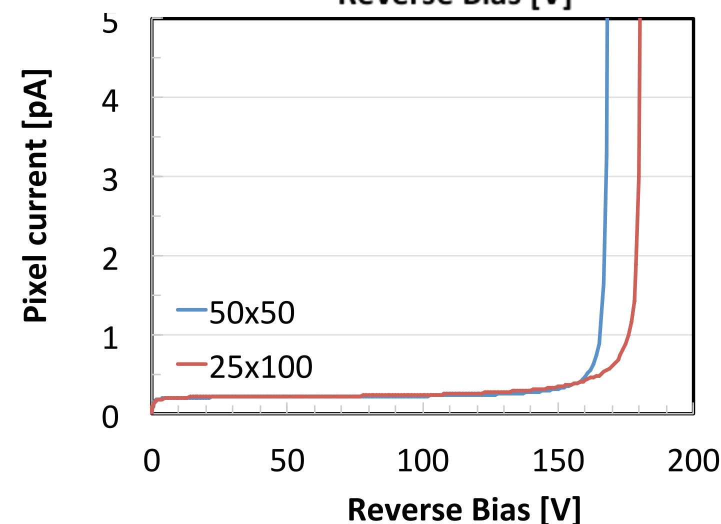


New 3D pixels: design and simulations



- All designs assuming a column diameter of 5 μm
- Full 3D simulations

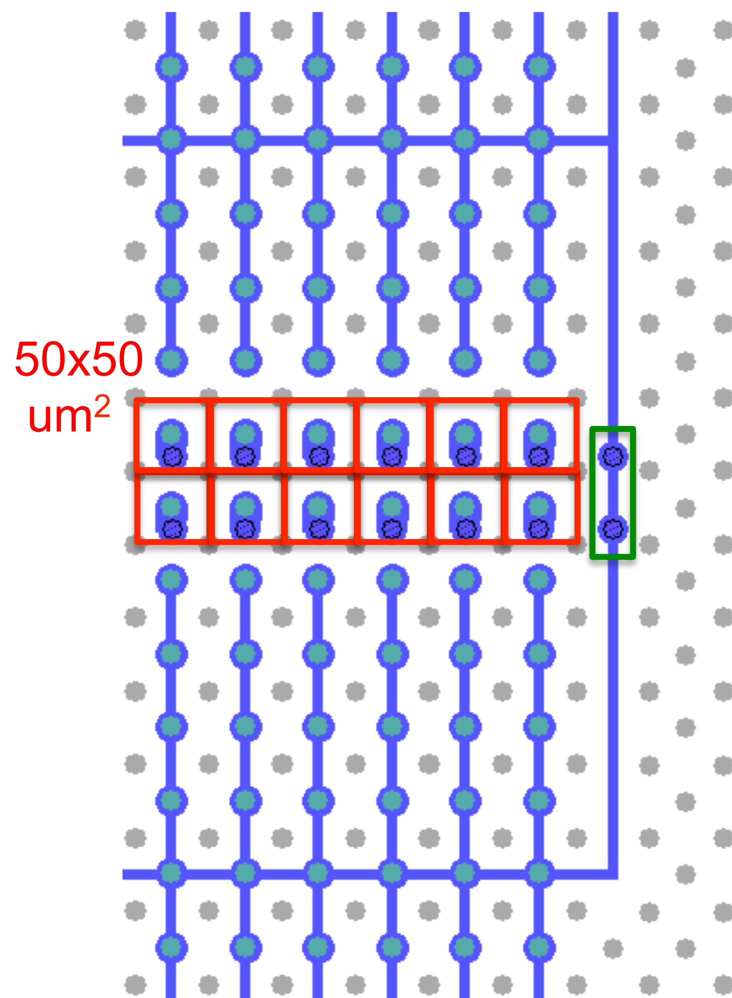




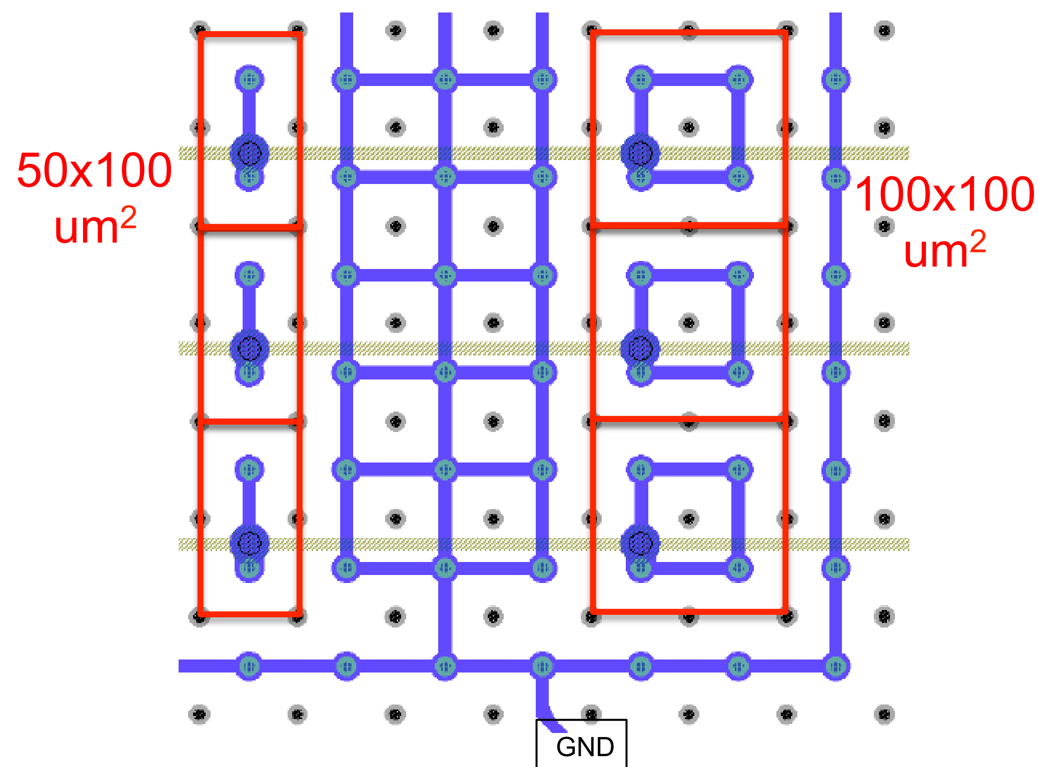
- 50x50 design safe, 25x100 is difficult … too little clearances (new ideas for bump pad to be tested)
- Capacitance compatible with RD53 specs, initial breakdown voltage high enough (to be refined with better surface-states models)

New pixels with existing ROCs ?

ATLAS FE-I4 50x50 (1E) + grid

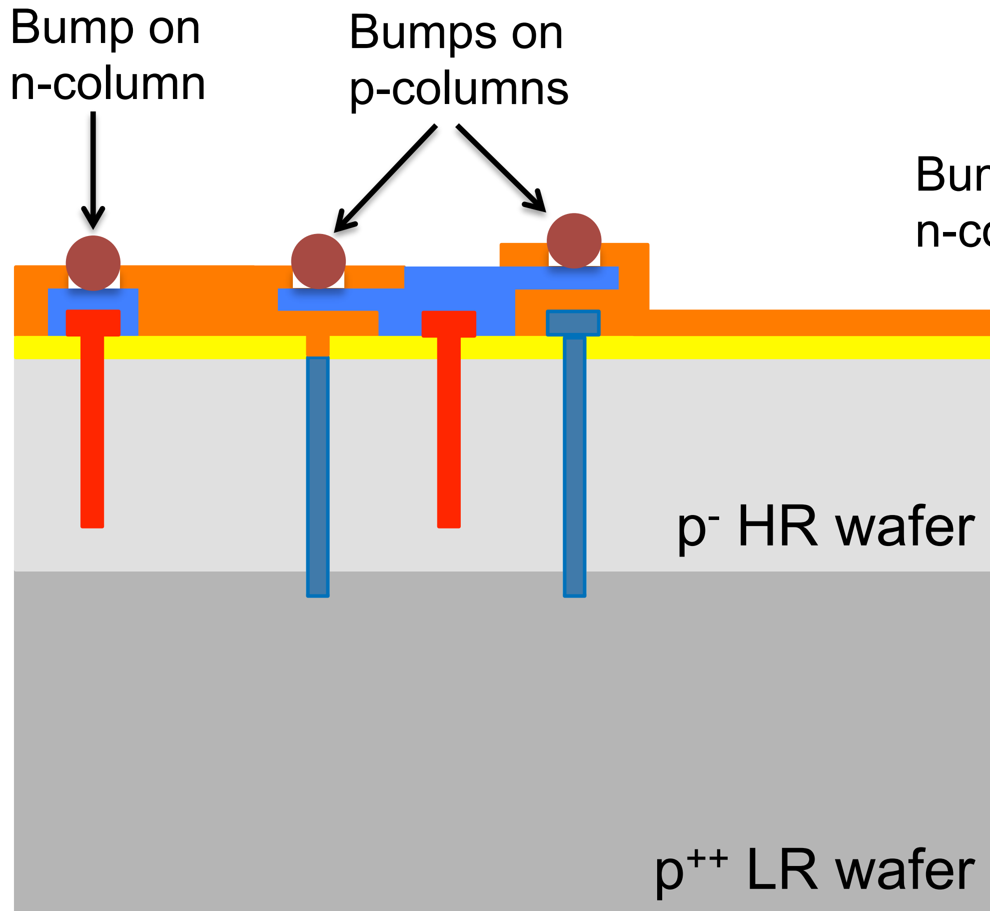


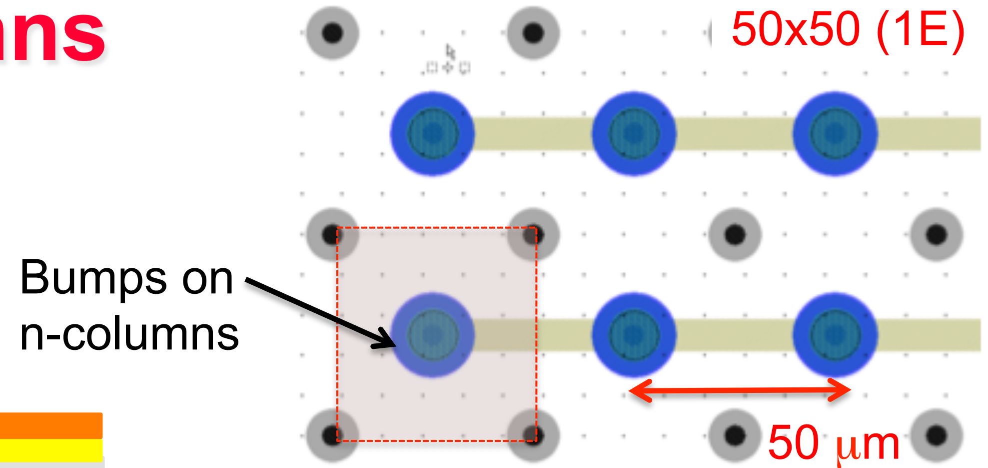
CMS PSI46: 50x50 (2E+4E) + grid

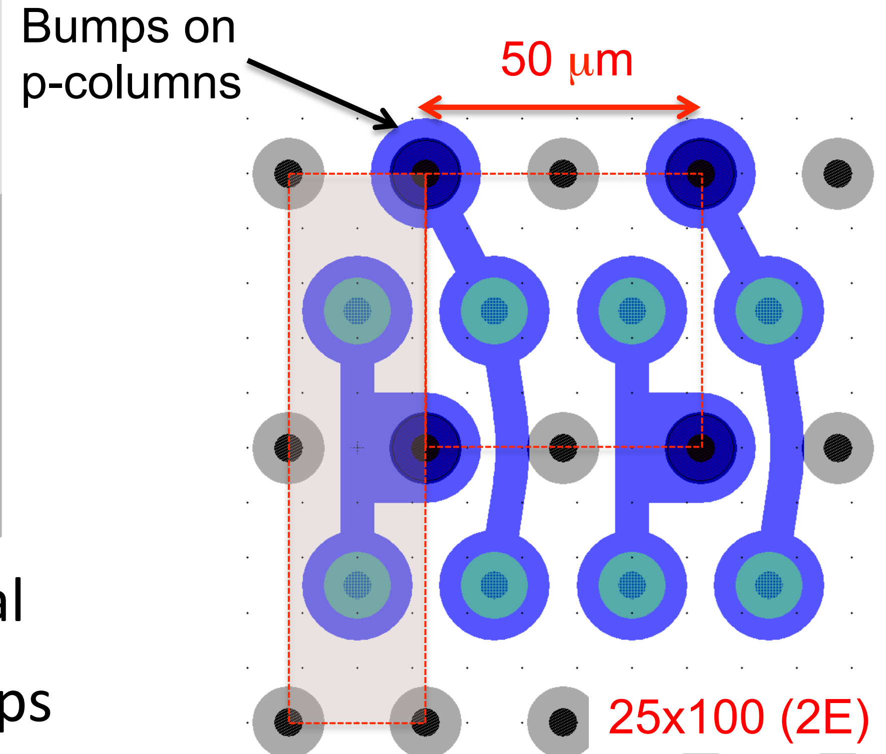


Small pixels take all bonding pads + rest of pixels at GND using a metal grid and extra-pads at the periphery

Bumps on columns







Very slim edges

- Very slim edge concept based on multiple ohmic columns termination developed for IBL (~200 μm) M. Povoli et al., JINST 7 (2012) C01015
- It can be made slimmer by reduced inter-electrode spacing

  (safely 75 - 100 μm, more aggressively down to ~50 μm)
- 3D guard rings also possible with similar dead area

25x100 (2E)

75 μm

Active area

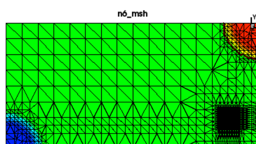
100 μm

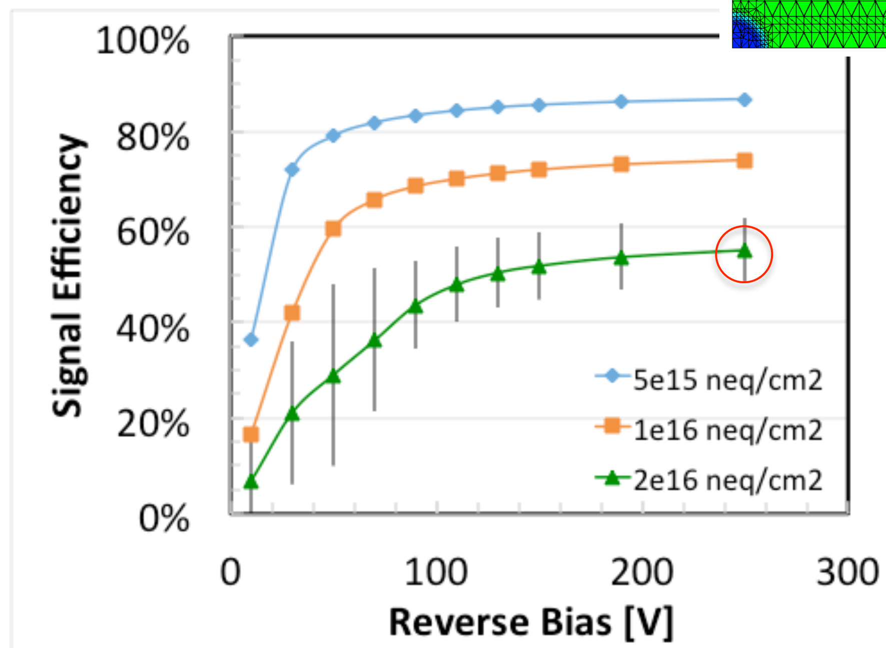
Active area

50x50 (1E)

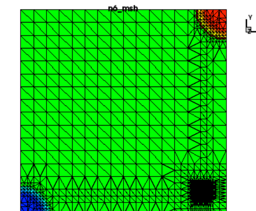
Signal Efficiency (preliminary)

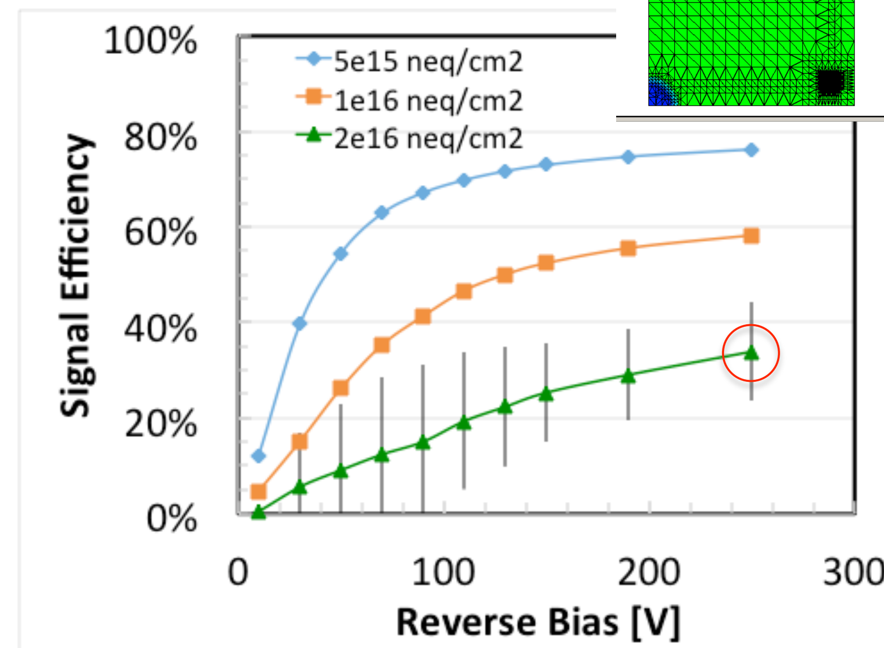
25 x 100





50 x 50





- 3-trap level "Perugia" model, M. Petasecca et al., IEEE TNS NS-53(5) (2006) 2971 with parameters from D. Pennicard et al., NIMA 592 (2008) 16

[Tends to underestimate SE at largest fuences, to be optimized, see D. Passeri]

- 1 μm thick (~2d) slice, with MIP vertical hits at several different points
- 20-ns integration of current signals, average, and normalization to injected charge

Status and plans

- Work done so far mainly aimed at defining the layout for a first batch at thin 3D at FBK, now submitted for fabrication
- More systematic studies to be carried out in AIDA-2020 WP7:
  - Impact of different layouts and process options
  - Charge collection with 3D simulation domains (effects of surface and column tips, inclined tracks, charge sharing)
  - Operation at high voltage (breakdown, charge multiplication)
- Additional effort will be devoted to planar active edge sensors (e.g., trade-off between dead area at the edge and breakdown voltage)
- All this requires:
  - Refined surface state model
  - Refined bulk damage model

  } Strong sinergy with modeling activity
  - Validation against experiments → Collaboration with all involved institutes