

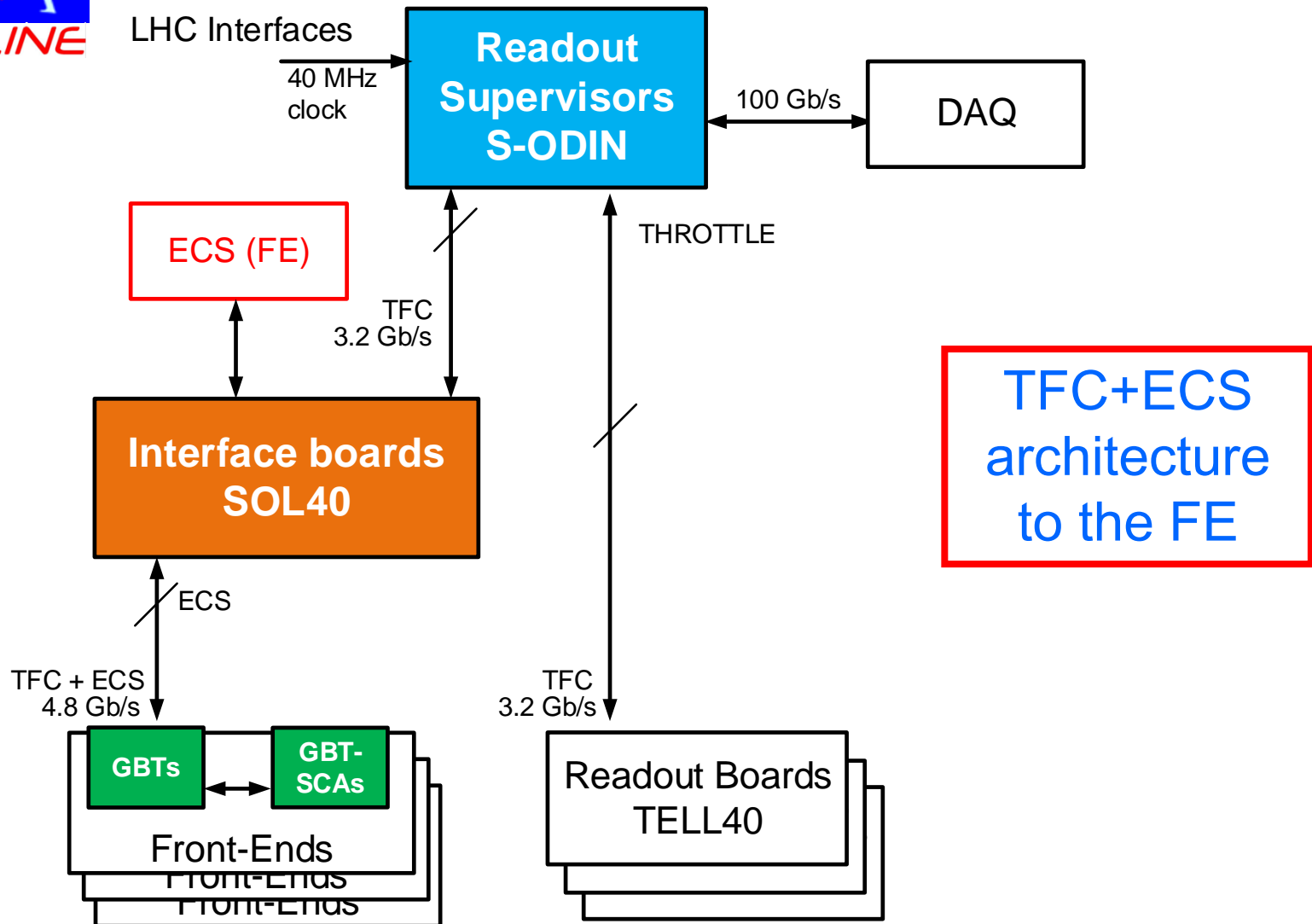


Developments for Front-End ECS

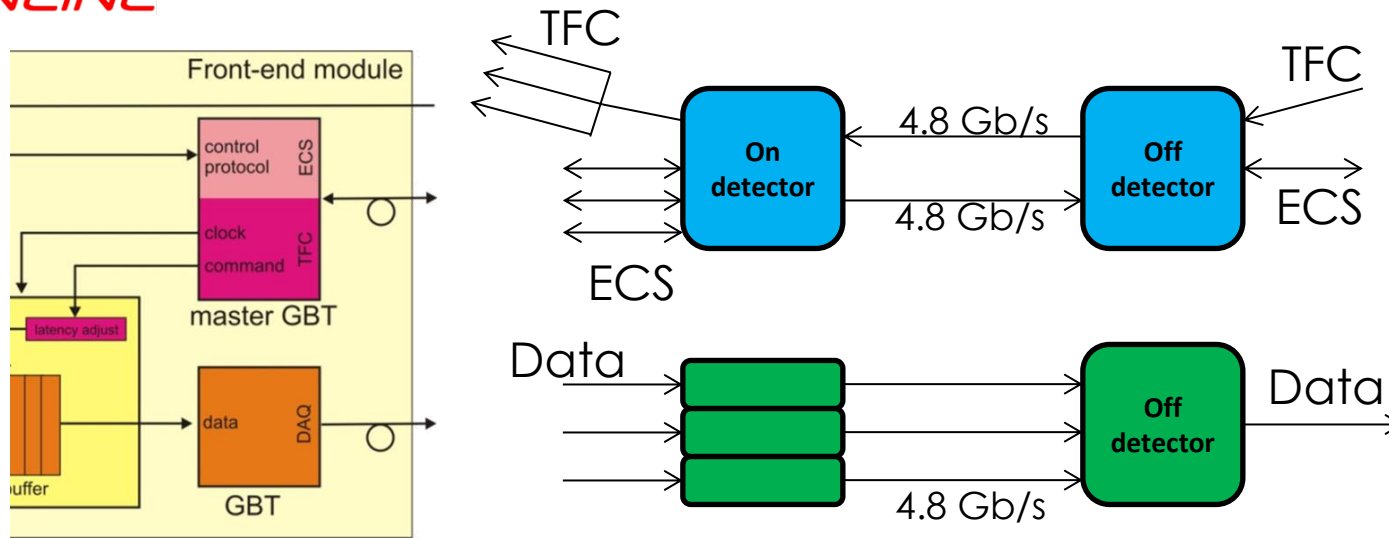
F. Alessio, C. Gaspar
(on behalf of all the people contributing to this)

LHCb Upgrade Electronics meeting
09-04-2015

Reminder: generic architecture



Reminder: Fast & Slow control to FE



Separate links between controls and data

- A lot of data to collect
- Controls can be fanned-out (especially fast control)

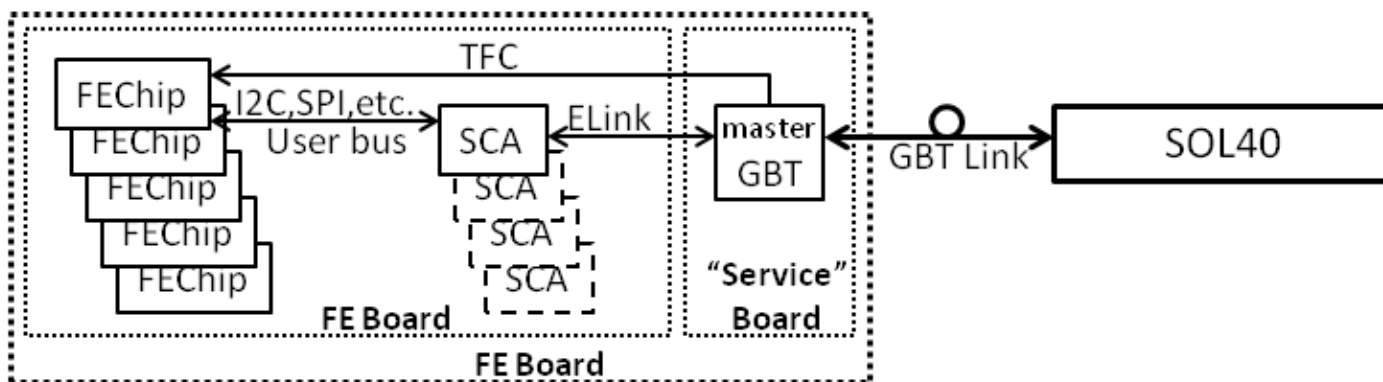
Compact links merging Timing, Fast and Clock (TFC) and Slow Control (ECS).

- Extensive use of GBT as Master GBT to drive Data GBT (especially for clock)
- Extensive use of GBT-SCA for FE configuration and monitoring

Main features

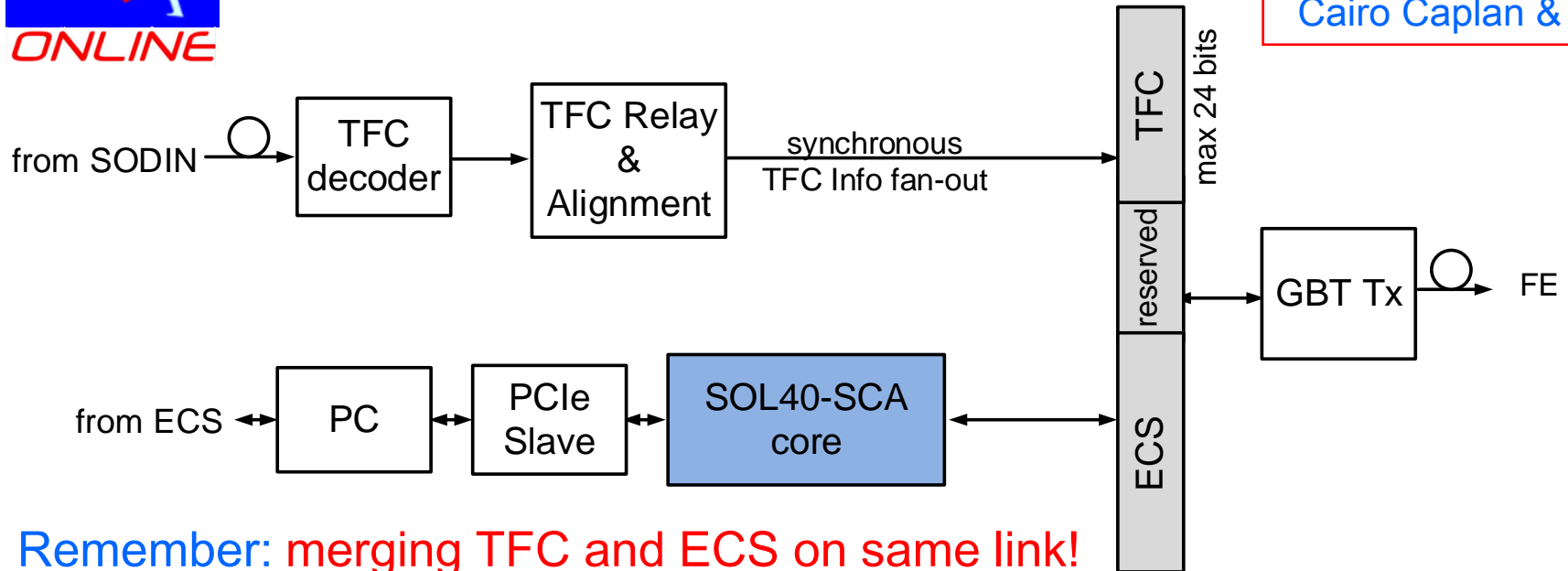
One (or more) SOL40 is used to control a slice of your FE:

- Propagate TFC information to the FE
 - Not covered here, see <https://cds.cern.ch/record/1491666?ln=en>
- Propagate ECS information to the FE
 - Configure/control Master GBTX
 - Configure/control Slave GBTXs
 - Configure/control GBT-SCAs
 - Configure/control FE chips
- Receive back ECS information from the FE
 - From all devices at the FE, return path
- Control all of this from WinCC, as usual
 - Within global LHCb ECS



Current developments: SOL40 firmware

Cairo Caplan & FA



Remember: **merging TFC and ECS on same link!**

→ SOL40 firmware will take care of doing all the complicated bit manipulations needed to control a GBT, its SCAs and your FE chipsets

- Responsible to generate right matrix of TFC commands to FE
- Responsible to delay TFC commands per partition/cluster of FE
- Single firmware for everybody with all necessary features and requirements → minimize unconformities, highly programmable
- **Centrally provided**

Current status: backbone ready, TFC part done, delays ready.

Current developments: SOL40-SCA core

It's a **firmware core** inside the SOL40 firmware which is responsible to:

- control the Master GBT and Slave GBTs at the FE
 - 1 Master GBT per link
 - Slave GBTs via I2C bus from Master GBT
- control all GBT-SCAs associated to that Master GBT
 - Up to 16(+1) GBT-SCAs per GBT link
 - Serialize/Deserialize with proper encoders (HDLC)
 - Targeting 36 GBTs to start with
 - Generic, no need to create specific commands at the ECS
- control all the FE chips associated to those GBT-SCAs
 - Support for all GBT-SCAs buses in a programmable way

For more details, see Cairo's presentation at Electronics Meeting in October

<https://indico.cern.ch/event/291724/contribution/2/material/slides/0.pdf>



Current developments: SOL40-SCA core

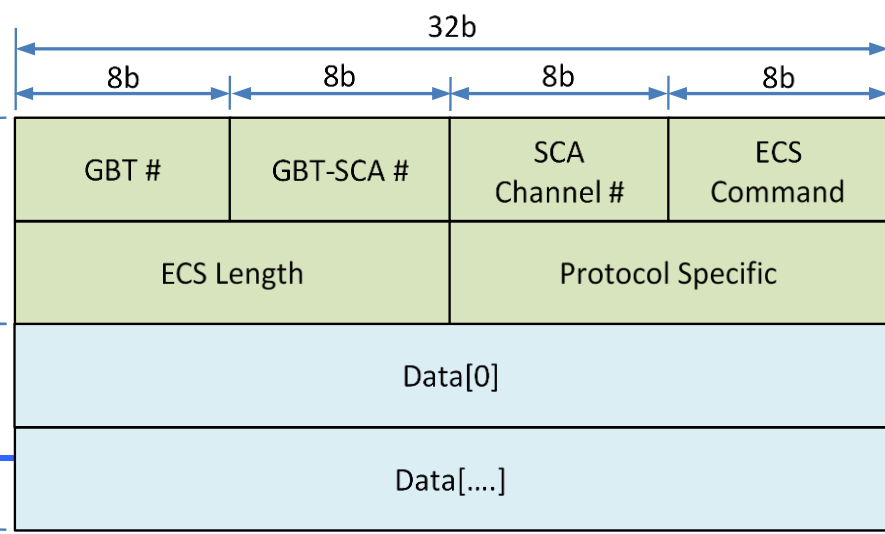
Current status:

- Backbone core ready → aim at fully qualifying it by summer
 - Included the part to control the Master GBTx
 - Under test in these weeks with (real) GBT and Mini-DAQ
 - First full I2C chain implemented
 - Will be tested soon in April by Cairo and GBT-SCA team with (real) GBT-SCA and Mini-DAQ
 - To do:
 - generic matrix to assign GBT-SCA to pair of bits
 - to add the other SCA protocols
 - retransmission of packets
 - checking of transmitted packets
 - Compilation done and looks quite good
 - 48% of Stratix V for 8 GBTs and 16 GBT-SCA/GBT
 - Defined a first draft of generic interface to the ECS:
 - Generic ECS command with all necessary info for the core

Command Field

Data Field

(only on multi-byte data operations)

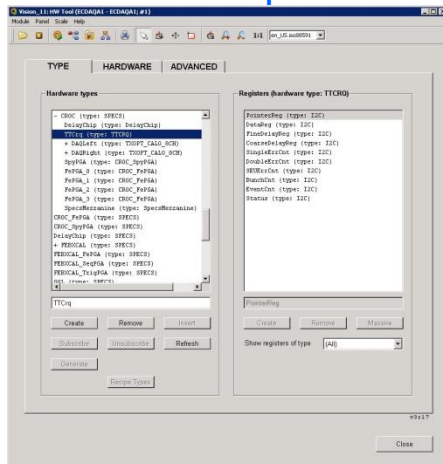




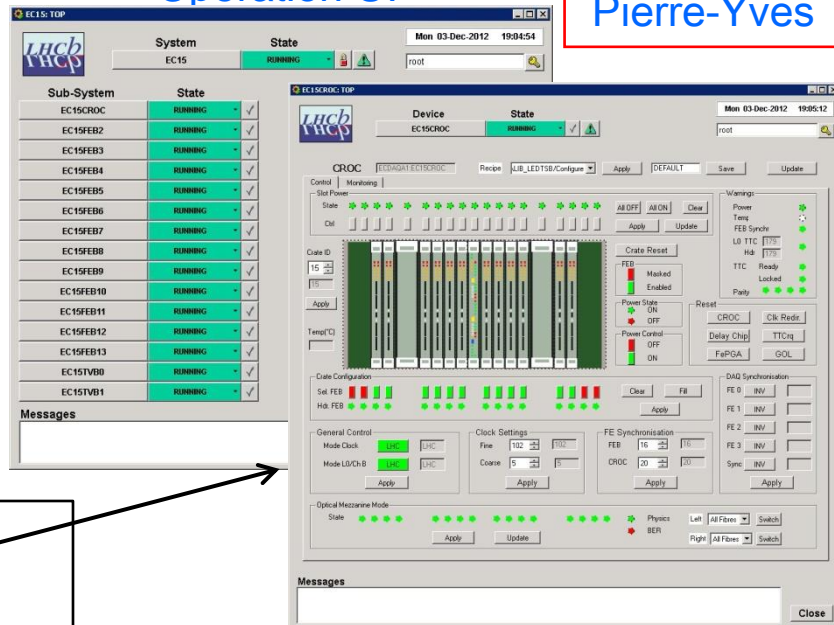
Current developments: software

Clara, Luis, Pierre-Yves

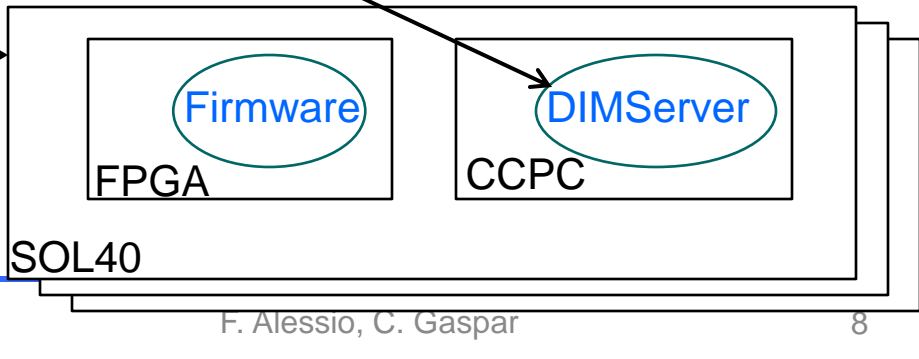
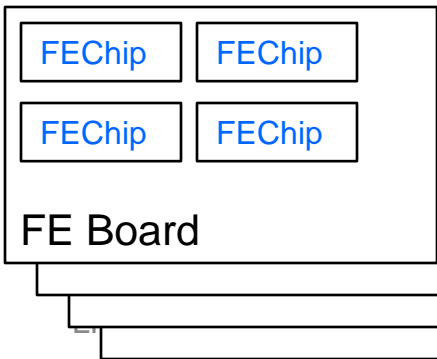
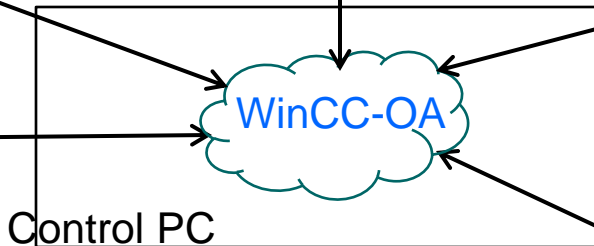
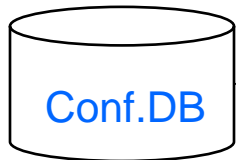
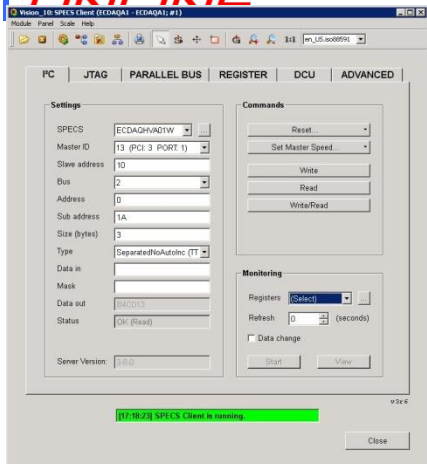
HW Description UI



Operation UI



Test UI



GBT Link



Current developments: software

- Will be centrally provided
 - Low-level libraries and command-line tools for the PC of the SOL40
 - Will allow accessing the different FE chips
 - A DIM server running on the SOL40 PC
 - Will implement higher-level commands to configure and monitor the FE
 - A WinCC-OA component(s)
 - Providing the high-level description and access of all electronics components

Conclusions

- Developments for sub-detector Front-End are ongoing together with global software for Mini-DAQ and PCIe40
 - **Time wise software will move in parallel with firmware over the summer**
 - As soon as we have a qualified part of the firmware we'll start working on the software
 - Most of the tools are (basically) already there
 - Needs adaptations from current LHCb ECS, but know-how is there
 - Always very quick response
 - **Sub-detectors are very much encouraged to come to any of us to discuss implementations, solutions, examples etc.**
 - Even better if you have something as realistic as possible
 - Even better if you can test something with us during or after the summer
- Note from the Wise Man: please, try to follow the specs as much as possible...
unconformities are a pain to handle... ☺