Draft 2

ALICE Review: 1 April, 2015

SAMPA, MPW2

Reviewers: Paul Aspell, Hans Kristian Solveit*, Marek Idzik*, Werner Riegler, A. Kluge
SAMPA team: Hugo Hernandez*, Bruno Sanches*, Arild Velure*, Sohail Mahmood*, Marco Bregant*, Marcelo Munhoz*, Danielle Moraes*
TPC representatives: Christian Lippmann, K. Read*, C. Britton*, K. Münning*
MCH representatives: Alberto Baldisseri*, H. Borel*, V. Chambert

*=remotely connected

Introduction

The aim of this review was two-fold:

- Review the responses of the SAMPA design team to the referee questions from review MPW2 part1.
- Review the design and physical implementation for the MPW2 for a submission in April.

Review material

https://indico.cern.ch/event/382908/

Review summary and preconditions before submission

The progress on the analog design/layout and the structured way of responding and acting to the referee questions/suggestions on the analog part was very positively acknowledged. Due to the improved implementation and presentation, the referee questions went into more detail and suggestions for further simulations were given, with emphasis on the noise behavior in the TPC operation mode.
A large number of measurement results have been presented and the progress on the MPW1 measurements was acknowledged. It was appreciated that for some measurements the results of several measurement campaigns were summarized, for other performance parameters, the detailed measurements are still outstanding.
Concerning the digital implementation, it became apparent during this review that the implementation is far from finalized and the status is incompatible with a submission in April. The functional implementation has not been finalized, the functional verification has only been started partially and the physical implementation has not started yet.
This will result in an additional delay to the already delayed MPW2 submission, originally planned for November 2014 and rescheduled to April 2015.

It is suggested to increase the coordination between the different designers and testing laboratories. The SAMPA management needs to propose a way to improve the man power situation and propose a schedule compatible with the TPC/MCH developments, considering that a second full ASIC submission (MPW3) might be required before production.
In summary, the review panel leans towards the preparation of the full ASIC submission with all required simulations performed before, as suggested by the review panel, including full system, post layout functional simulations. However, as substantial changes have been applied to the MPW1 analog and ADC circuits the submission of 1 or 3-channel analog-only (front-end and ADC) test circuits in addition to the full system submission could be considered. Before the actual submission another review needs to take place.

MPW1 test results in different institutes and their impact on the MPW2 design (M. Bregant)

MPW1 test results in different institutes and their impact on the MPW2 design (H. Hernandez)

The power consumption of MPW1-chip1 was presented. However, the test board did not allow direct measurement and about 1 mW needed to be subtracted from the obtained values corresponding to auxiliary components on the test board, resulting in ~9 mW. Simulations predicted 6.8 mW. Measurements by a different test laboratory showed a lower consumption. It needs to be verified whether this is due to different operation conditions or due to a strange operation mode of the ASIC.
The reviewers suggest clarification why there is a spread between simulation and measurements and make this measurement with several ASICs. The reviewers suggest to verify that all test boards operate with the same bias voltage, as this has an impact on the power consumption and also suggest to verify the process map for this MPW to evaluate the process parameters of this MPW.
An undershoot of the pulse shape in the mode 20/30mV/fC-negative was presented. The reviewers asked whether this happened in the last stage, which was confirmed. Furthermore, it was asked why it did not show up in the simulation. The design team responded, that this behavior is initiated due to the non-ideal behavior of the IO pad and bond wire. However, at time of the submission no correct models of the IO pad were available. The simulation shows this behavior now and for MPW2 the situation has been corrected.

The peaking time measurements have been shown and were found to be in general too short. According to the design team the measurement probes have an effect in the measurement reducing the pulse length. It was reported that simulation does not show the difference in peaking time. Also, since the design is made for a load of 10 pF (input to ADC) it is not clear why the probe loading of 10 pF should change the peaking time. The review panel suggests to investigate this discrepancy before changing blindly the peaking time. It also was reported that different laboratories see different peaking times and that this is due to

different peaking time definitions. The reviewers suggest the SAMPA team defines the measurement procedure/definition and coordinates the measurements in the different places actively. It was mentioned that this effect could be due to the different driving strength of p/n transistor acting as source/sink.

Sometimes, but especially for measurements on gain and linearity (slide 11 to 16), only single chip measurements were presented, whereas the reviewers suggest to present plots for several ASICs and channels.

On the measured power supply rejection ratio (PSRR) the referees wanted to know why the simulation is better than measurements and why the simulations plots show oscillatations at high frequency. The simulated (and measured) PSRR is very good (~30dB peak at ~1MHz), if possible it should be improved (slide 17-18)

It was commented in some plots (simulation/measurements) that it was not clear with which capacitance the input has been loaded and thus comparisons are not evident, particular on the noise tests (slide 18 -21). The presented measured noise values for the TPC case exceed the specifications and miss the measurements by the TPC and Dubna team. Furthermore, no tests with a TPC chamber have been presented. It was questioned whether the TPC case simulated noise curve is correct as it has a negative slope for capacitor values from 0 to 15 pF. From the discussion it is not clear whether the noise ENC was properly simulated - it should be verified (slides 19-21). The reviewers request a verification/explanation and would like to understand the noise contribution of different stages. The measurements plots have a shape more according to expectations. In slide 19, giving the MCH case noise, the noise specification is marked wrongly. It was stated that the increased noise compared to the specification and higher than simulation is due to the low PSRR and the test environment. The reviewers commented that the situation needs to be specified and that the situation in the test laboratory will always be better than in the experiment. It was also stated by the TPC team that the effective capacitance including the cabling seen by the front-end might be bigger than 18 pF.

I/O pads have 0 Ohm series resistance. Extreme care when handling needs to be taken.

The reviewer would like to know the gain sensitivity, peaking time, pulse shape to capacitance (simulation and measurements).

The crosstalk (slide 22/24) needs to be measured with the expected detector capacitance connected. It was reported that “further away neigbours” also have similar crosstalk reaction and the reviewers commented that this points to an effect due to coupling via biasing lines or power supply and can be improved by decoupling. The different way of cross talk presentation between MCH and TPC did not allow a comparison. It has been positively remarked that for the MPW2 design the input impedance has been reduced.

It was remarked that for the ADC only dynamic measurements where shown, but also static measurements are important, including INL and DNL. For the dynamic measurements signal with the expected frequencies (MHz) need to be evaluated. It was reported that the internal decoupling capacitance is 70 pF only, which is considered much too low. ADC performance the presened ENOB (7.8) is too low and shown for very low input signal frequency - it needs to be understood (slide 29).
Measurements of INL and DNL at default experimental sampling frequency should be done for better understanding. ENOB should be measured dynamically scanning both: sampling frequency and input frequency.

It was reported that under certain conditions oscillations were observed (slide 32-35), however the referees remarked that the source of these oscillations have not been located sufficiently. It is important to understand the source and to evaluate whether the ASIC is operated with too little margin with respect to the internal circuits or with respect to the external environment. The design team noted that with a refined test board these oscillations were not observed. Further tests and simulations also including non-ideal operation points (high/low VDD, temperature) need to be conducted. It is not clear why the oscillations only occur for the negative polarity and it was suggested to investigate in the preamplifier. It was pointed out that the oscillations are sensitive to the operation voltage which according the reviewers is an indication that operation parameters are on the limit. Slide 9: pulse shape for negative polarity is close to oscillations. Is it related with slide 32 - oscillations in chip3 for negative polarity? This situation needs to be understood and corrected. Except problem with oscillations (slide 32) the measurements of pulses (slide 33) should be compared quantitatively with simulations - are the shapes and amplitudes in agreement with expectations?

Chip3 contains front-end and ADC. The measurements of the whole chain - digital ADC response to injected charge – were not presented and need to be done. In fact, only quantitative measurements of the whole chain can demonstrate whether the signal processing in a single channel is correct.

The reviewers commented that the transistors do not work in saturation mode and are thus susceptible to oscillations and that a bias networks with many stages is sensitive to pickup.

It was presented that at present the decoupling for the front-end has been calculated and sufficiently implemented but the decoupling for the ADC is still missing.

Response to the questions of the reviewers, as summarised in the review report (H. Hernandez)

Below is the list of the reviewer comments to the responses:

Slide 9: In IBM gain was so small, in TSMC gain is higher, with these results it might be OK.

Working in class AB, means not linear. Results are good, but with some process variation the positive cancellation might not be there anymore. Designing transistors close to saturation voltage might cause unpredictable behaviour. Concerning the underdamped behaviour for negative pulses (with MPW2 simuation seem now correctly damped) it needs to be taken care that all transistors are be in correct operation region and not close to border.

Slide 17: simulation results of transient results need to be shown, not only DC. Matching simulation with several transistors only useful with transient response especially working in the AB mode.

Slide 20/21 is not sufficient as also wave forms are needed.
Slide 20 & 21 is the same. MCH is missing.

Slide 26: Min. size capacitors should still work, adding additional buffer per ADC is possible but creates slightly different condition for each ADC.

Slide 29/30 same table

Slide 34 presently only 80 pF decoupling per ADC channel, too little.

In general more simulations are needed: 25% less power consumption, what about noise linearity —> Linearity is the same as it comes from shaper, only output stage of buffer is redesigned as now 10 lower capacitor to drive.

The DAC capacitances (power, size) have been decreased a lot - good improvement

Additional reference buffer was added in each channel - it adds additional power - if acceptable OK. The reviewers think that realistic simulations (multichannel, bond effect, post-layout, decoupling capacitors) should be done to verify quantitatively the performance of the whole system.

More measurements are available, but some issues are still not correctly understood. In places simulation results do not match the measurement results. It is not clear whether all reasons are understood, that could cause concern, which can destroy a chip, like oscillations.