SAMPA: MPW1 test results their impact on the MPW2

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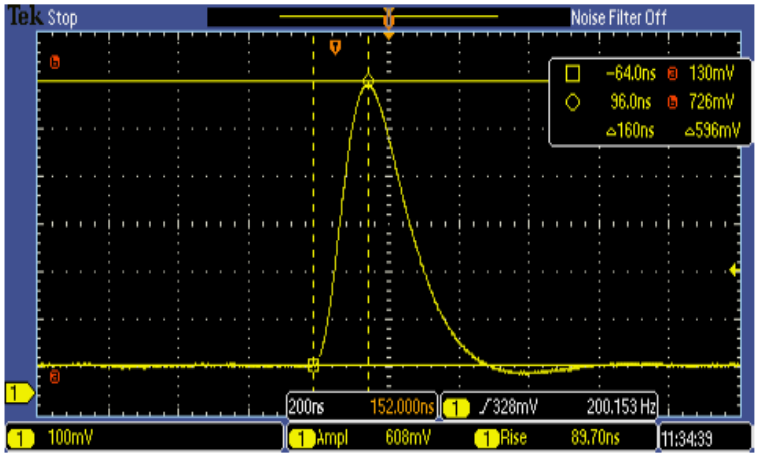
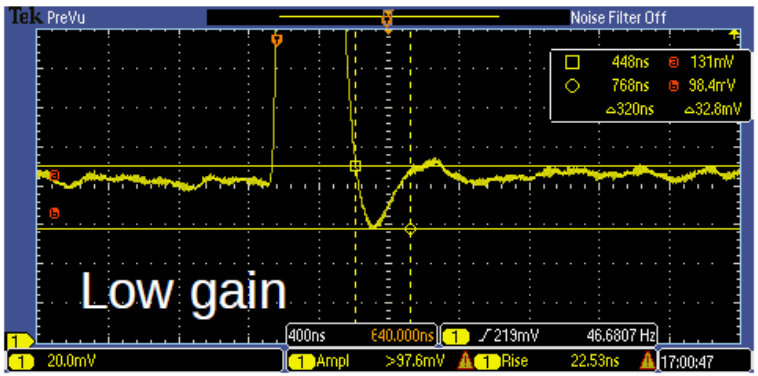
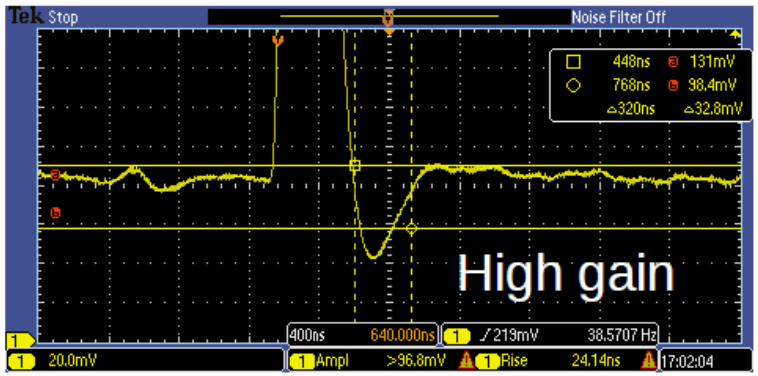
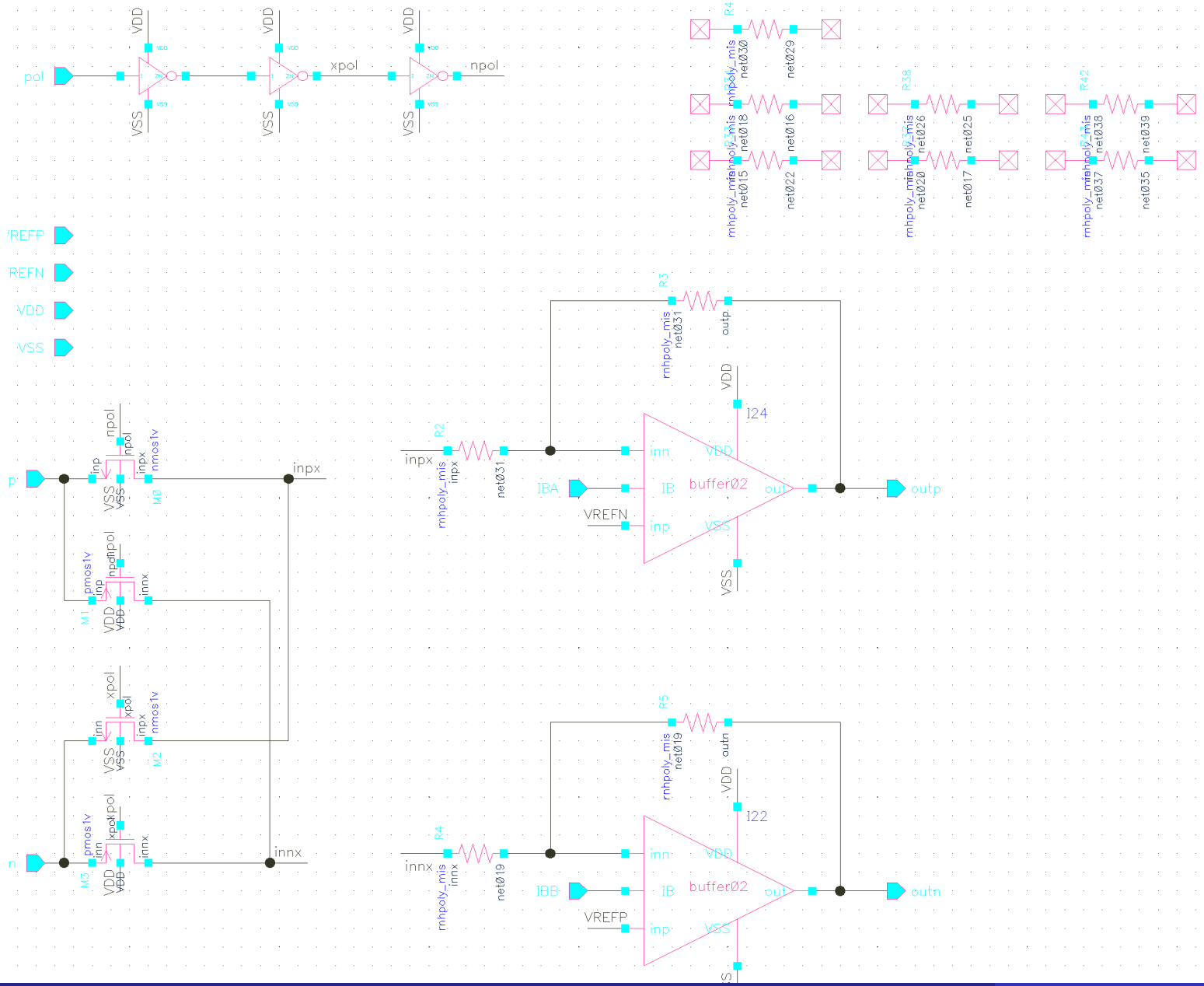
Negative Polarity undershoot





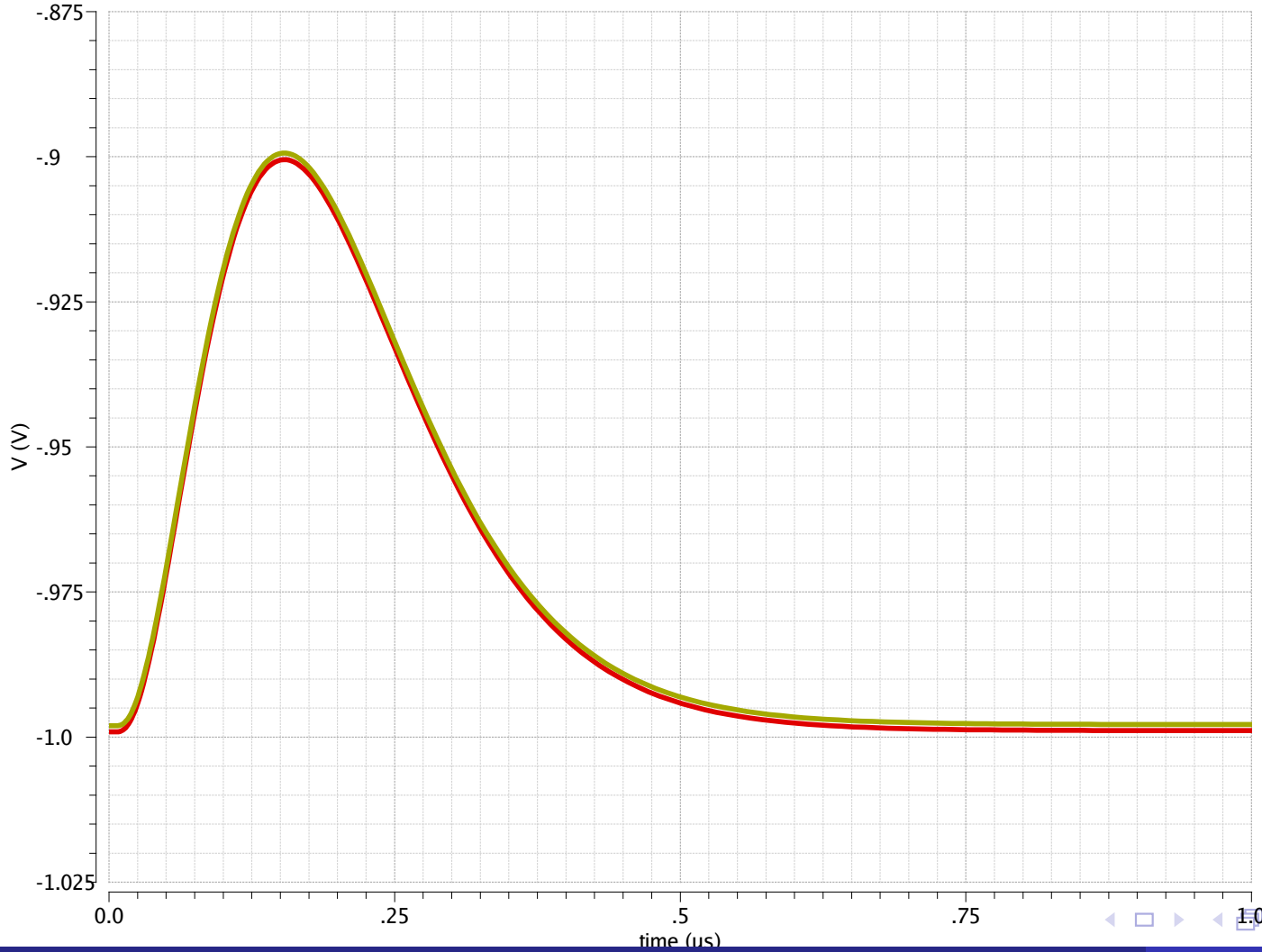


Negative Polarity undershoot: Solution



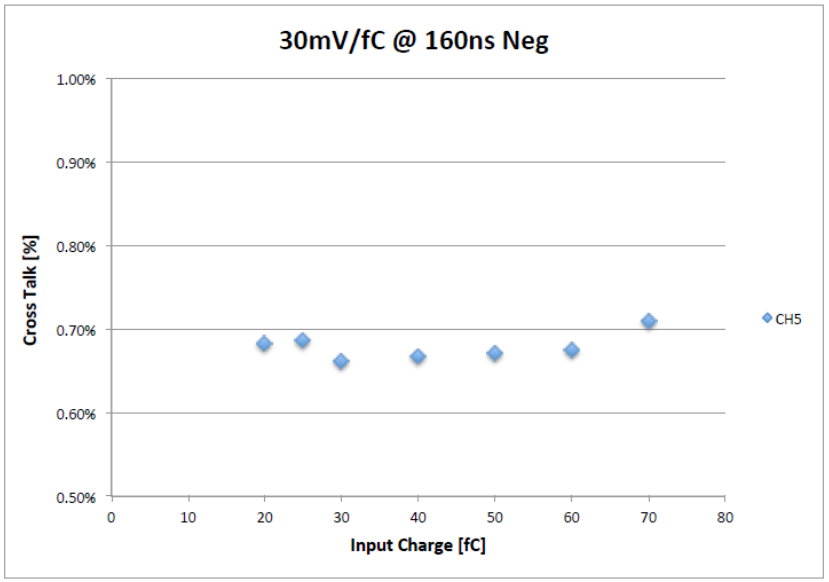
Neg/Pos Polarity undershoot: Solution 160ns@30mV

view: extracted Input charge=5fC



Crosstalk : 0.7%

xTalk vs Input charge (4<->5)



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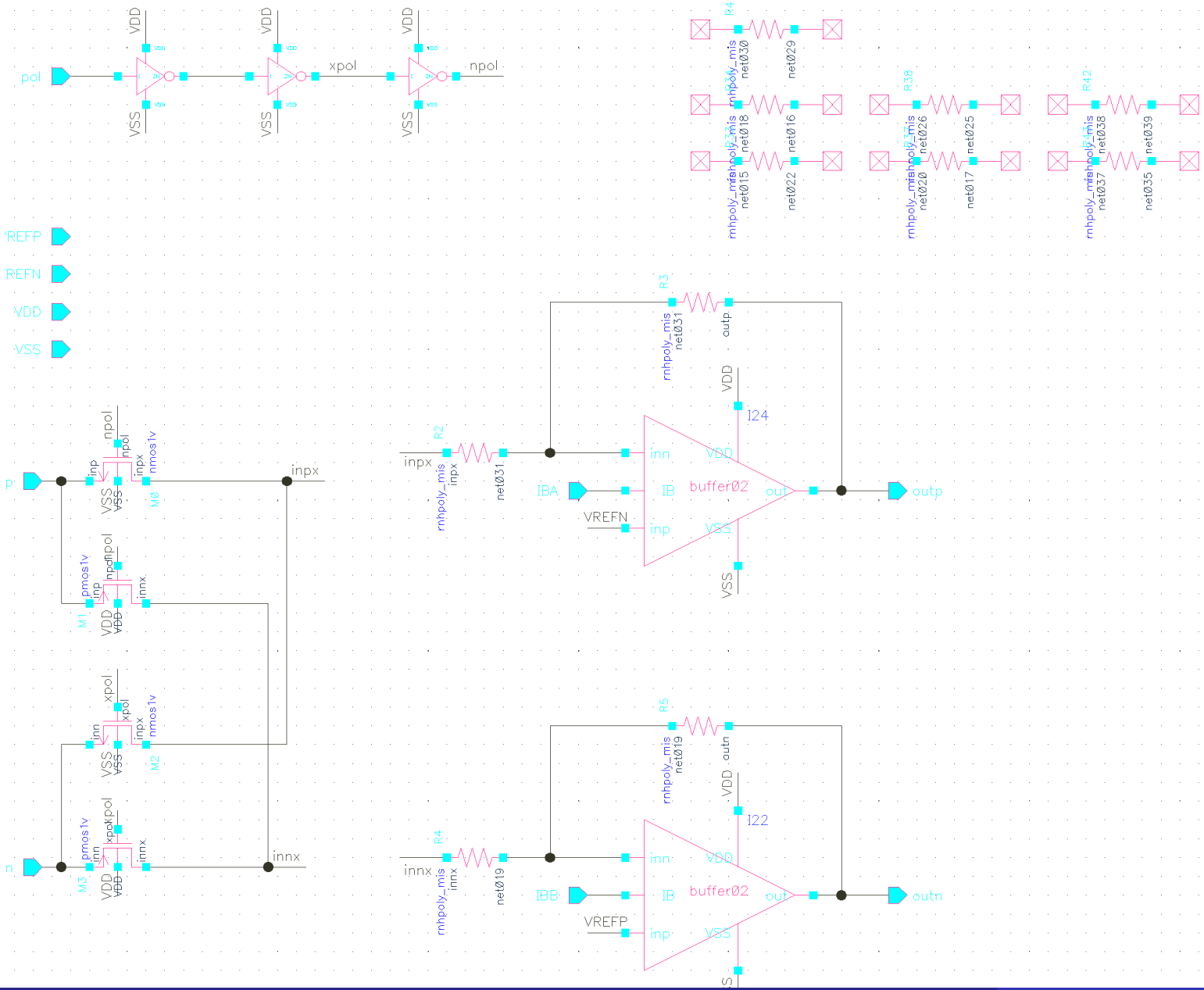
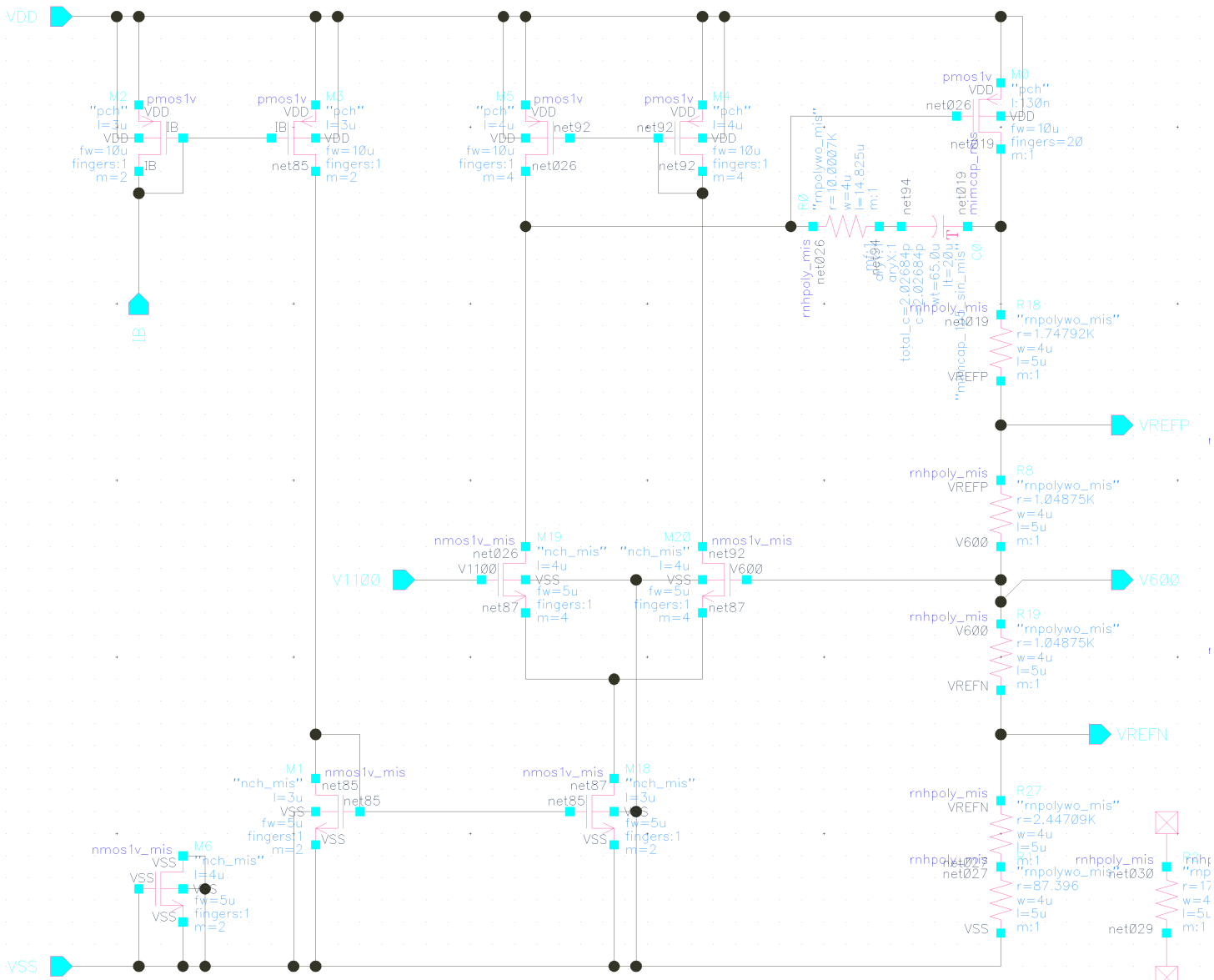
Crosstalk: partial Solution



Crosstalk: partial Solution

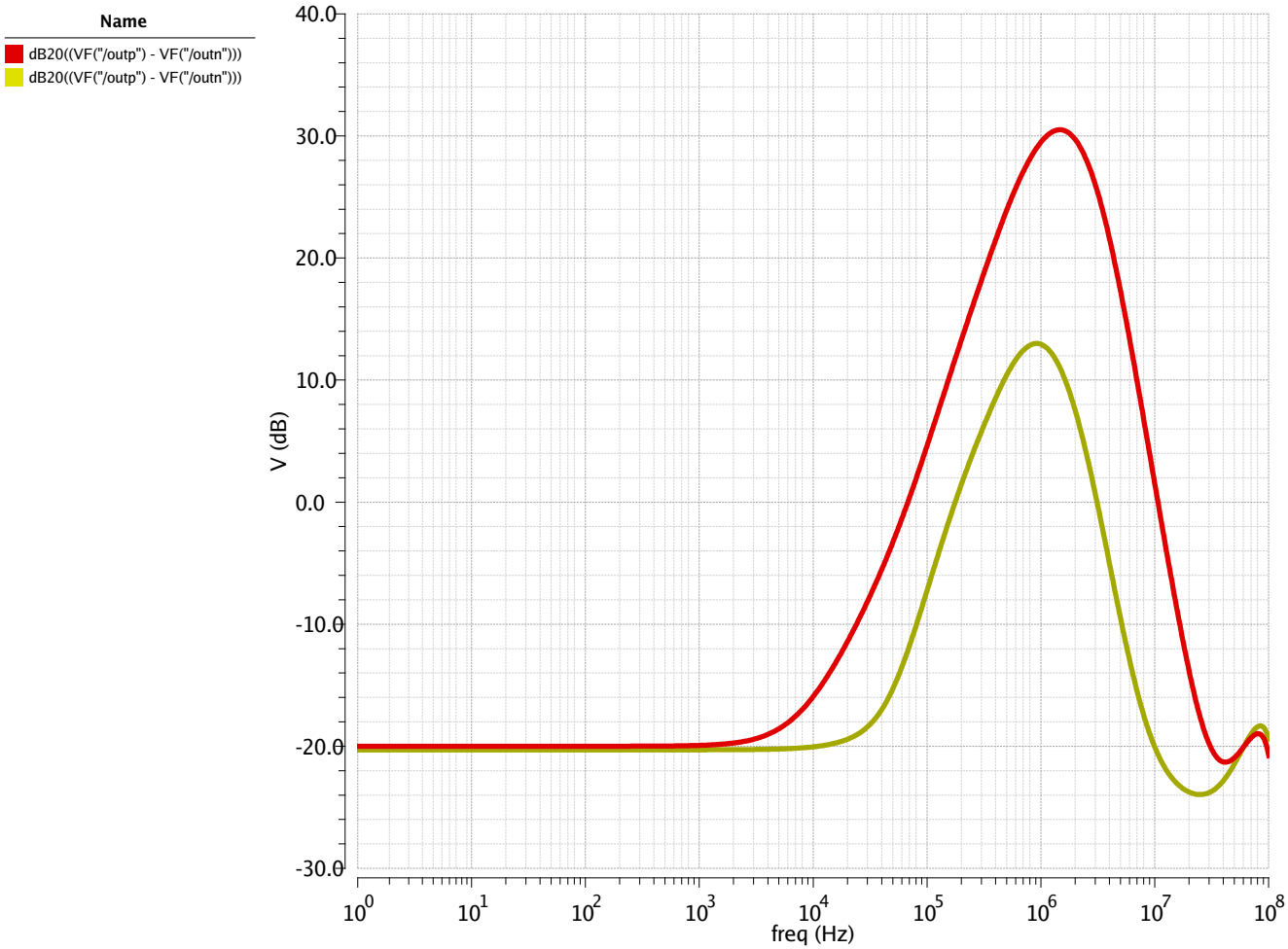


Crosstalk: actions

- Simulations including more package effects: Mutual inductance
- Reduce the bond-wire length: Chip01 (MPW1) presents long bondwire ($\approx$ 5mm).
- Minimize crosstalk due to IR drop and finite PSRR.
- The GBW of the CSA was increased to reduce the input impedance (from 35Ω to 20Ω).

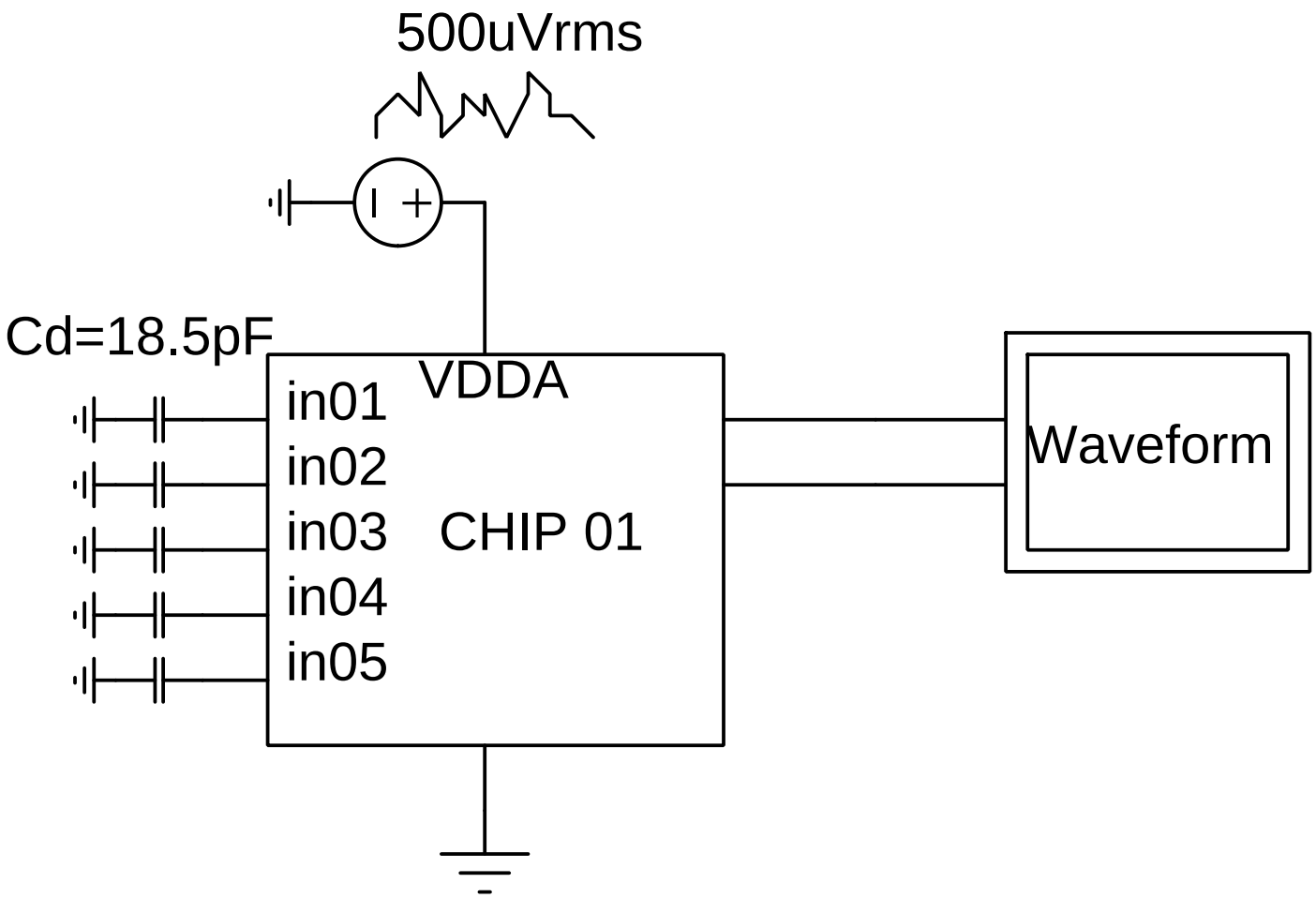
Chip 01: Power Supply Rejection Ratio (PSRR)

160ns 30mV/fC $\Rightarrow$ RED
300ns 4mV/fC $\Rightarrow$ YELLOW;



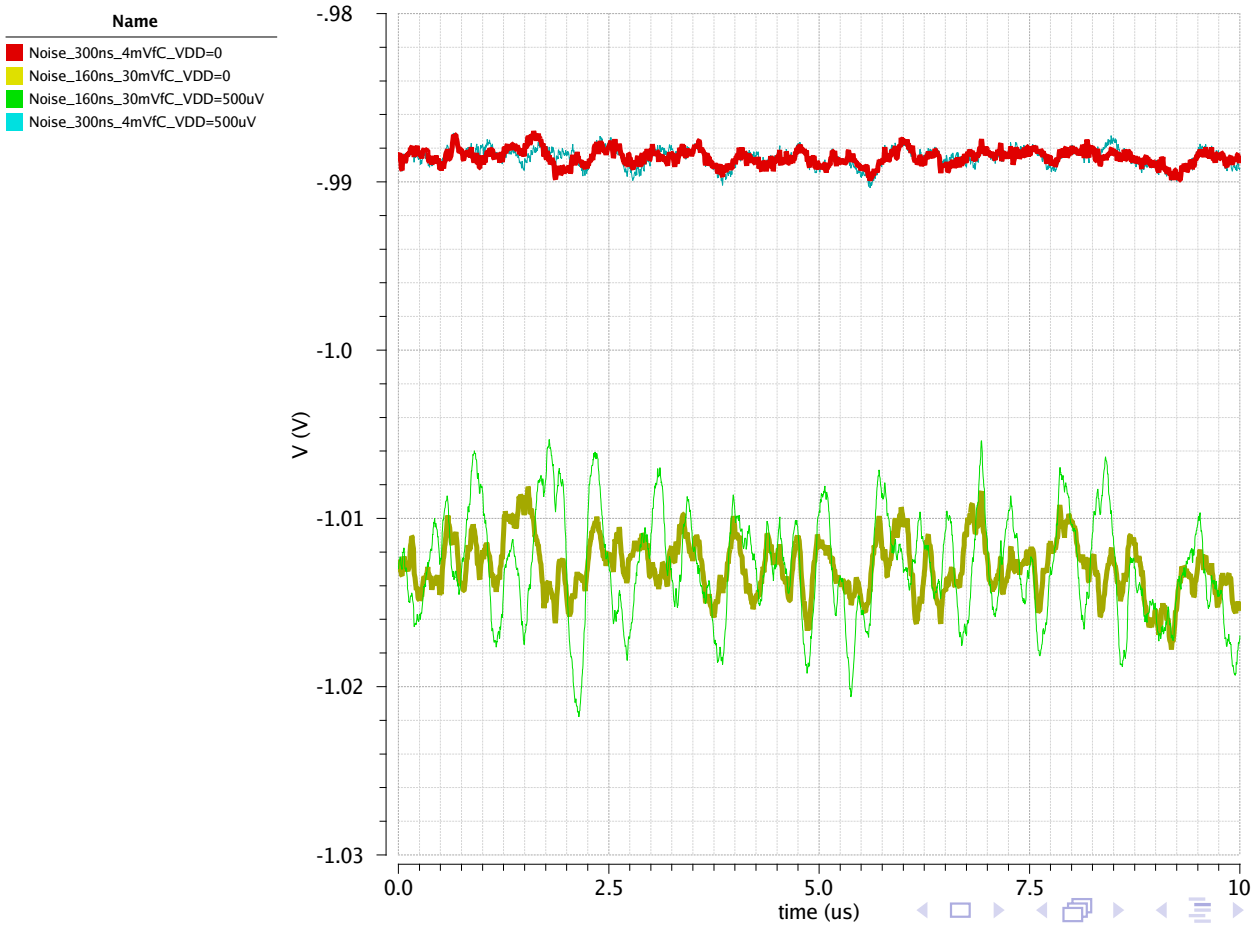
Trasient noise simulation

Fmin=1kHz Fmax=100MHz



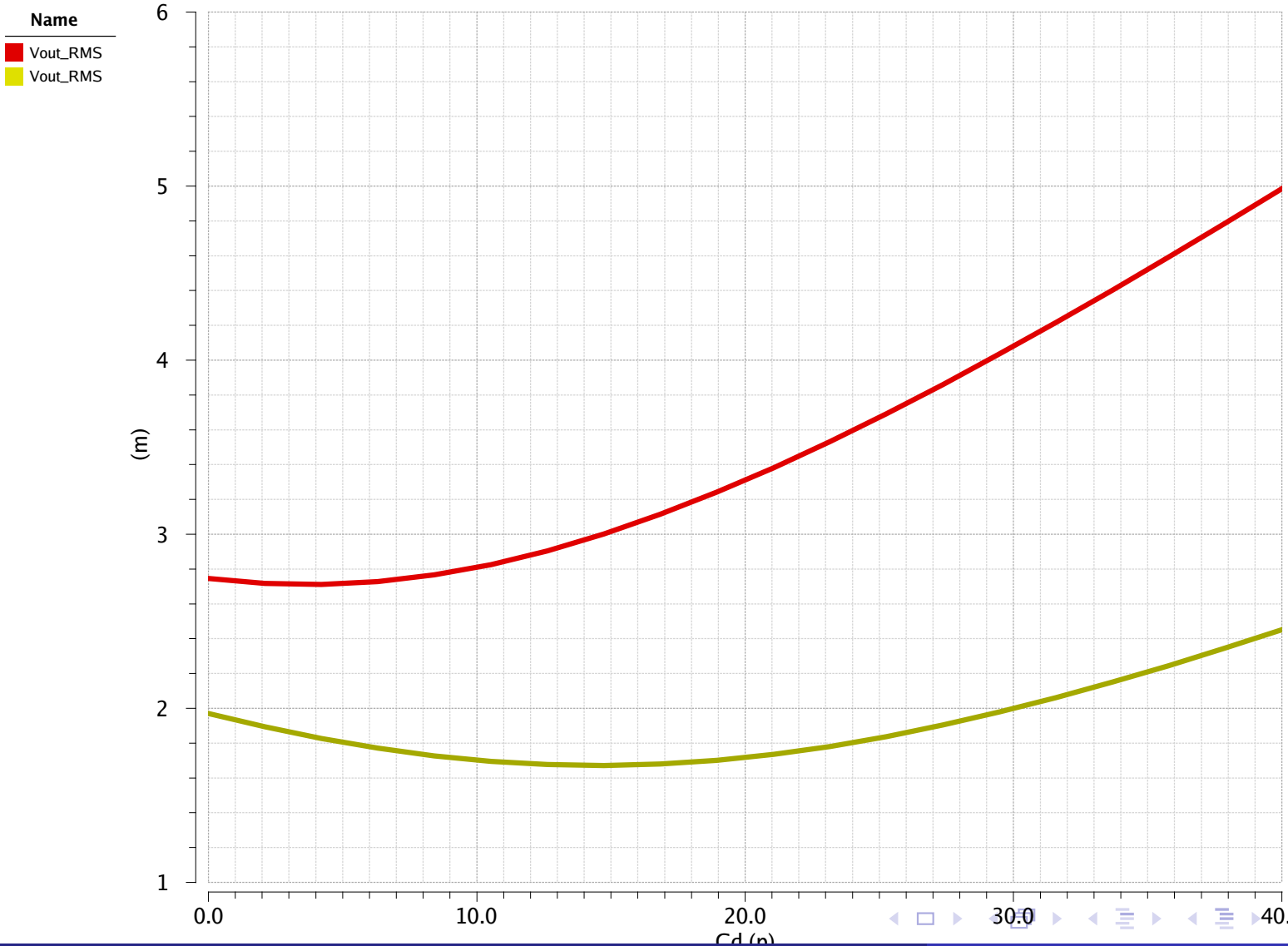
Result: Trasient noise simulation

Supply Voltage Noise	VDD=0 Vrms	VDD=500 uVrms
300ns 4mV/fC	472 uVrms 736e	528 uVrms 823e
160ns 30mV/fC	1.78 mVrms 370e	3.21 mVrms 667e

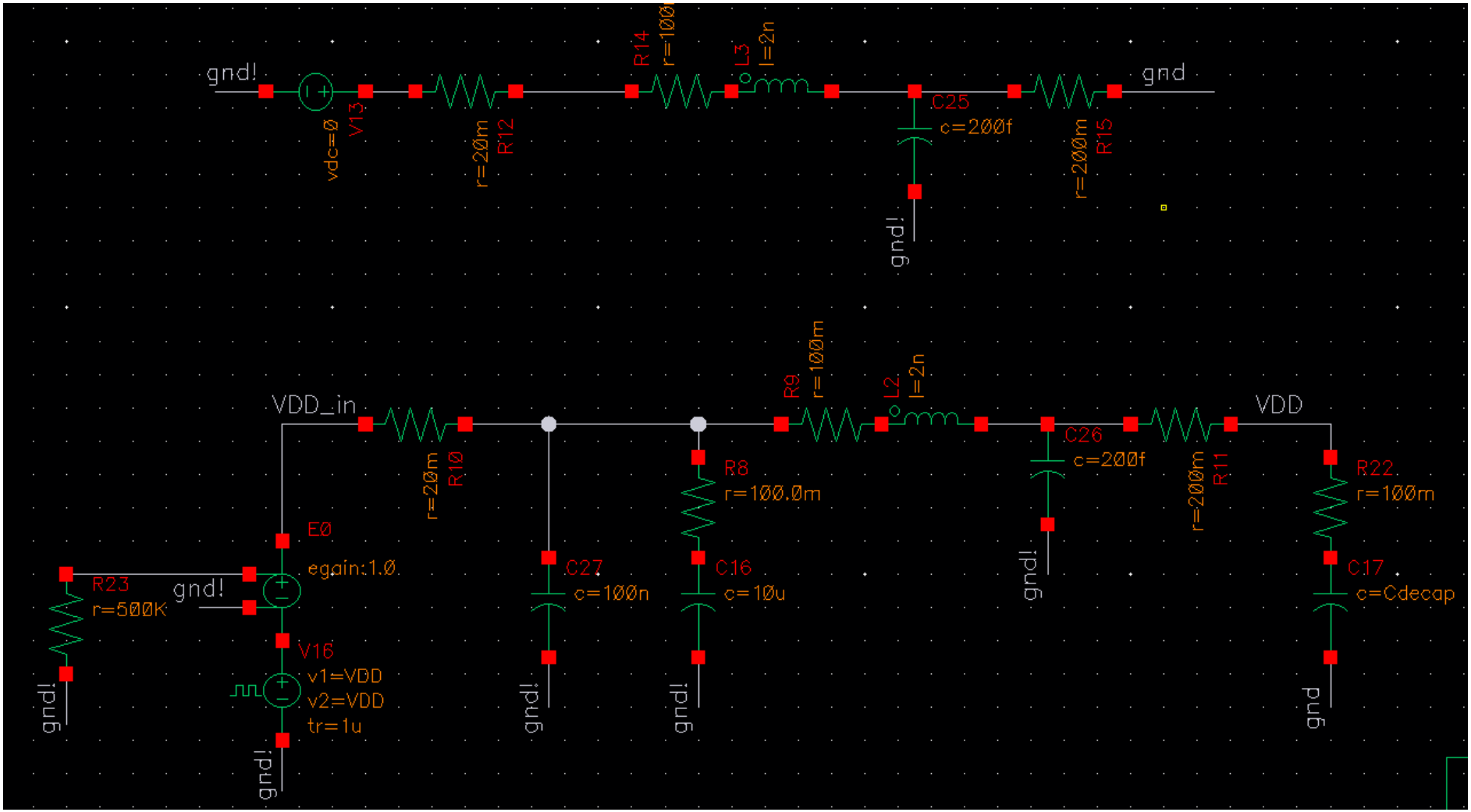


Vrms Vs Cd 160ns@30mVfC

RED: with VDD noise YELLOW: without VDD noise



Noise model of the supply voltage



Front-end Output noise VS DeCap (per channel)

Configuration:160ns@30mV/fC
view: extracted
Number of channel: 16

Cap	Vrms
10pF	3.5mV
100pF	1.95mV
150pF	1.84mV
250pF	1.84mV

from MPW1 to MPW2: what has changed ?

- Front-end: Non-inverter stage (undershoot problem, crosstalk)
- Front-end: CSA (reduce the input impedance)
- Front-end: All NMOS of the front-end was implemented with triple-well (noise isolation).
- ADC: custom cells of the digital part (TSMC cells were validated)
- ADC: asynchronous to synchronous (reduce power of the reference circuits)
- ADC: Capacitor Array (reduce power of the reference circuits)
- ADC: onchip reference buffer
- System: Bandgap, 0.6Vto1.1V circuit