Universidade de São Paulo

SAMPA MPW2 design review II

MPW1 test results

(a comprehensive overview)

M. Bregant

1/04/2015

Acknowledgments

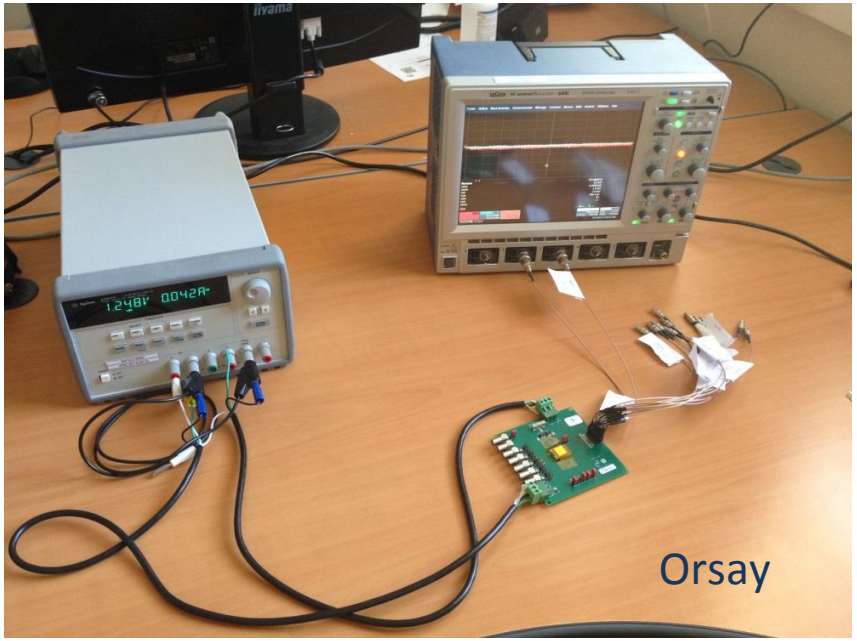
- Fr - Orsay : Patrice & the French colleagues
- No - Oslo: Sohail
- No - Bergen: Ganesh
- Ru – ISJR: Sergey
- Br – São José: Danielle
- Br – USP-Poli: Stelvio, Tiago
- Br – USP-IF: all the “volunteered” colleagues and students..

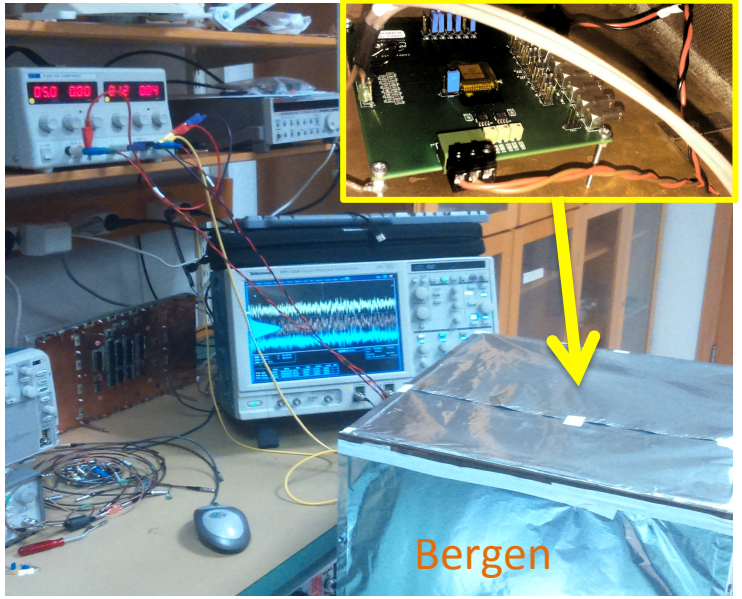
overview

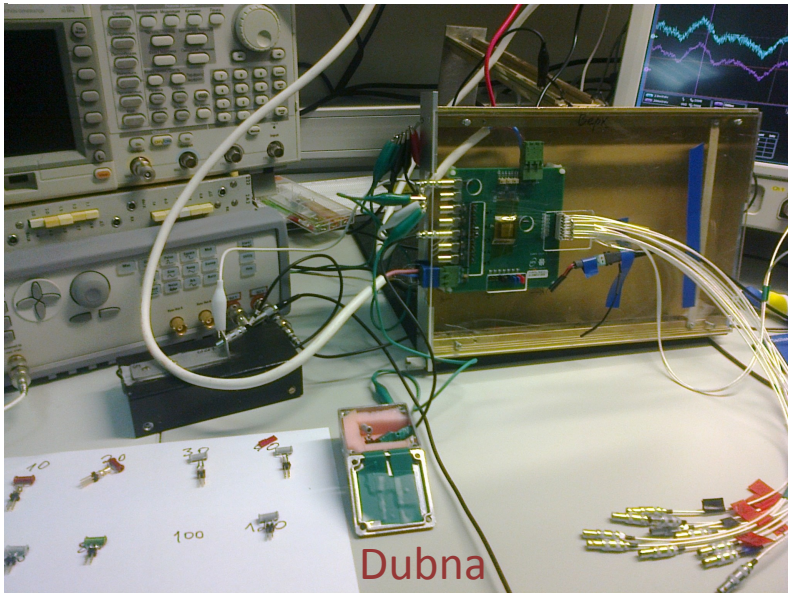
- Chip_1: “Analogue”, CSA+Shapers
  - Power consumption
  - Pulse shape
  - Peaking time
  - Gain value and linearity
  - PSRR
  - Noise
  - xTalk
  - “on the field”: reading a GEM detector
- Chip_2: “ADC”
  - Testability problems
- Chip_3: “FullChain”, CSA+Shapers+ADC+(dummy*)DSP
  - General functionality
  - Testability criticalities
  - Tests so far

+ still ongoing and coming soon

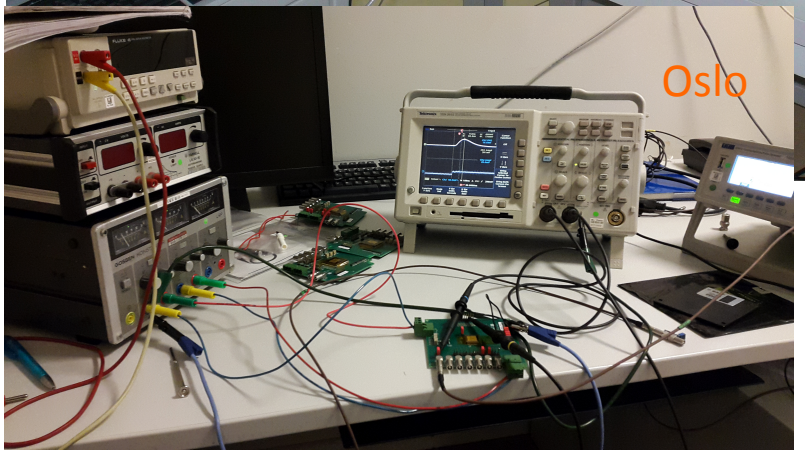
*The DPS is a partial, incomplete, prototype, which aim was to check compatibility with the other blocks


Orsay


Bergen

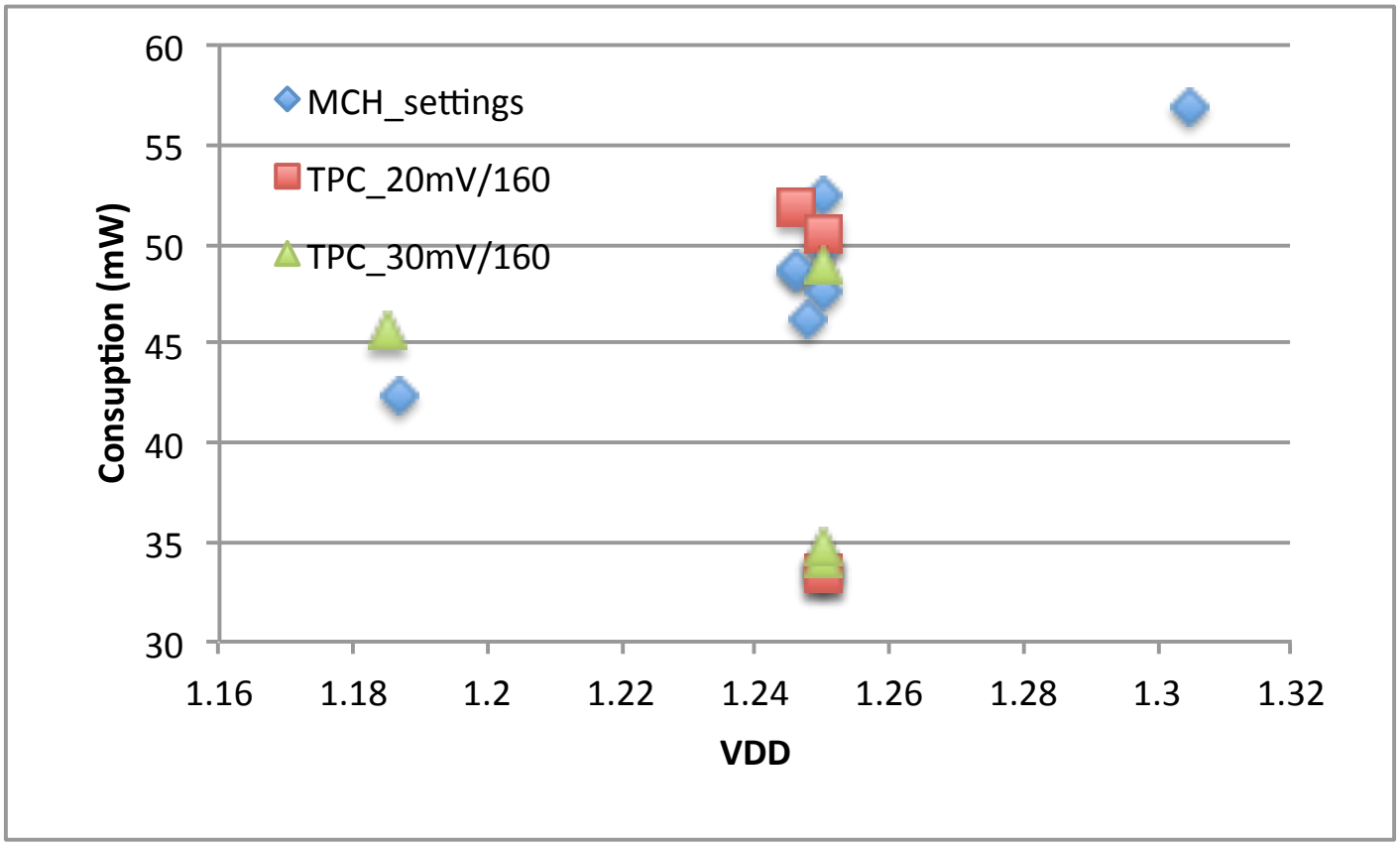

Dubna


São Paulo


Oslo

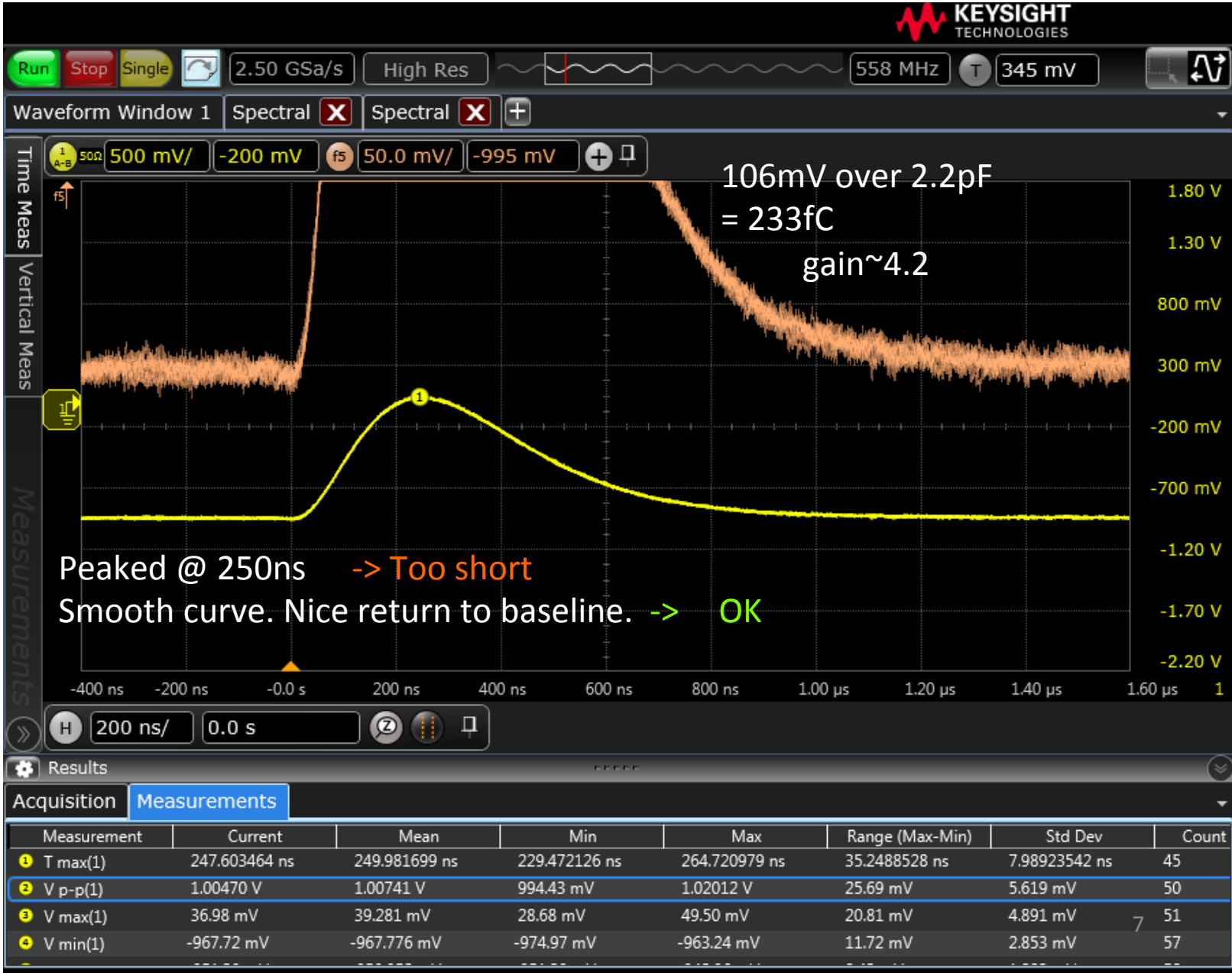
CHIP_1 “analogue”

Chip1: Power consumption

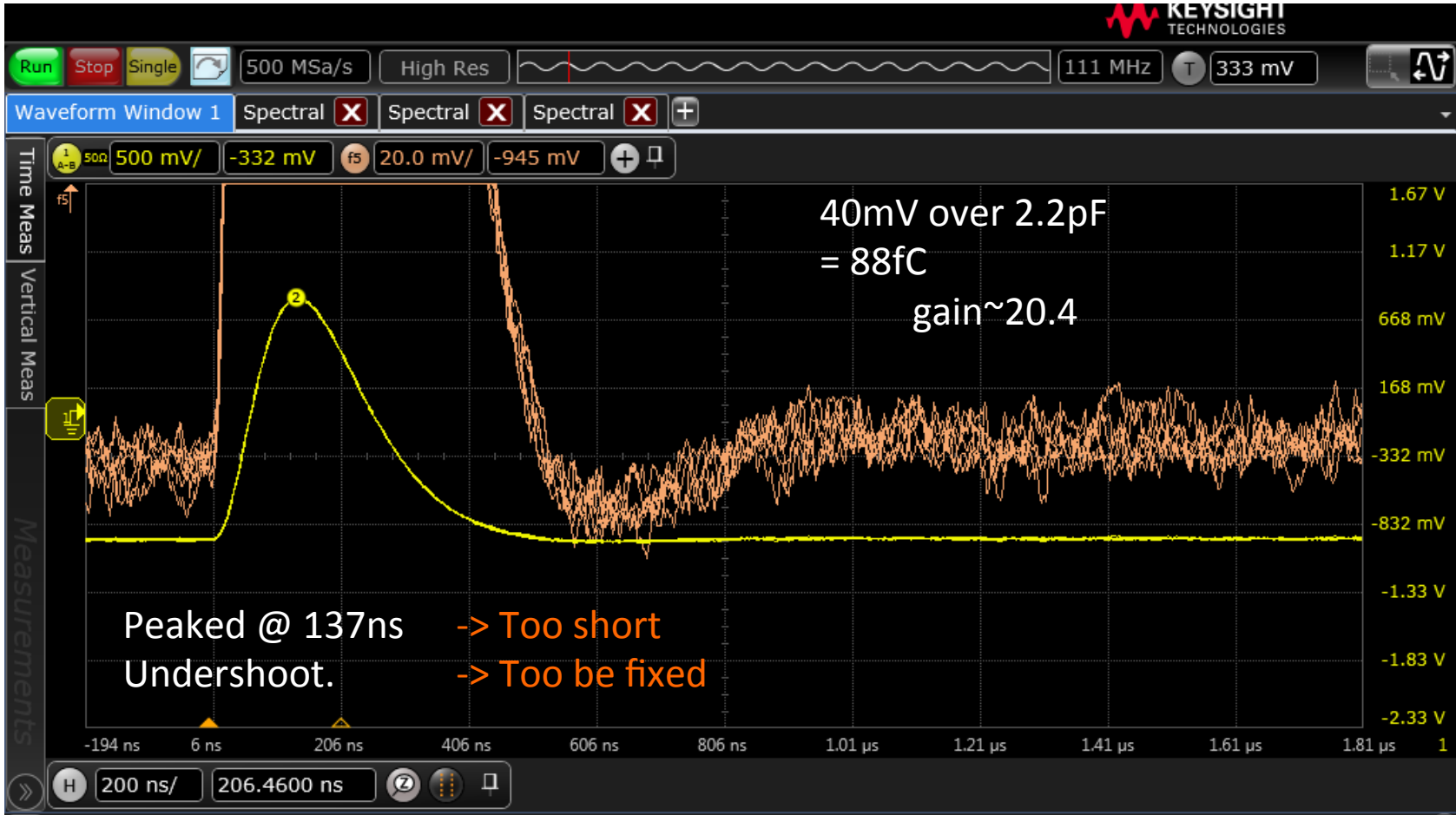


Power in the range of 10mW/ch. For some chips in the target of 6-7mW/ch
Almost there. Space to improve in MPW2

Chip1: pulse shape [4mV Pos]

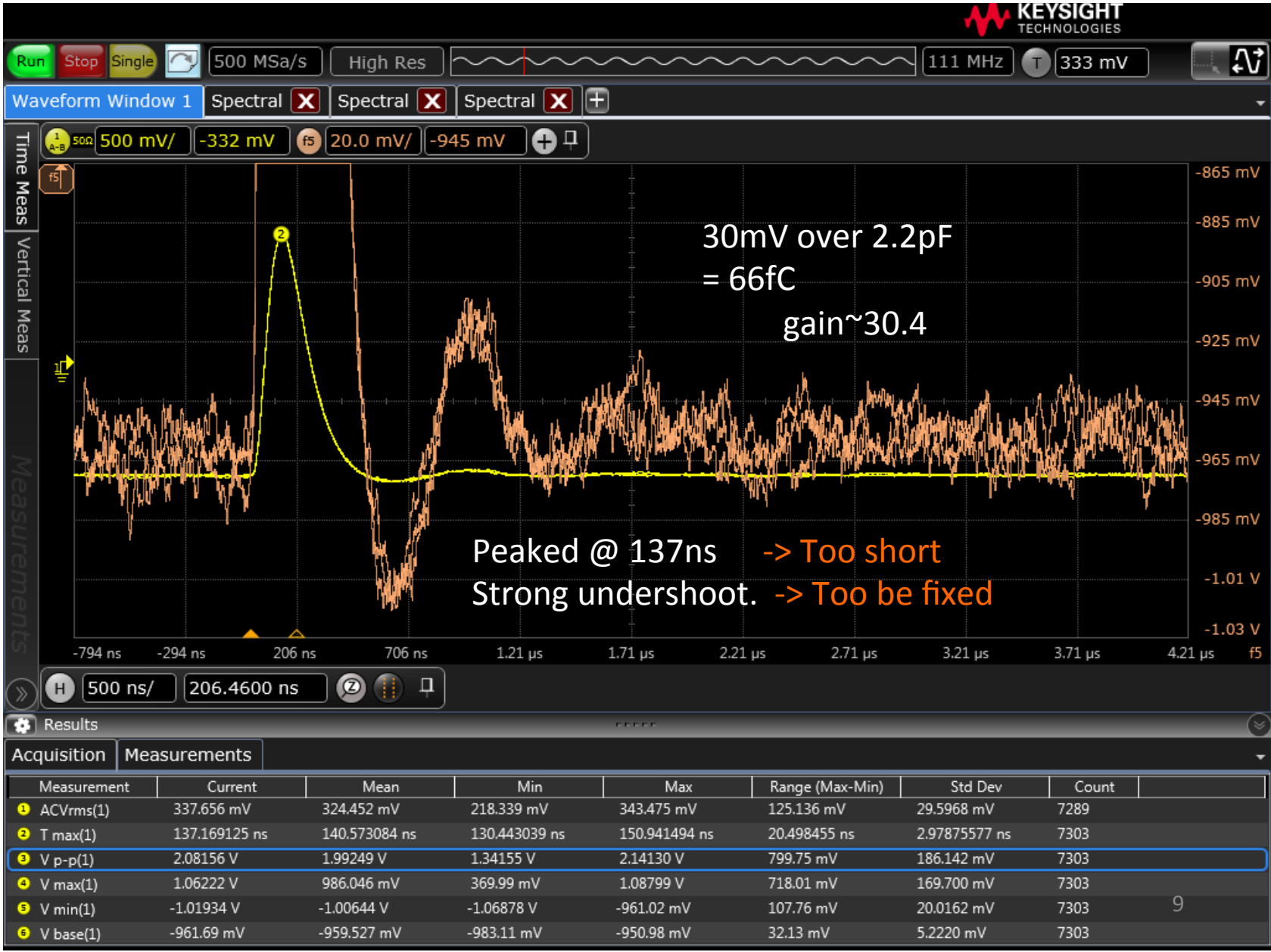


Chip1: pulse shape [20mV Neg]



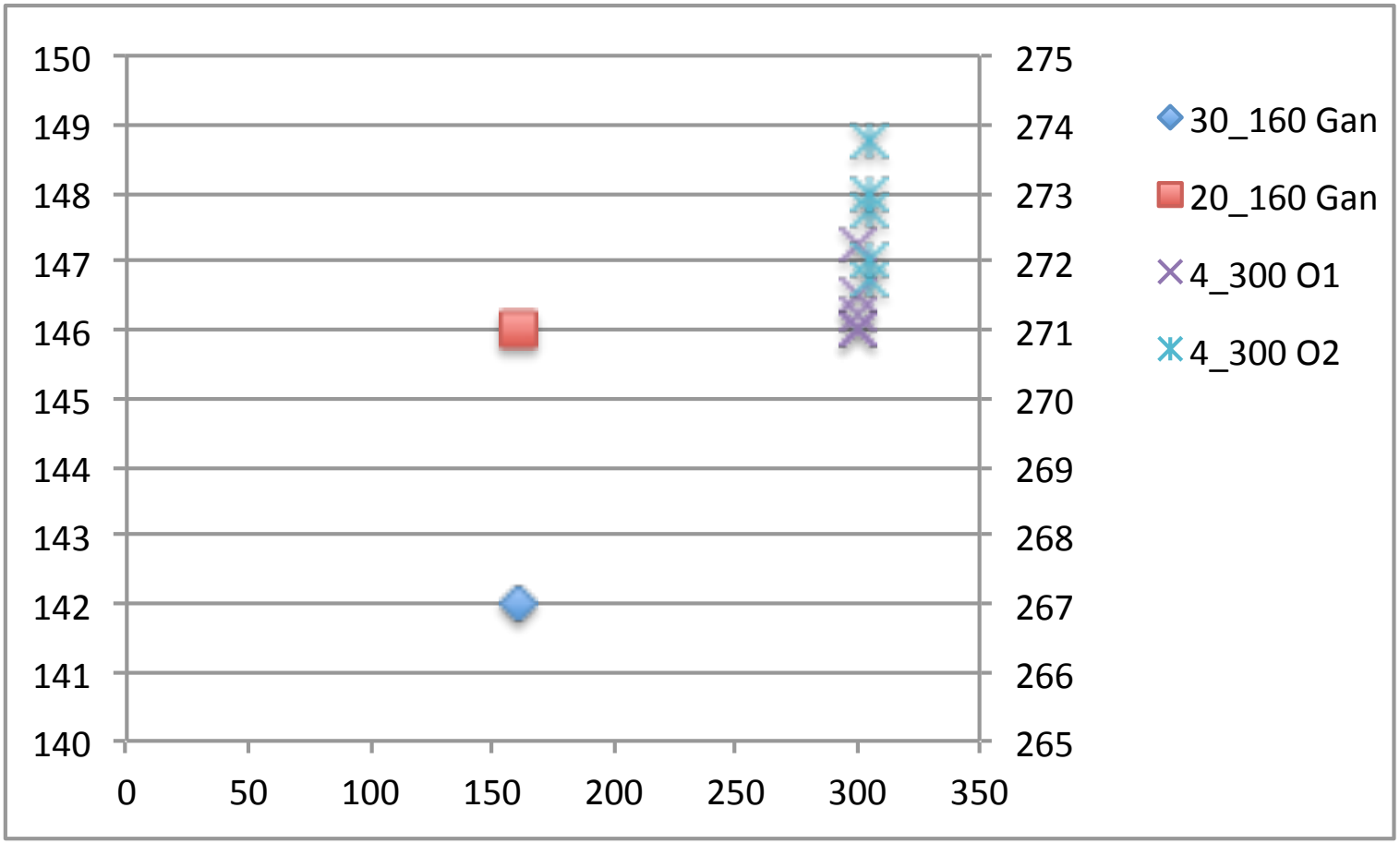
Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
ACVrms(1)	442.811 mV	442.929 mV	439.476 mV	448.126 mV	8.64976 mV	938.486 µV	14456
T max(1)	136.912157 ns	139.215774 ns	129.324274 ns	149.639959 ns	20.315685 ns	2.78257006 ns	14455
V p-p(1)	1.79593 V	1.79425 V	1.76891 V	1.82095 V	52.04 mV	6.6599 mV	14455
V max(1)	823.45 mV	822.539 mV	799.02 mV	841.27 mV	42.25 mV	5.2140 mV	14455
V min(1)	-972.49 mV	-971.714 mV	-987.96 mV	-958.26 mV	29.70 mV	4.1977 mV	14455
V base(1)	-950.98 mV	-950.432 mV	-961.69 mV	-940.28 mV	21.42 mV	2.3726 mV	14455

Chip1: pulse shape [30mV Neg]



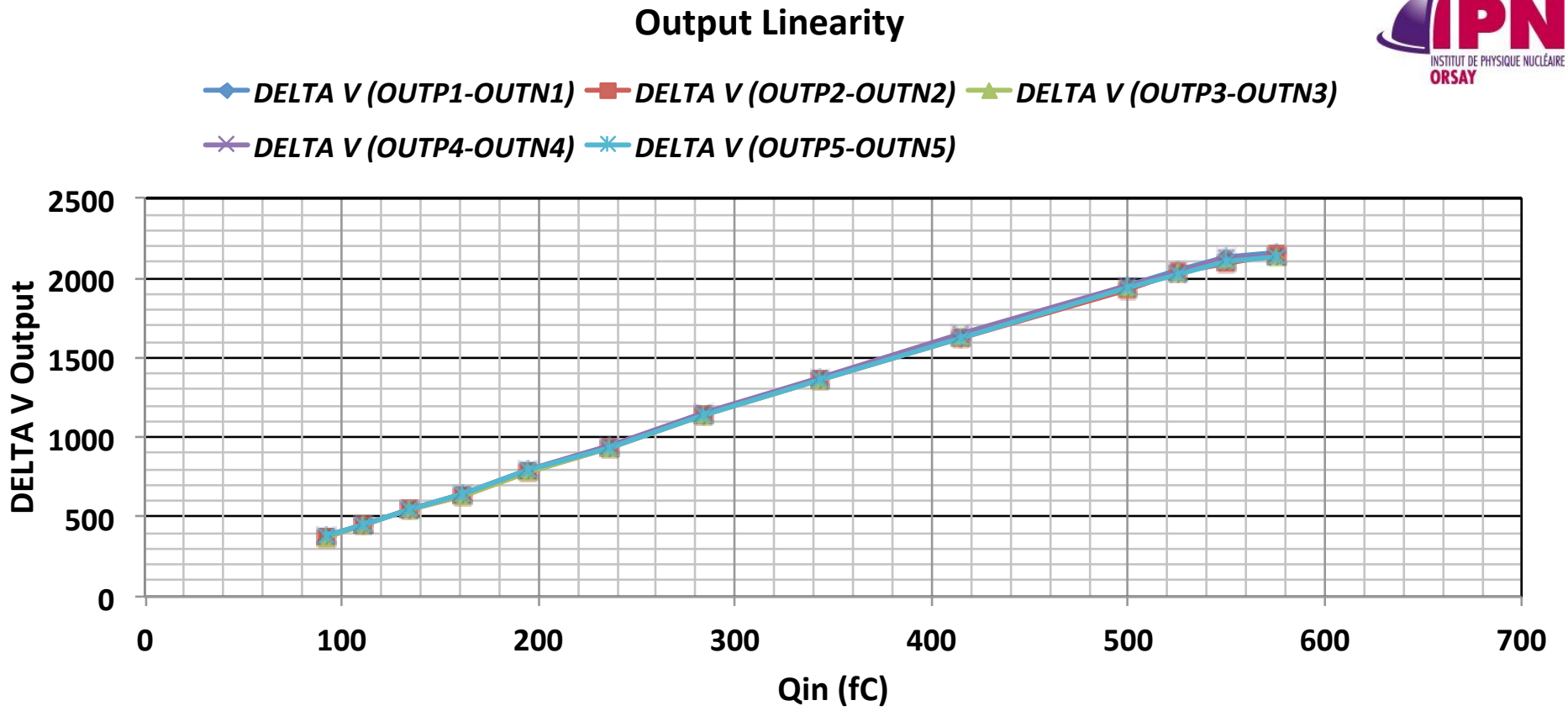
Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
ACVrms(1)	337.656 mV	324.452 mV	218.339 mV	343.475 mV	125.136 mV	29.5968 mV	7289
T max(1)	137.169125 ns	140.573084 ns	130.443039 ns	150.941494 ns	20.498455 ns	2.97875577 ns	7303
V p-p(1)	2.08156 V	1.99249 V	1.34155 V	2.14130 V	799.75 mV	186.142 mV	7303
V max(1)	1.06222 V	986.046 mV	369.99 mV	1.08799 V	718.01 mV	169.700 mV	7303
V min(1)	-1.01934 V	-1.00644 V	-1.06878 V	-961.02 mV	107.76 mV	20.0162 mV	7303
V base(1)	-961.69 mV	-959.527 mV	-983.11 mV	-950.98 mV	32.13 mV	5.2220 mV	7303

Chip1: Peaking time



Uniform among chips/channels systematically shorter
Parameters to be tuned in MPW2
Some lab-offset: different definition/measuring protocol

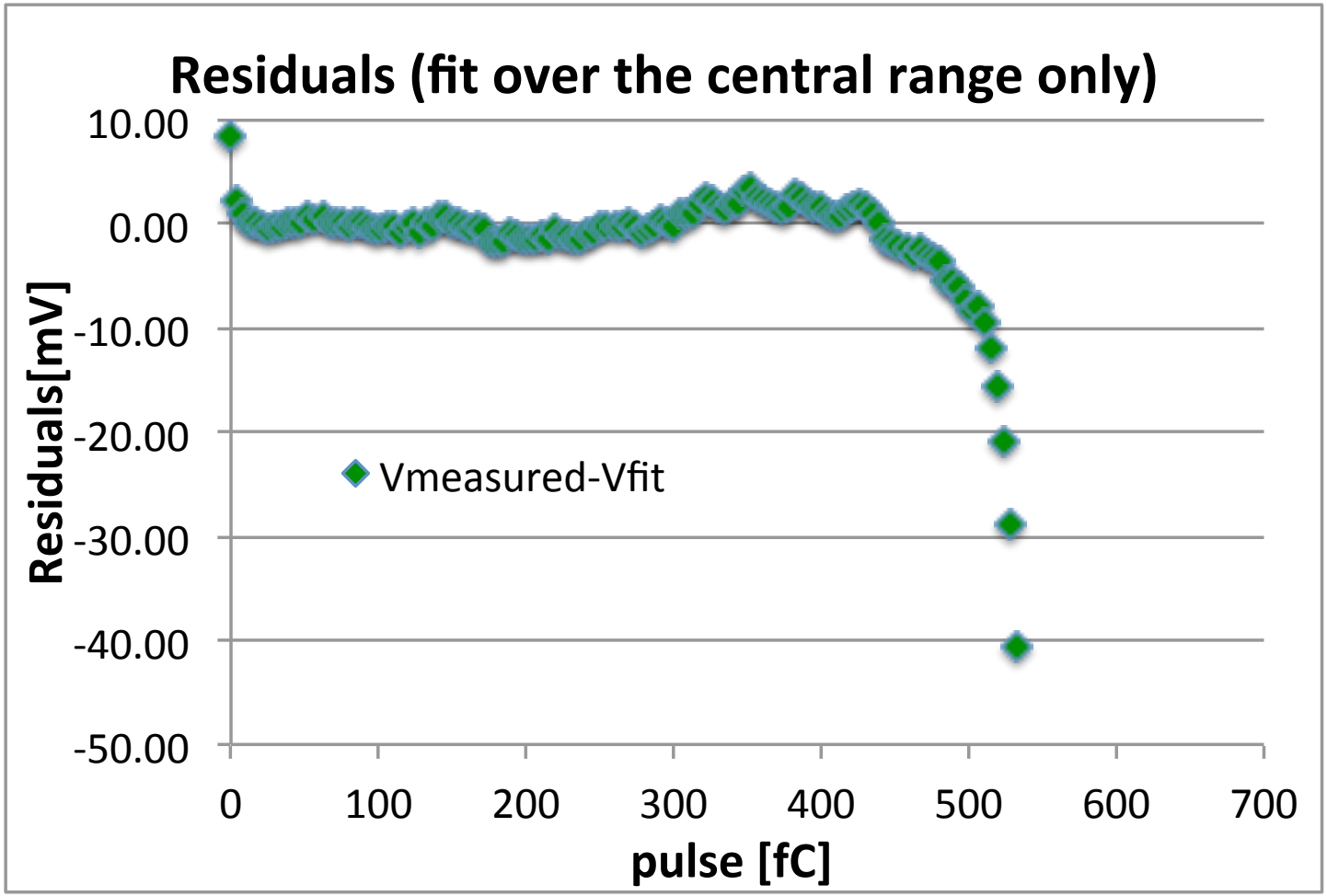
Chip1: Gain value [4mV/fC Pos]



Constant slope up above 500fC pulsed

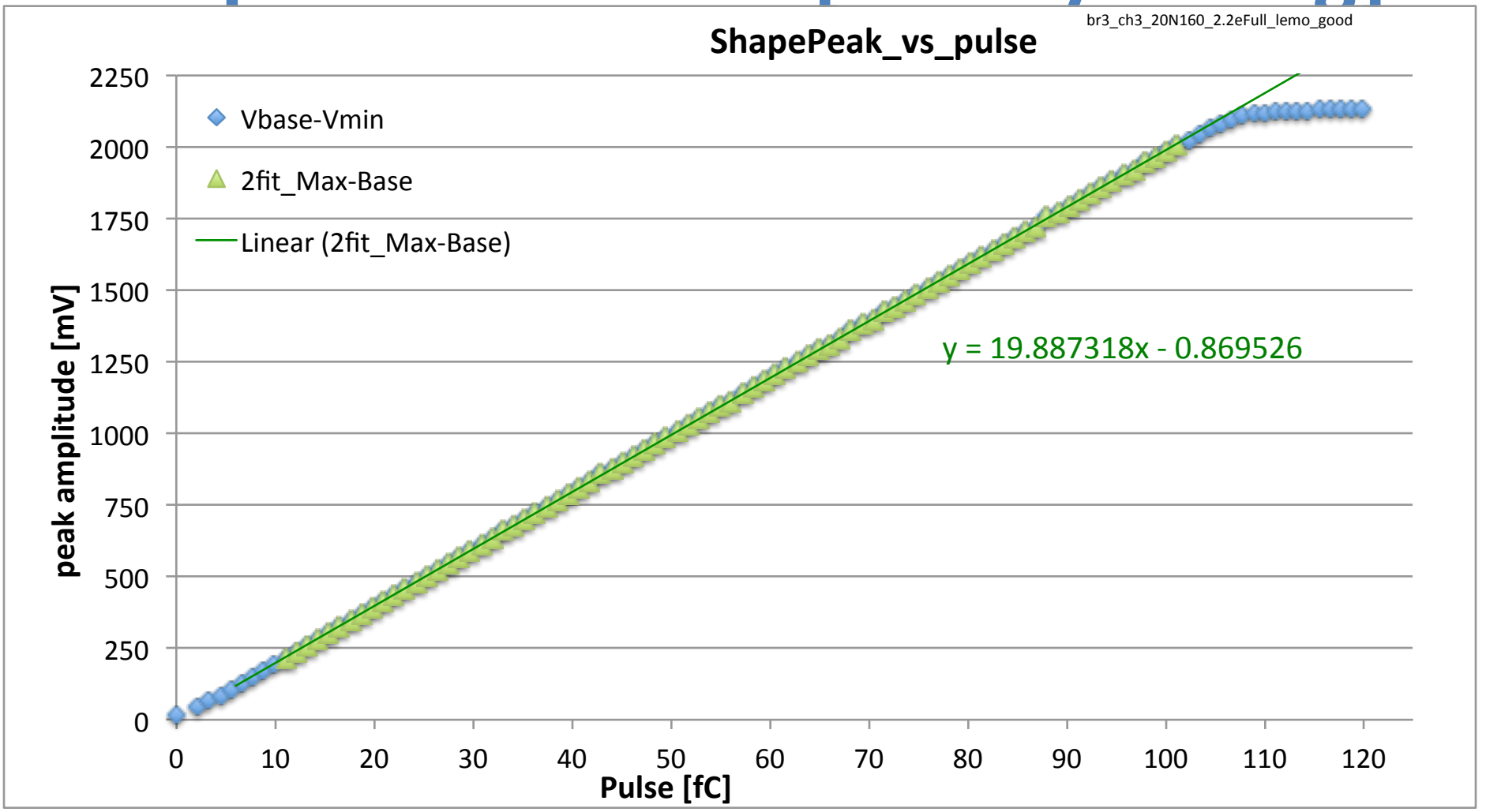
Chip1: Gain linearity [4mV/fC Pos]

(different chip/lab)



Very goo(<.2%) in the 0-400-fC range.
better than 1% in the 400-500 fC range

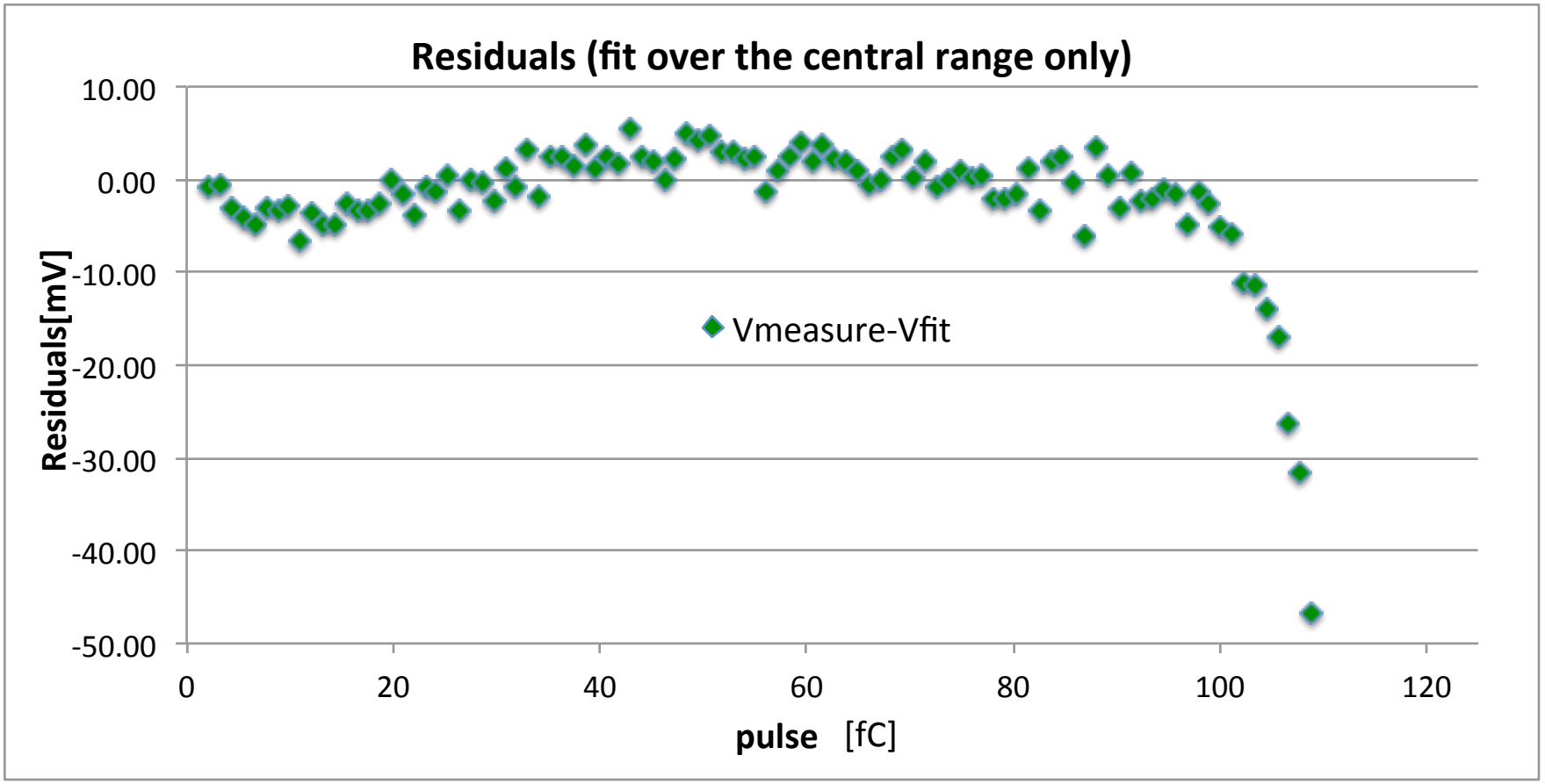
Chip1: Gain value [20mV/fC Neg]



Constant slope up about 100fC pulsed

Chip1: Gain linearity [20mV/fC N]

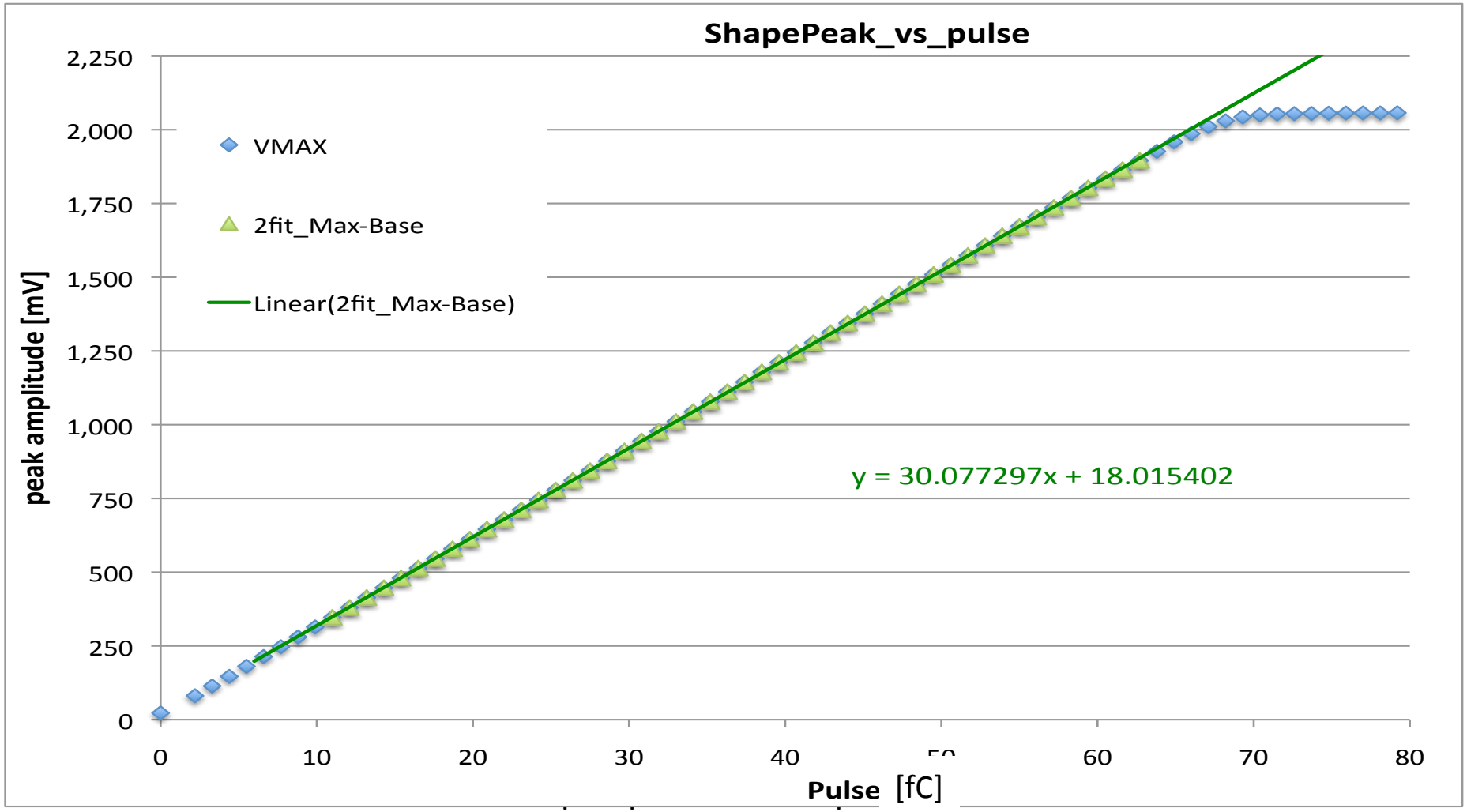
br3_ch3_20N160_2.2eFull_lemo_good



Very goo(<.2%) in the 0-80-fC range.
better than 1% in the 80-100 fC range

Chip1: Gain value [30mV/fC Neg]

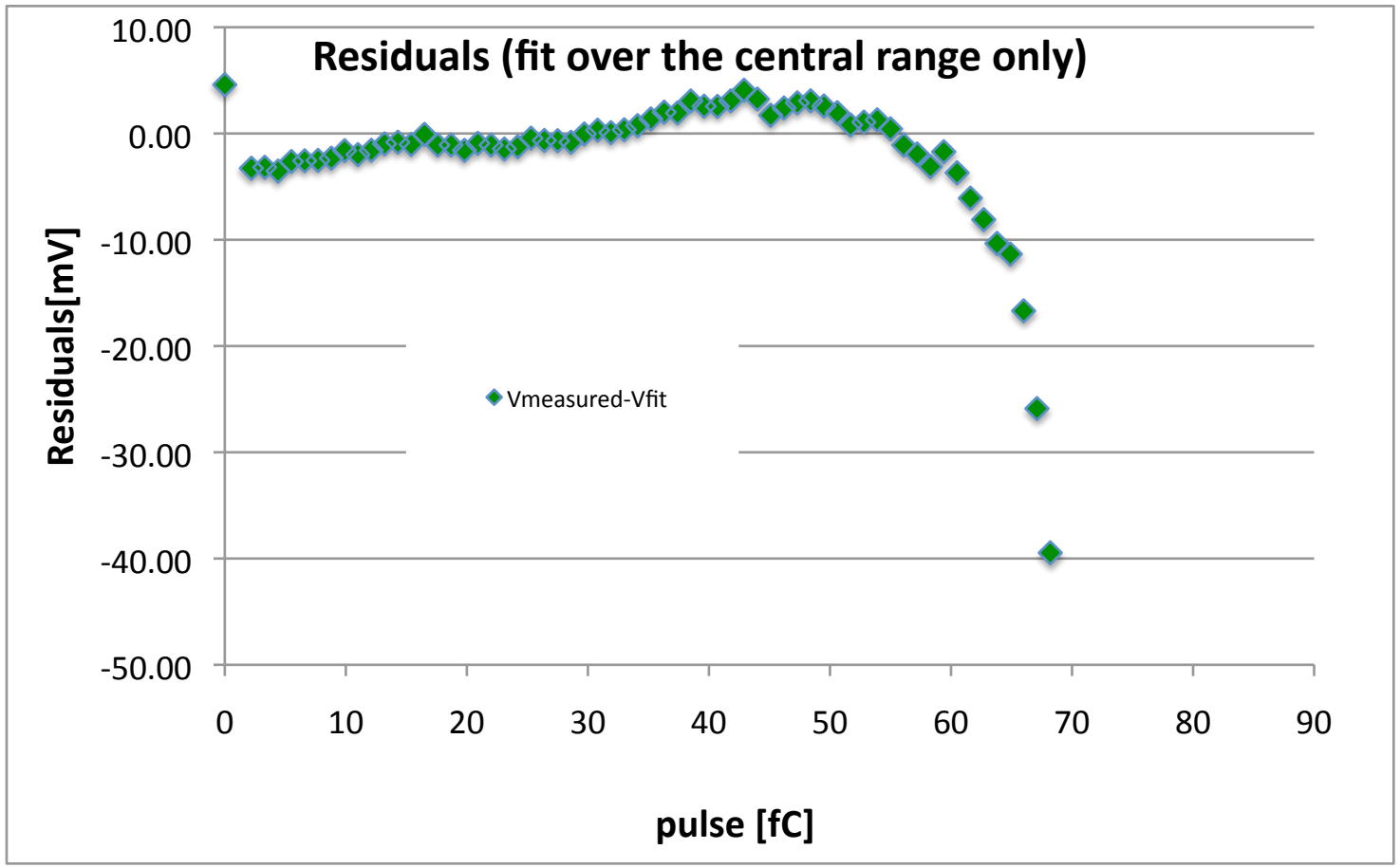
PulseResults_Im1_ch5_30N160_2.2eFull_lemos



Constant slope up about 60fC pulsed

Chip1: Gain linearity [30mV/fC N]

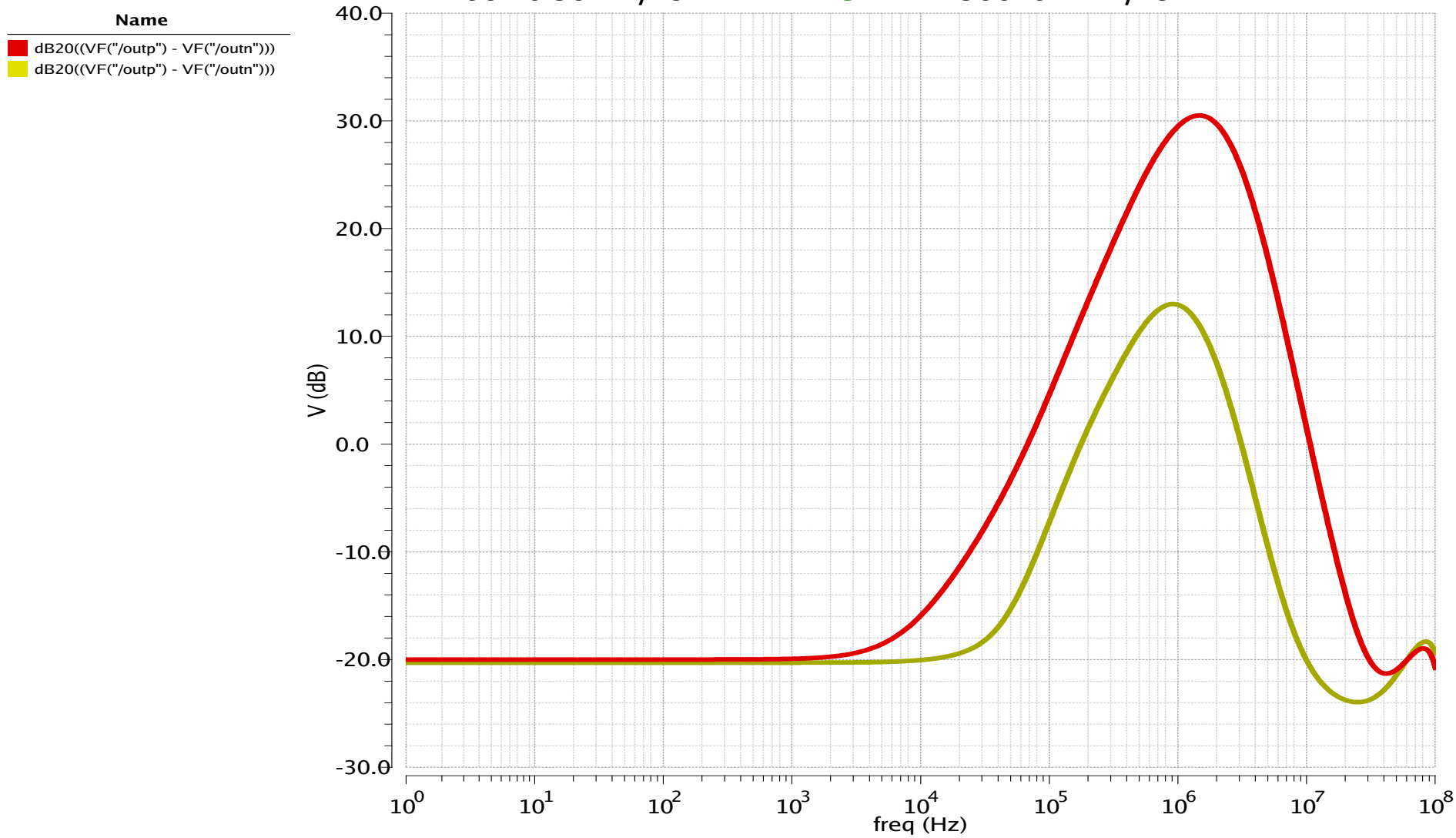
PulseResults_Im1_ch5_30N160_2.2eFull_lemos



Very goo(<.2%) in the 0-50-fC range.
better than 1% in the 50-65 fC range

Chip1: PSRR simulation

RED: 160 ns 30mV/fC **GREEN**: 300ns 4mV/fC



Chip1: PSRR measured

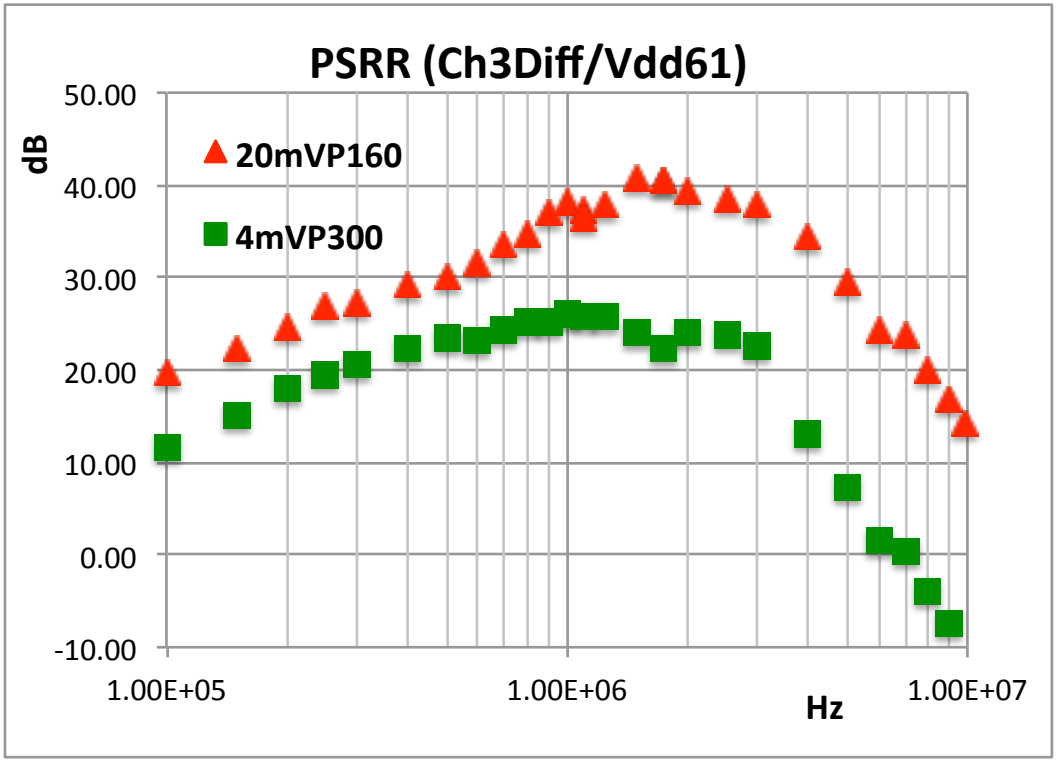
Injected a sine in the VDD, PSRR calculated as the ratio between spectral intensity (a the given frequency) of the FFT of Ch3_differential and FFT of VDD measured on pin61 of the chip

RED: 160 ns 30mV/fC **GREEN**: 300ns 4mV/fC

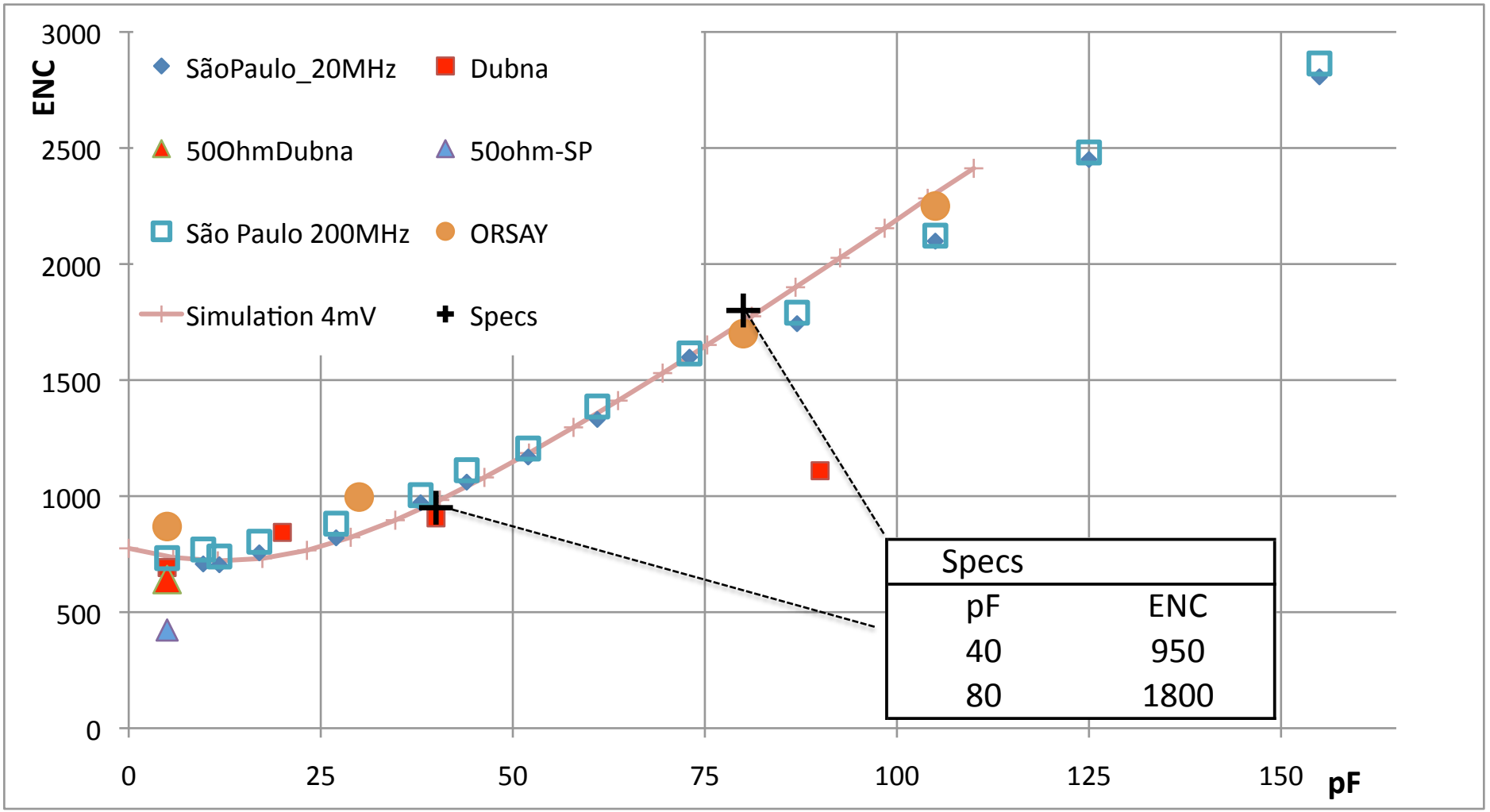
Shape of the PSRR reproduced.
Value even a factor 3 worse..
(but not a easy measurement..)

The present of a "bump" in the 50-60MHz region (corresponding to second peak on the simulation) was only visually verified performing a sweep.

Agreement Simulation/Test
PSRR needs, and it is going, to be fixed/improved in MPW2

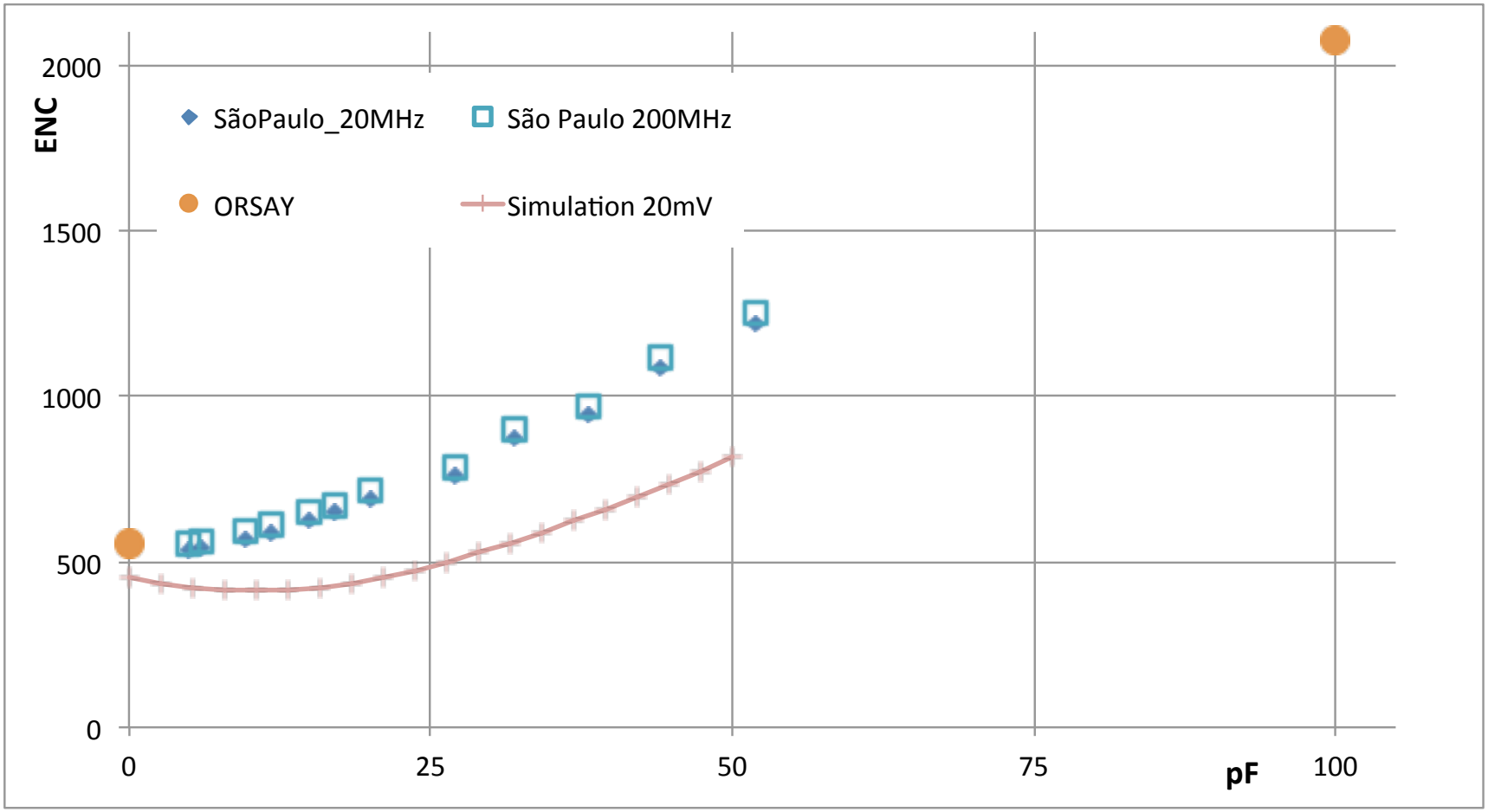


Chip1: Noise @4mV



All lab agree for low C values. Anyway, the noise looks OK

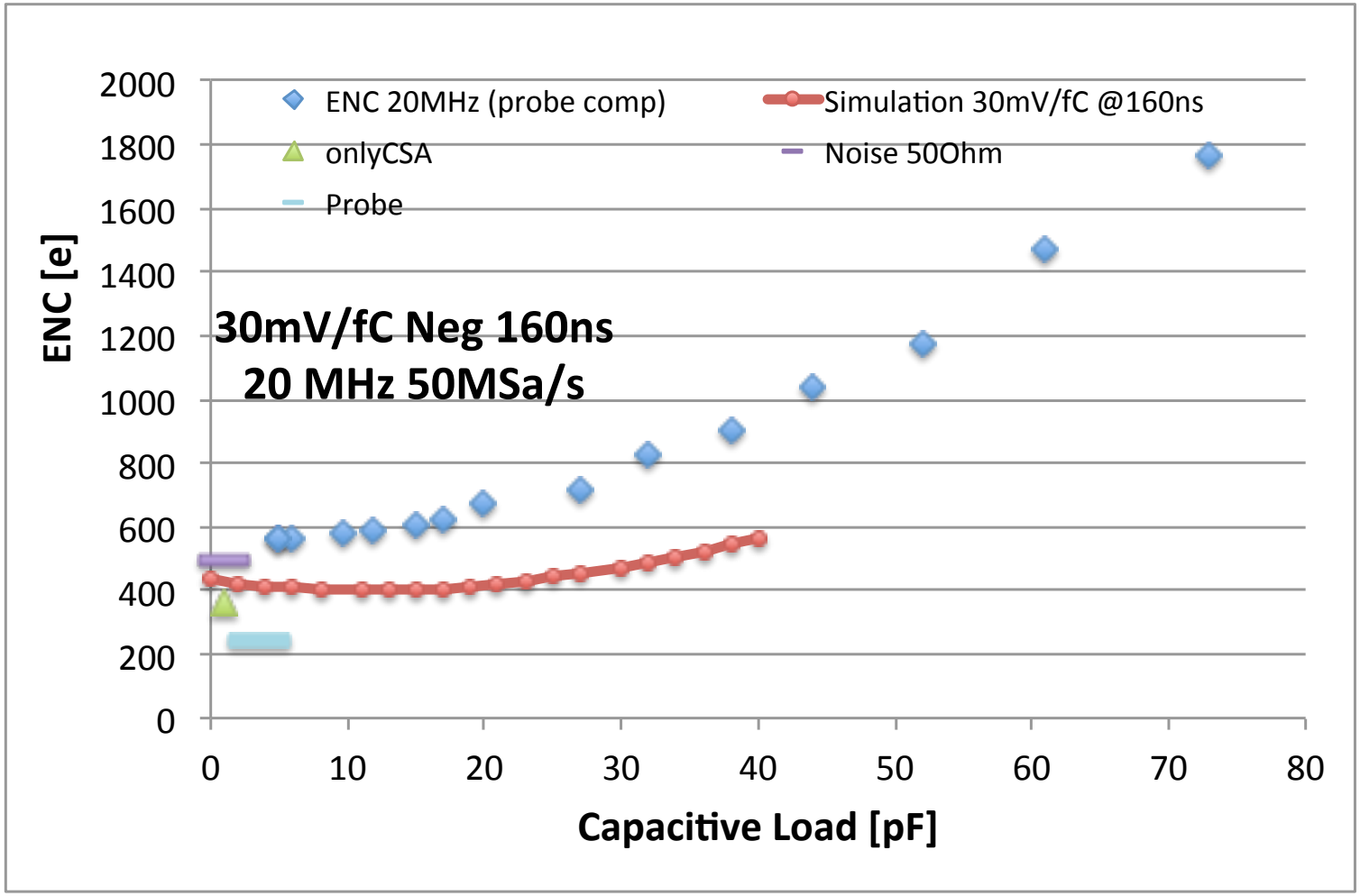
Chip1: Noise @20mV



Well above simulation….

Chip1: Noise @30mV

Im1ch5_30N160lowBW



Again.. Well above simulation

PSRR could explain that. See Hugo presentation

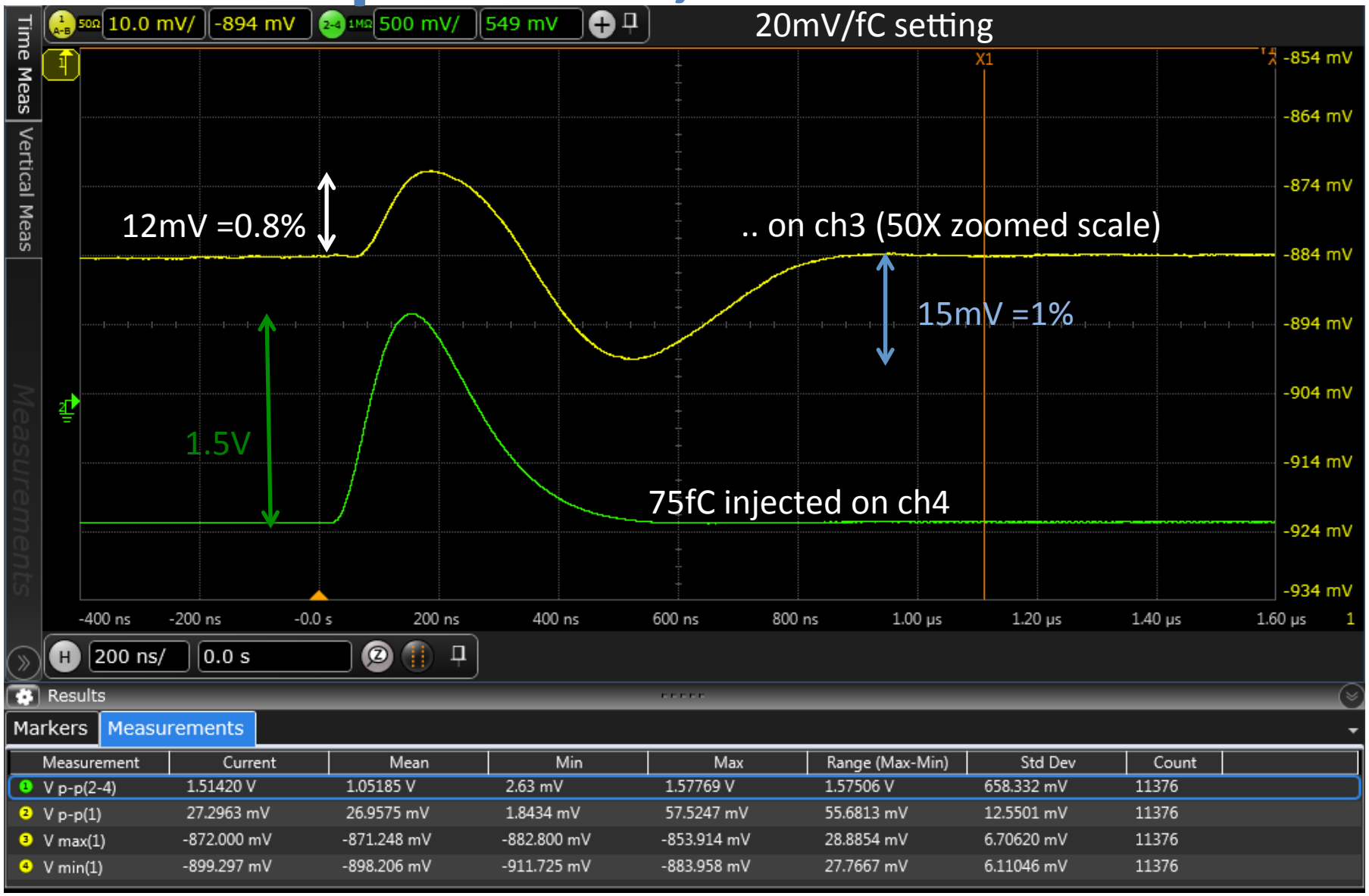
Chip1: xTalk

Orsay measurements @ 4mV/fC 300ns

Crosstalk external capacitor (4,7pF) Qin=92fC (Vin=20mV)							
Injected Channel	Adjacent Channel		V Channel (mV)	VADJ E (mV)	VADJ F (mV)	Crosstalk E (%)	Crosstalk F (%)
1		2	380		2.42		0.64
2	1	3	381	1.64	1.67	0.43	0.44
3	2	4	379	2.2	2.48	0.58	0.65
4	3	5	380	2.32	2.52	0.61	0.66
5	4		382	2.56		0.67	

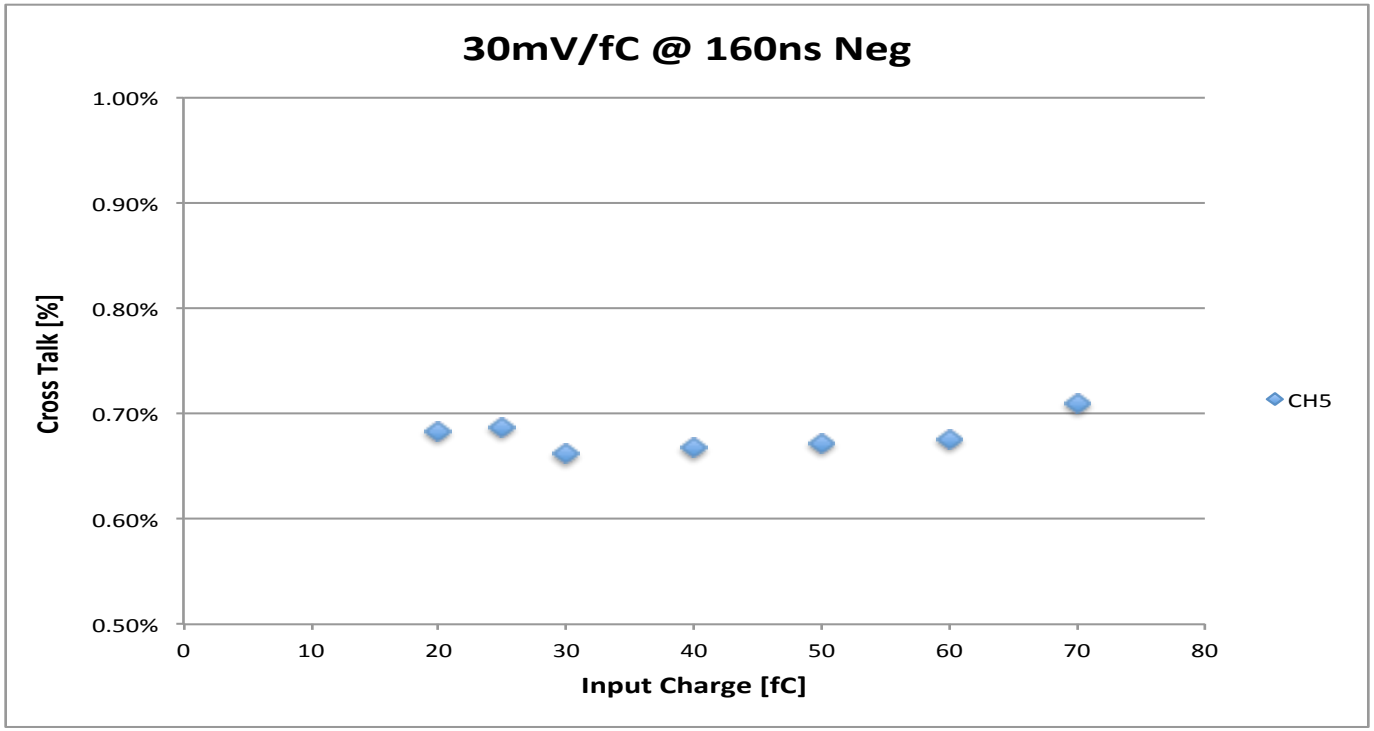
Crosstalk external capacitor (4,7pF) Qin=500fC (Vin=106mV)							
Injected Channel	Adjacent Channel		V Channel (mV)	VADJ E (mV)	VADJ F (mV)	Crosstalk E (%)	Crosstalk F (%)
1		2	2010		14.4		0.72
2	1	3	2010	6.62	8.15	0.33	0.41
3	2	4	2000	8.75	11.3	0.44	0.57
4	3	5	2010	10.5	12.55	0.52	0.62
5	4		2000	13.6		0.68	

Chip1: Xtalk, a bad case



Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
V p-p(2-4)	1.51420 V	1.05185 V	2.63 mV	1.57769 V	1.57506 V	658.332 mV	11376
V p-p(1)	27.2963 mV	26.9575 mV	1.8434 mV	57.5247 mV	55.6813 mV	12.5501 mV	11376
V max(1)	-872.000 mV	-871.248 mV	-882.800 mV	-853.914 mV	28.8854 mV	6.70620 mV	11376
V min(1)	-899.297 mV	-898.206 mV	-911.725 mV	-883.958 mV	27.7667 mV	6.11046 mV	11376

xTalk vs Input charge (4<->5)



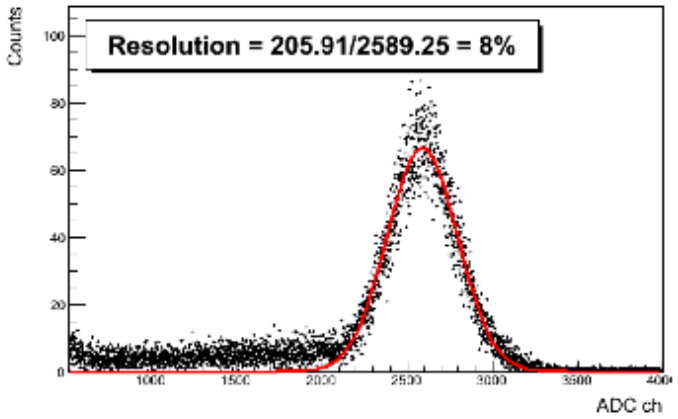
Overshoot behaviours seen here too.. (same cure as for direct signals)

Xtalk is higher than specs… coupling in the testboard (present even in the Improved version) and coupling in the wirebonds (small chip in relative big package) for sure play a role on that.

Chip1: with GEM
survived and operated nicely

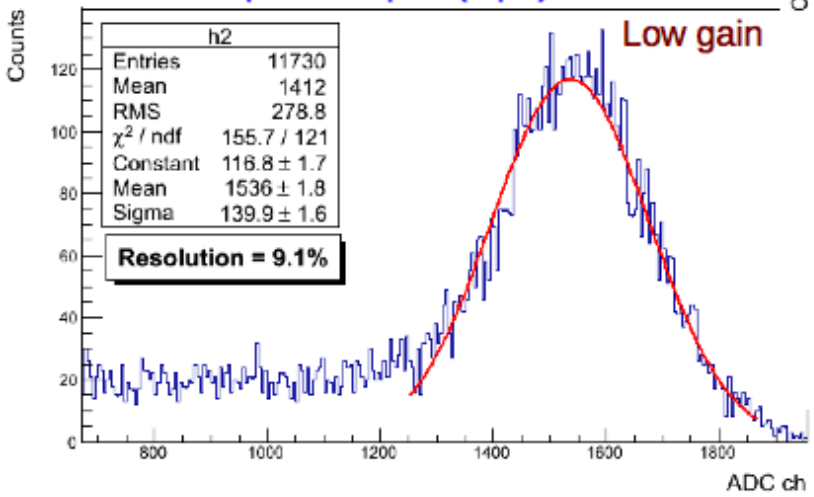
Results: Fe55 energy spectrum: Ne mix.

Discrete-component pre-amp

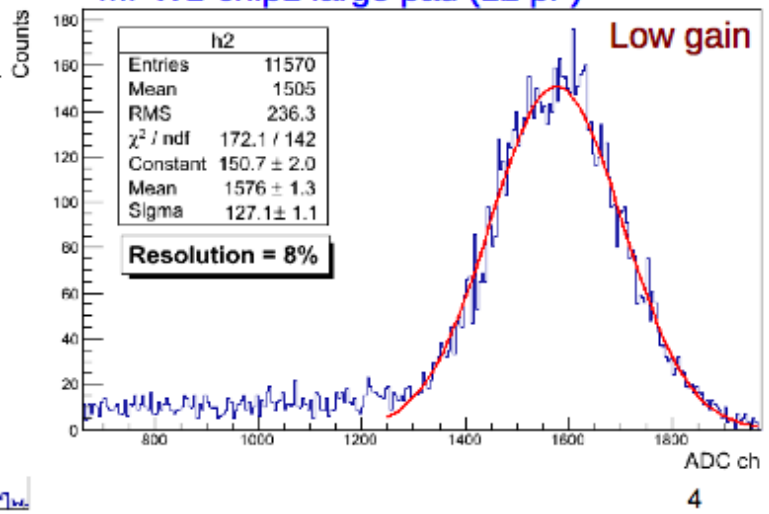


- Single ended waveforms
- small pad – 6 x 15 mm^2
- Large pad – 30 x 30 mm^2
- Ne + CO_2 + N_2 (90 % +10 % + 5%)
- Detector gain ~ 2000

MPW1-chip1 small pad (2 pF)



MPW1-chip1 large pad (12 pF)



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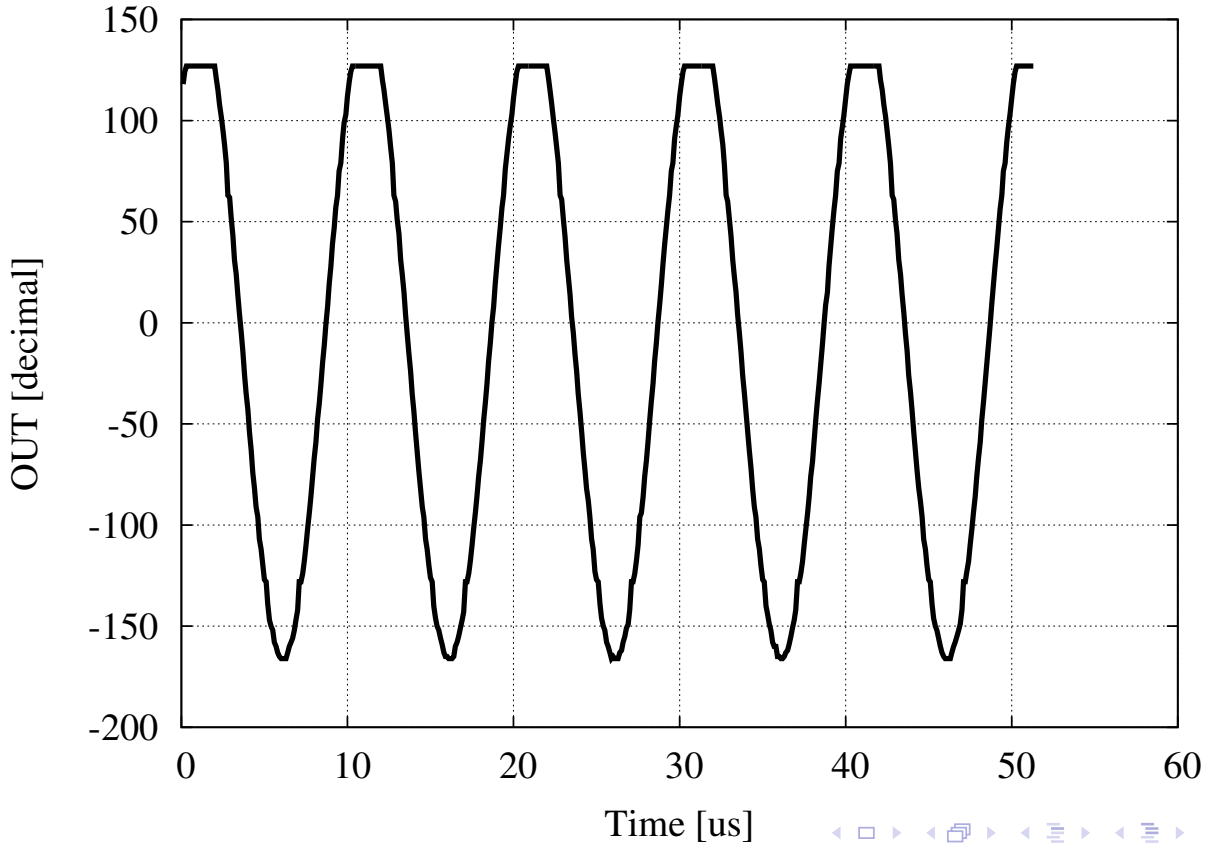
CHIP_2 “ADC”

Chip2: ADC distorted output

Chip02: ADC output (Non-improved board)

Input: sine wave [Amp = 500mVpp Freq= 100KHz] VREF=1.25V VREFN=0V



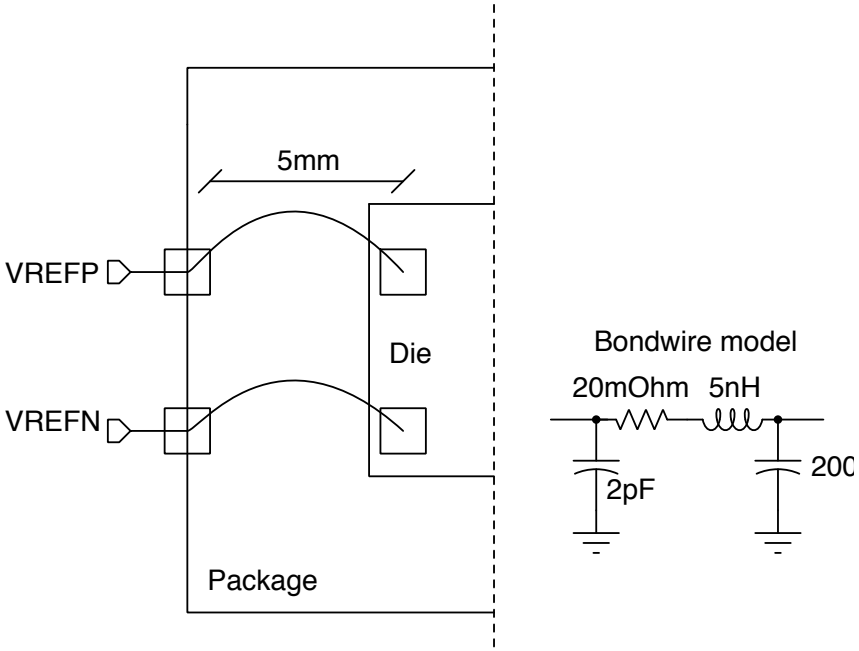
Hugo 25/3

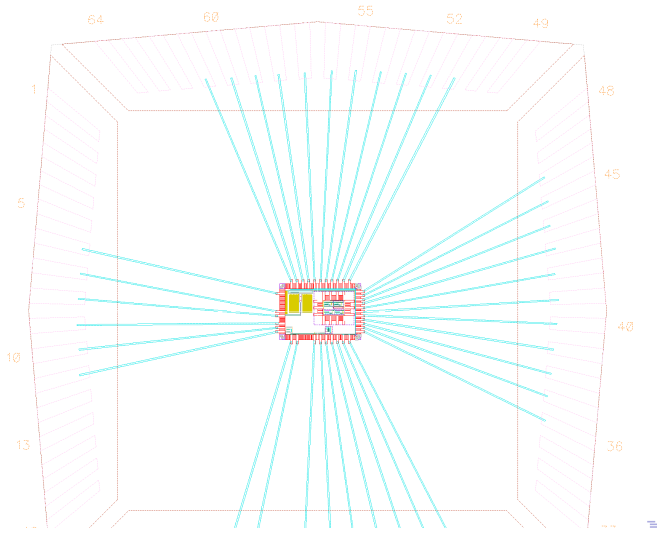
Chip2: reason for the problem

Chip02: bondwire diagram

The distorsion is generated by the bondwire inductance of the ADC voltage references (VREFP, VREFN)

Bondwire length ≈ 5mm Inductance ≈ 5nH (1nH per mm)





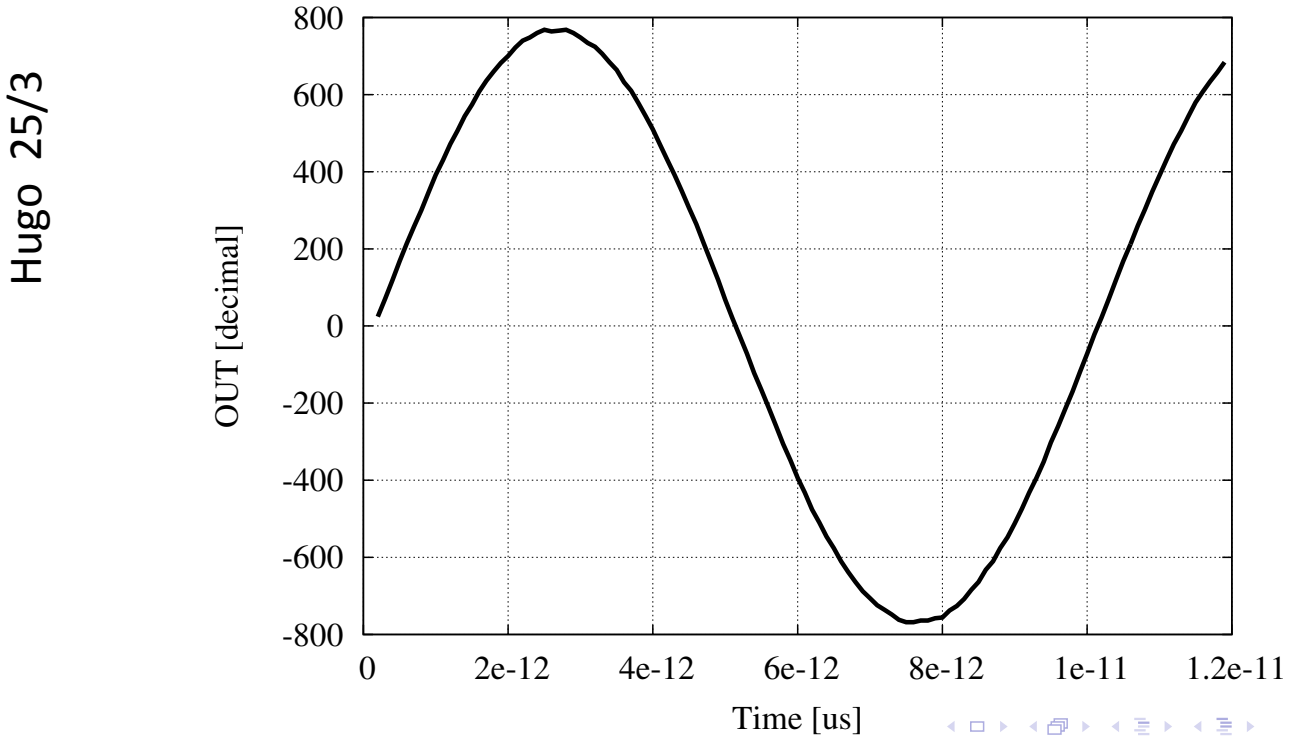
Hugo 25/3

Chip2: Board Patched

Filter/load reference lines… signal improves a lot.. But characterization is not possible with this setup. Considering chip-on-board option

Chip02: ADC output (improved board)

Input: sine wave [Amp = 1Vpp Freq= 10KHz] VREF=1.25V VREFN=0V ENOB=7.8bits



Chip_3 “full Chain”

Chip3

- As for chip2, ADC voltage reference are external to the package chip
- Same distortions and the ADC signals
- Highest gain settings (30mV/fC) is oscillating

Chip3: 30mV/fC oscillations

Chip3 – tests – Negative polarity

Observed oscillations while using negative input polarity options

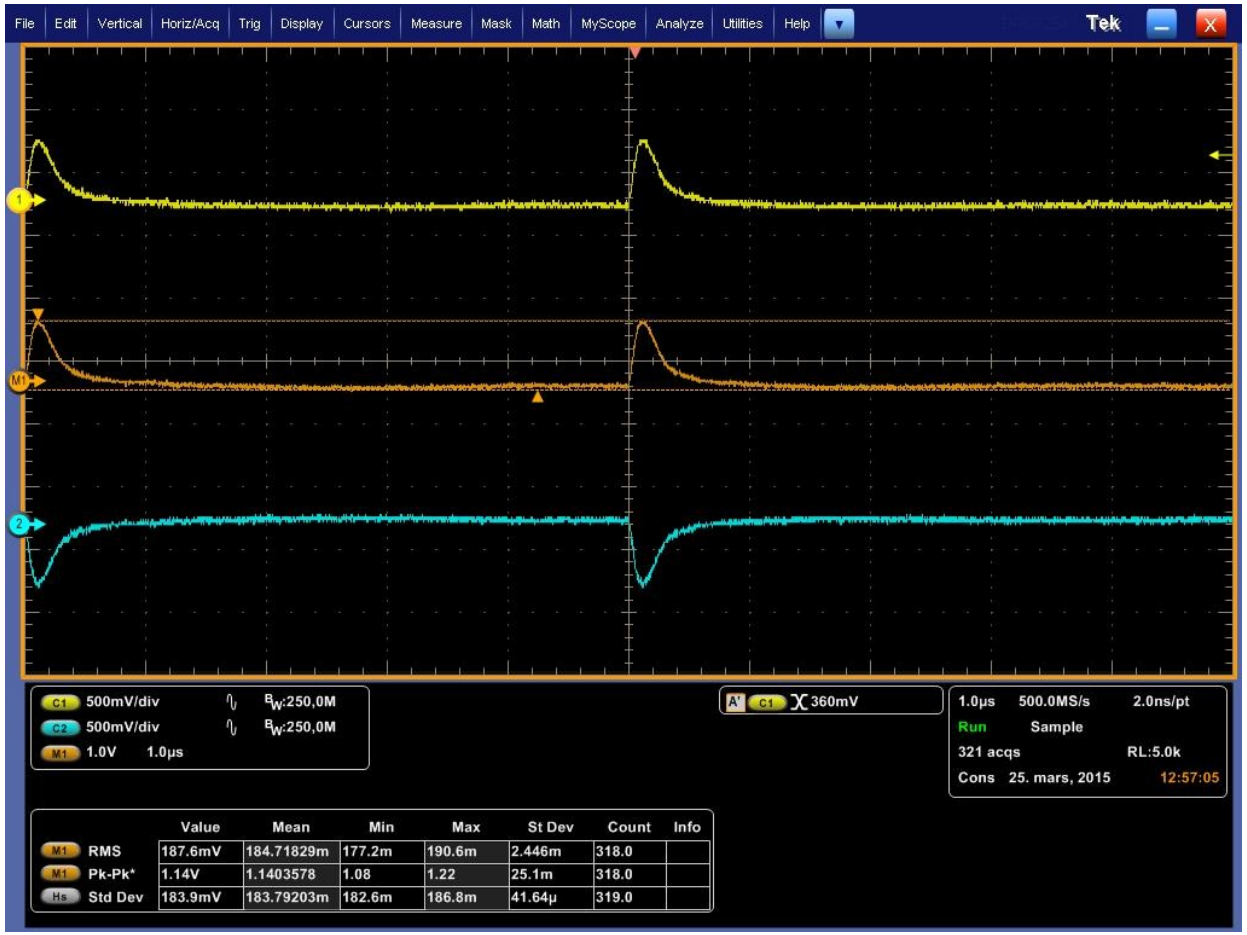
Ganesh SampaTest meeting 25/03

Chip3: 30mV/fC oscillations

Chip3 – tests – Positive polarity

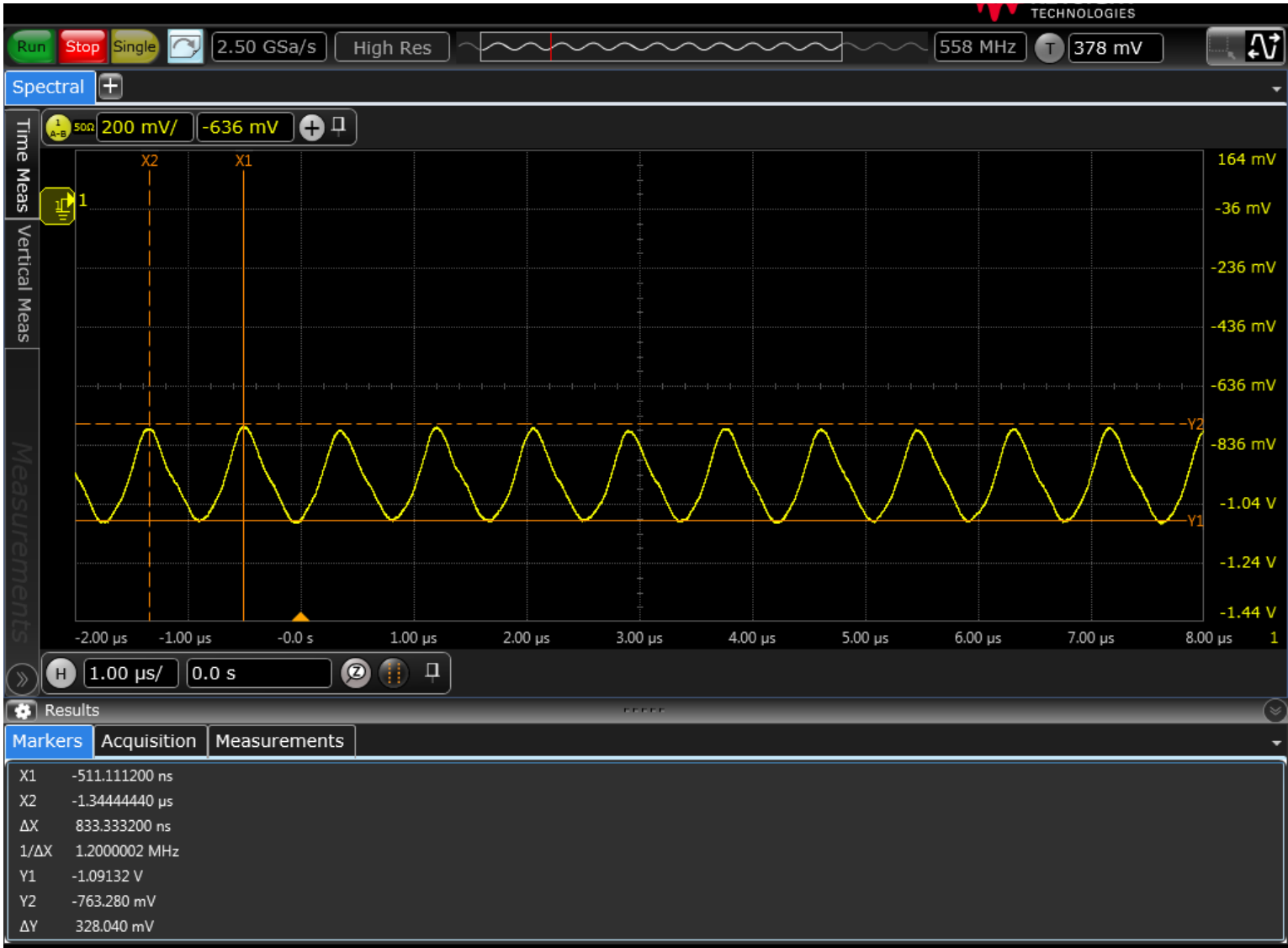
Observed oscillations while using negative input polarity options

Ganesh SampaTest meeting 25/03



30mV/fC oscillations

Visible in some chip1 testboards. Investigated a bit more there



30mV/fC oscillations

Visible in some chip1 testboards. Investigated a bit more there

- Only for negative polarity settings
- Lowering VDD helps (all chips worked very stable at 1.19V)
- Increasing VDD things gets worse, some chips with VDD=1.30V show instabilities with 20mV/fC gain
- All Channels on the chip oscillates together
- Modifying analog Vrefs (450/750), bringing P -and N-side baseline away from “1.2V” improve stability too.
- Noise environment plays a role
- oscillation amplitude scales with VDD

Problem appear in relation with undershoot -> Already been fixed in MPW2

Proper positioning of the baseline seems to be important, too.

-> To be kept monitored for MPW2

What's missing?

- VDD corners investigated
  - Vdd=1.19 just lower range
  - Vdd=1.31 could show stability problems

What's about chip irradiation?

Preparation on going (Oslo/Sohail). Test schedule for the end of the month.

overview

- Chip_1: “Analogue”, CSA+Shapers
  - Power consumption
  - Pulse shape
  - Peaking time
  - Gain value and linearity
  - PSRR
  - Noise
  - xTalk
  - reading a GEM detector

- Chip_2: “ADC”
  - Testability problems

- Chip_3: “FullChain”, CSA+Shapers +ADC+(dummy*)DSP
  - General functionality
  - Testability criticalities
  - Tests so far

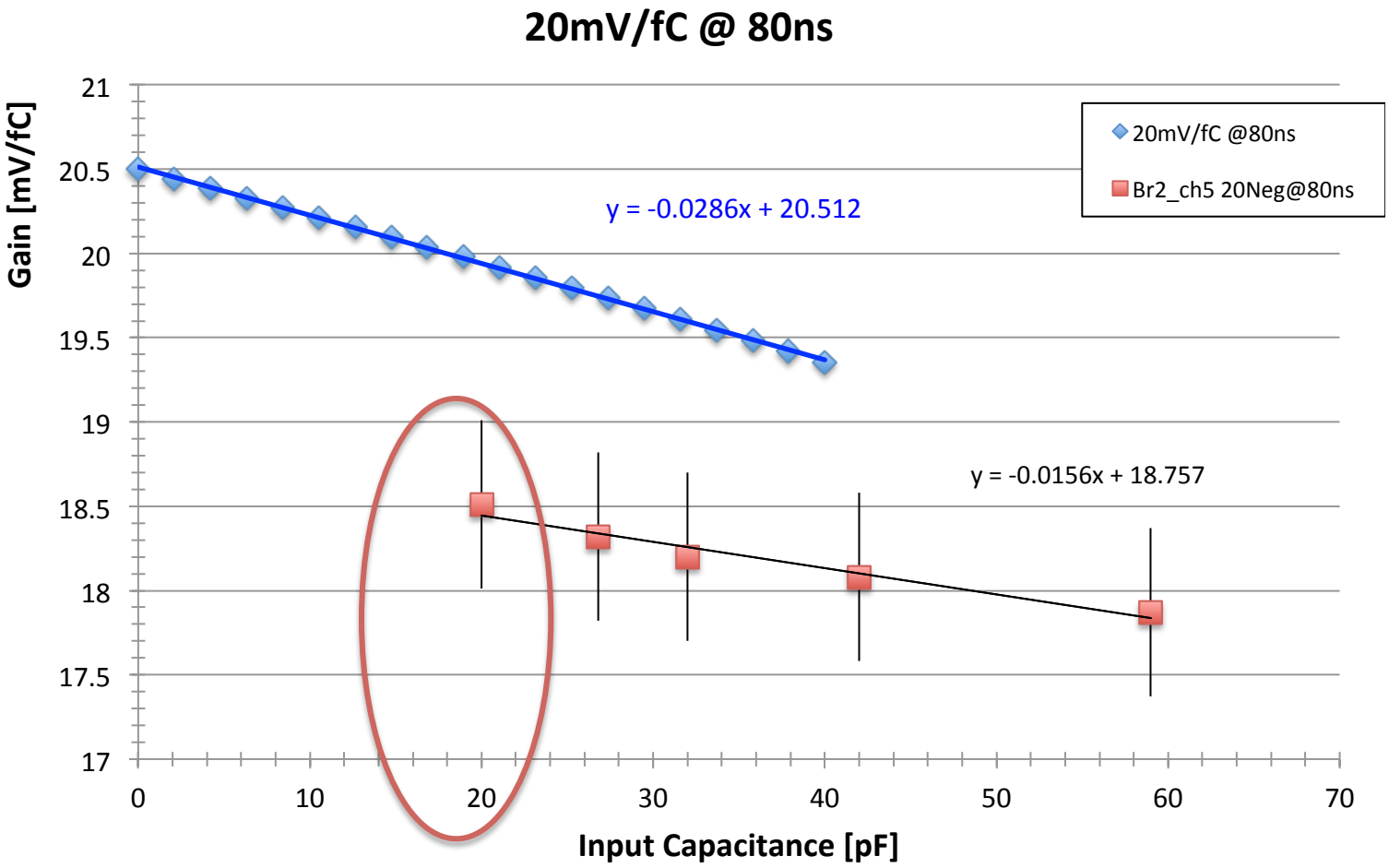
+ still ongoing and coming soon

- To tuned/fixed
  - To be reduced a bit more
  - Overshoots/long tail -> Fix last stage
  - A bit to fast -> fix it
  - Proper gain, GOOD linearity
  - To be improved
  - Due to PSRR
  - Not perfect, yet, likely wirebond play a role
  - Promising
- Inductive load form wirebond screw up signals.. In the (little) extend it was possible to test it, it looks ok.
- Suffer of the same problem of chip2 test
  - Readout chain up to ADC verified
  - Noise @4mV appears to be less than LSB
  - Noise @20/30mV appears to ~2LSB
  - Affected by oscillation for 30mV/fC Neg
  - Irradiation tests are coming.

ADDENDUM

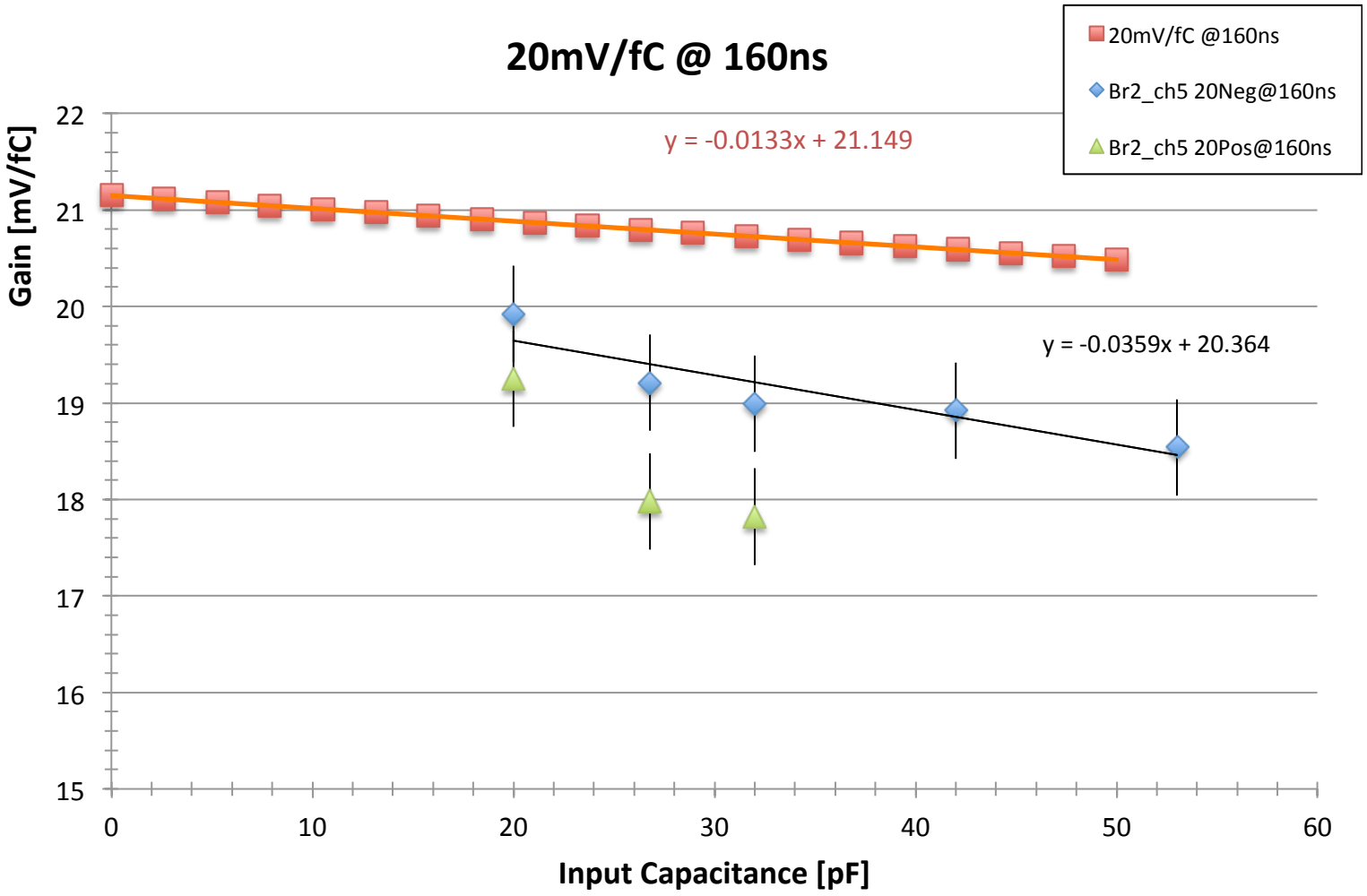
The missing gain vs C measurements

Gain vs Detector Capacitance – TPC

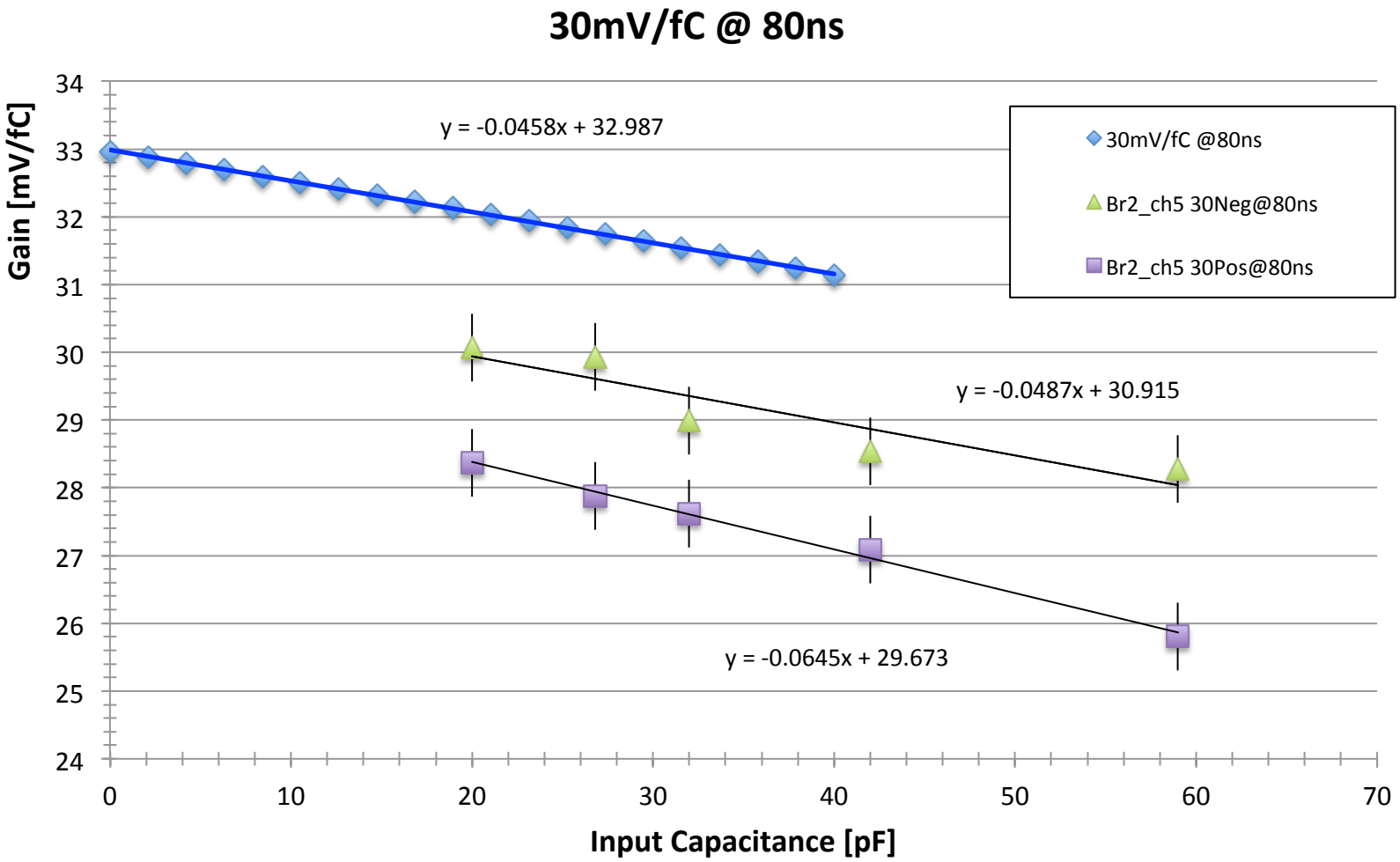


"cable offset": the lemo going from the "pulser" capacitor to the lemo input is "loading" with about 20-25 pF

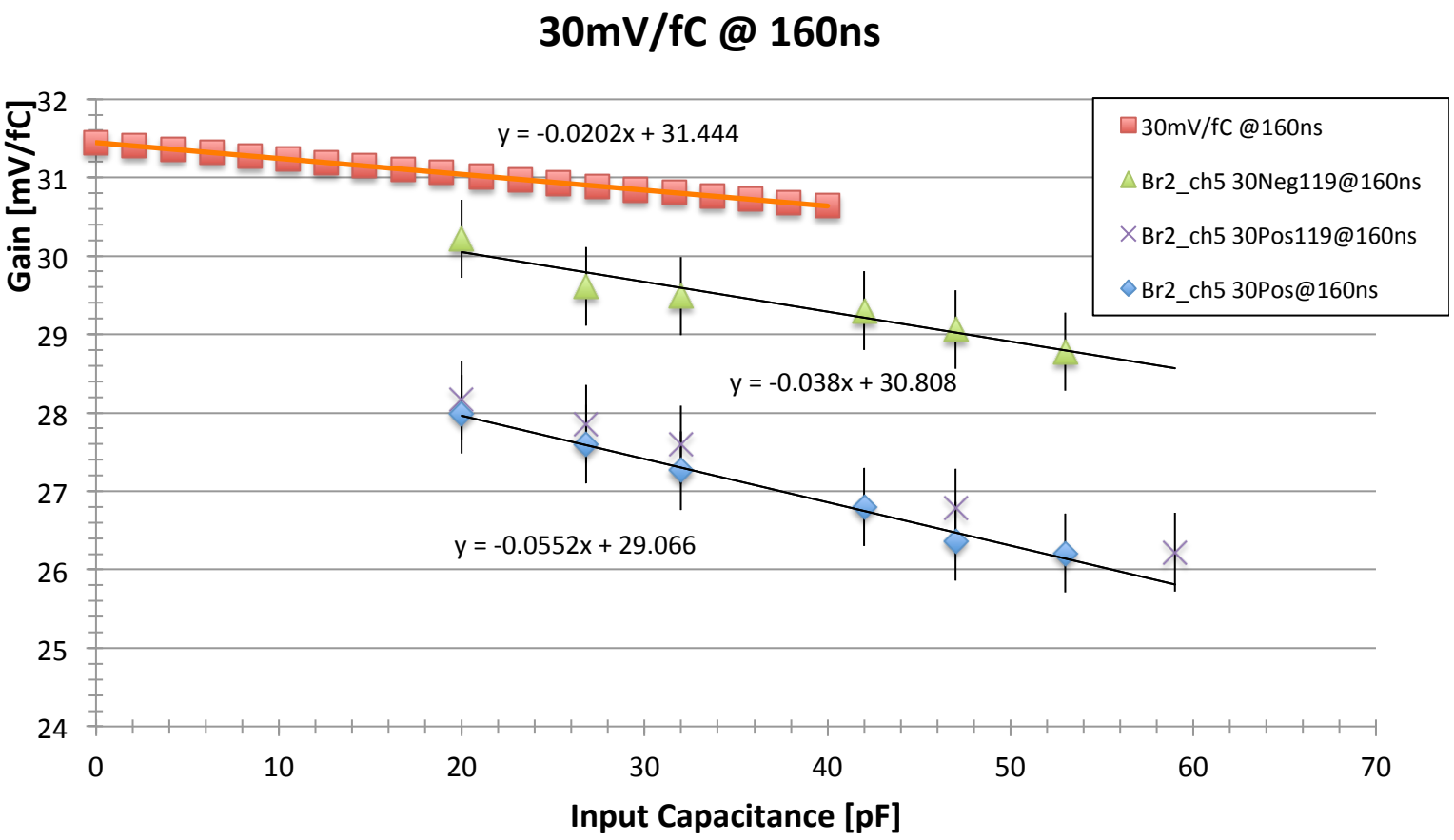
Gain vs Detector Capacitance – TPC



Gain vs Detector Capacitance – TPC



Gain vs Detector Capacitance – TPC



Gain vs Detector Capacitance – MCH