SAMPA: MPW2 Design review

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Definitions

Corners:
LV=1.1875V

HV=1.325V

LT=0°C

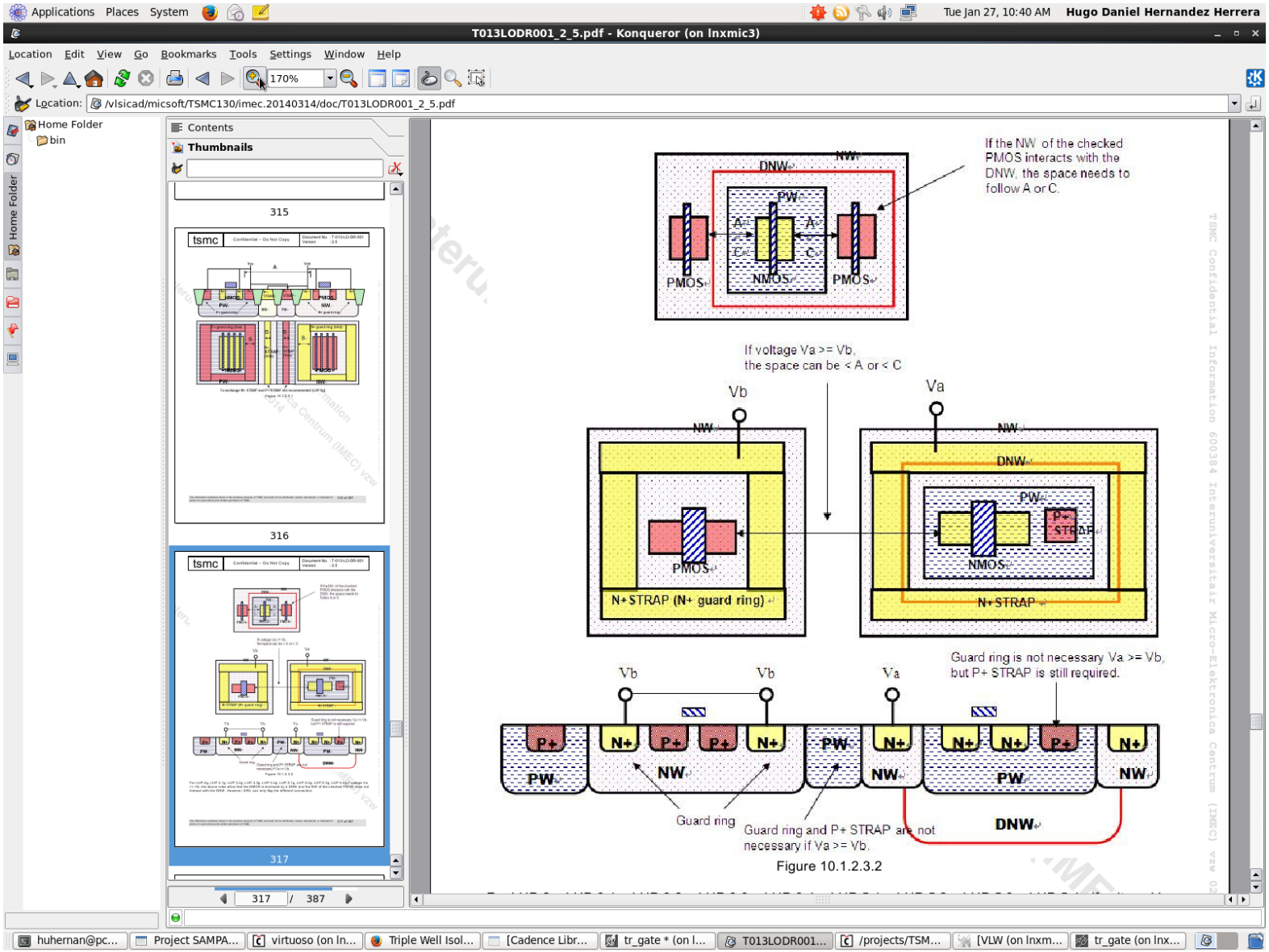
HT=50°C

Models:
typ= Typical
ss= Slow
ff = fast
MC=Monte Carlo

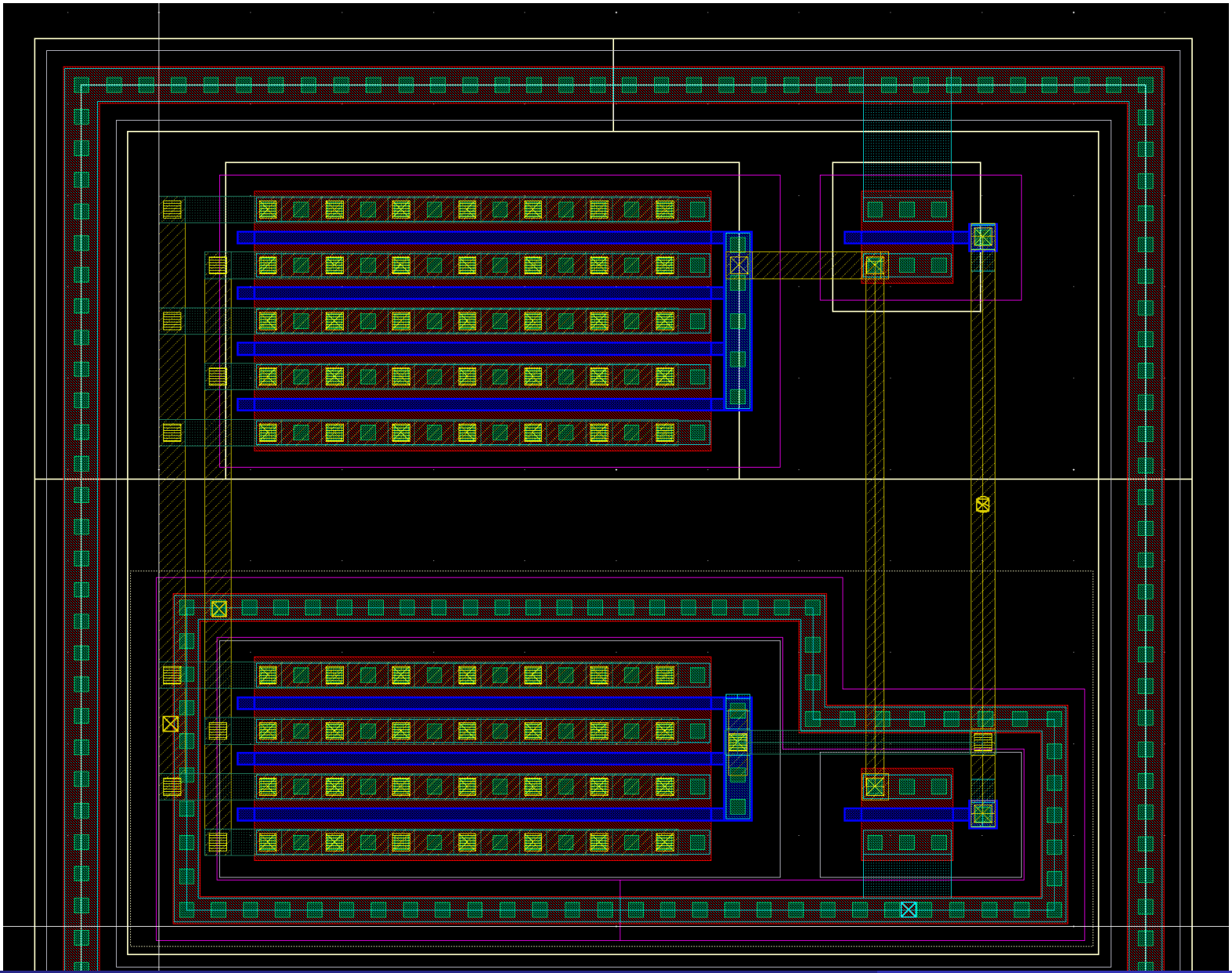
Question

The analog power domain needs to be protected from the digital noise environment. NT_N division trenches need to be implemented. The use of triple well transistors should be considered.

Triple-well implementation: TSMC recomendation

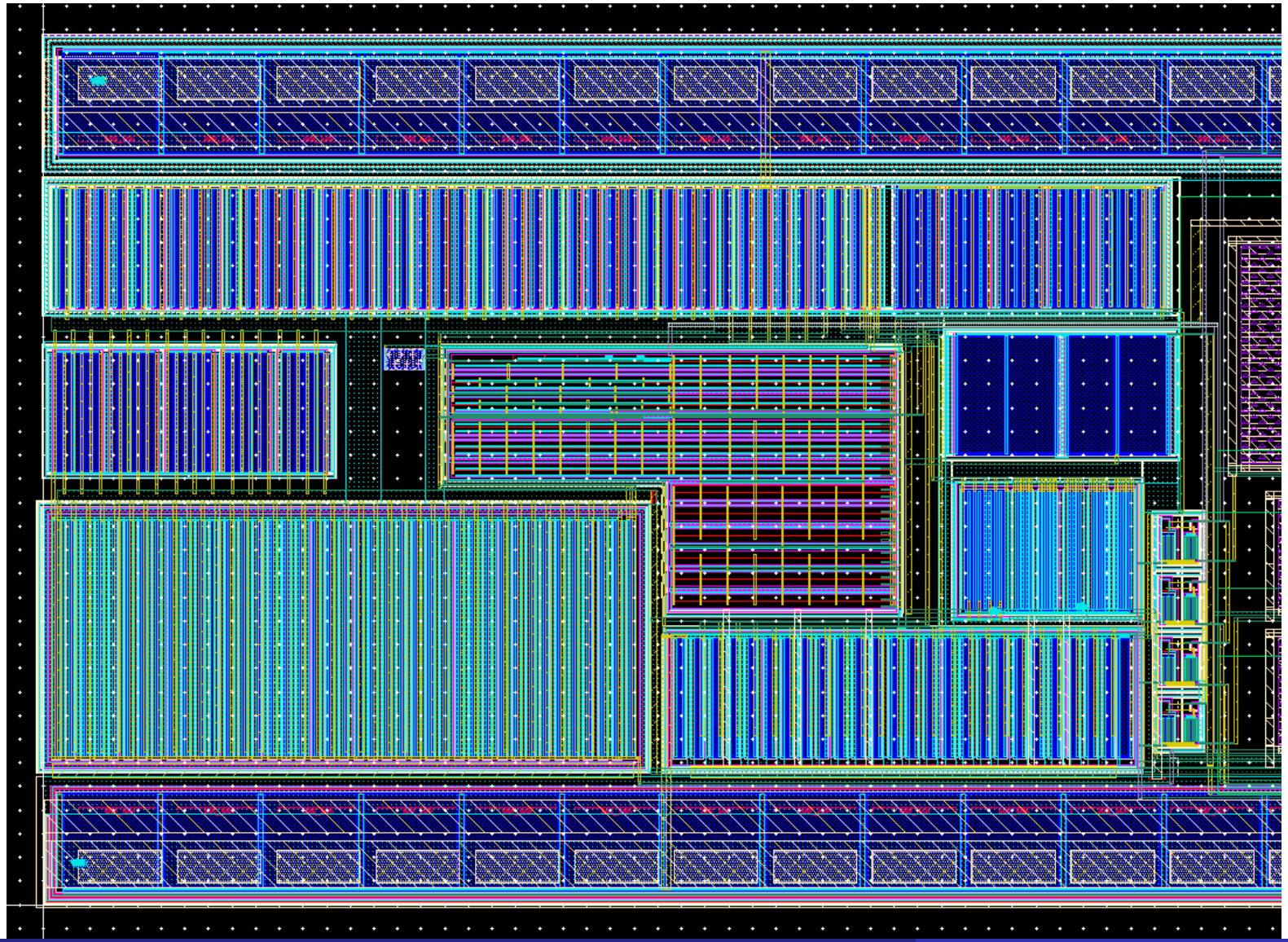


Triple-well implementation: Example



NMOS transistors of the frontend are triple_well

CSA layout implemented with triple-well option

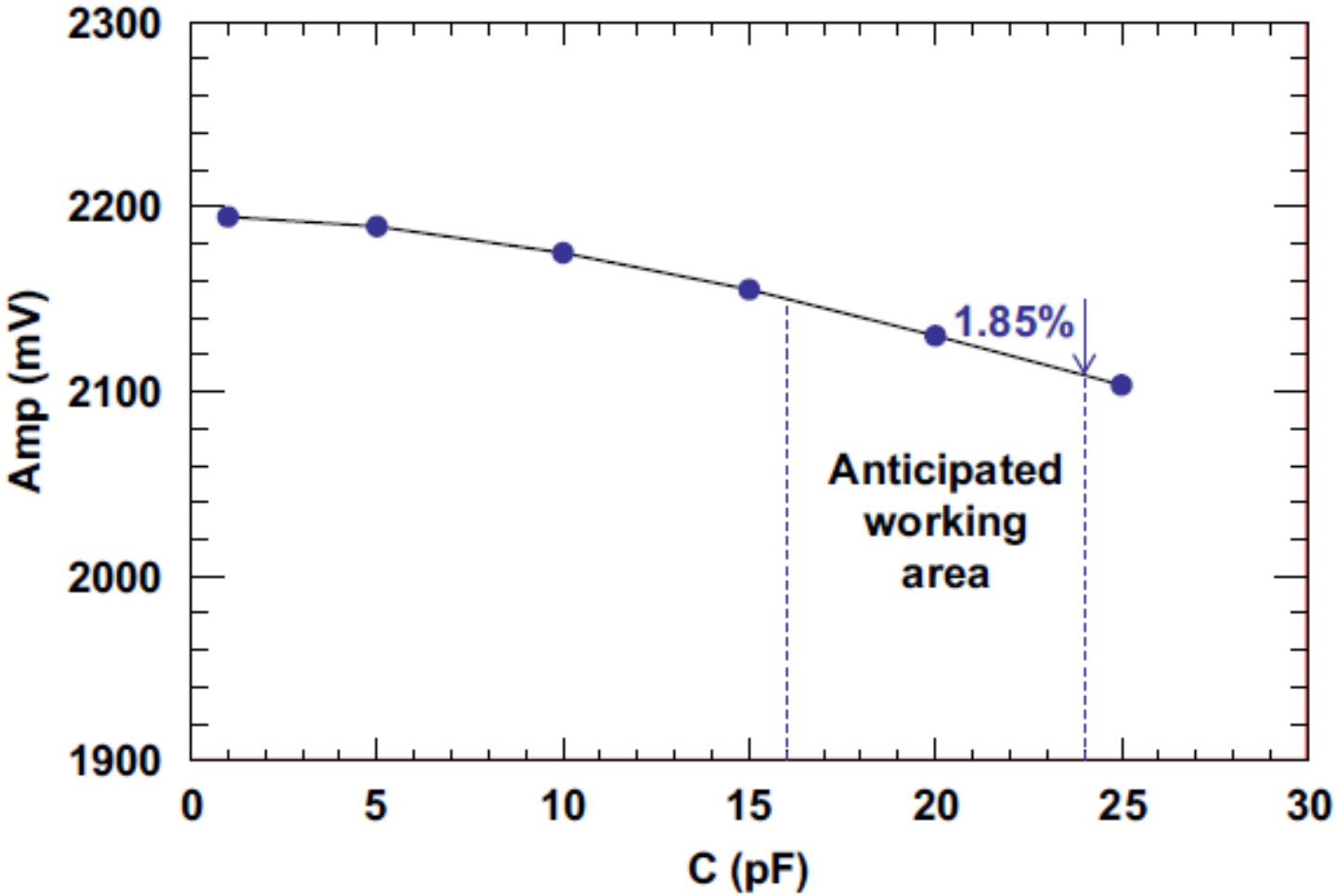


Question

It was commented that the CSA has no boosting transistors. According to the experience of the reviewers they are necessary in TSMC 130 as the transistor gain is not sufficient. The concern is that the CSA response depends strongly on the detector capacitance. Thus, it is required to study in simulation and test (MPW1), the dependence on capacitance

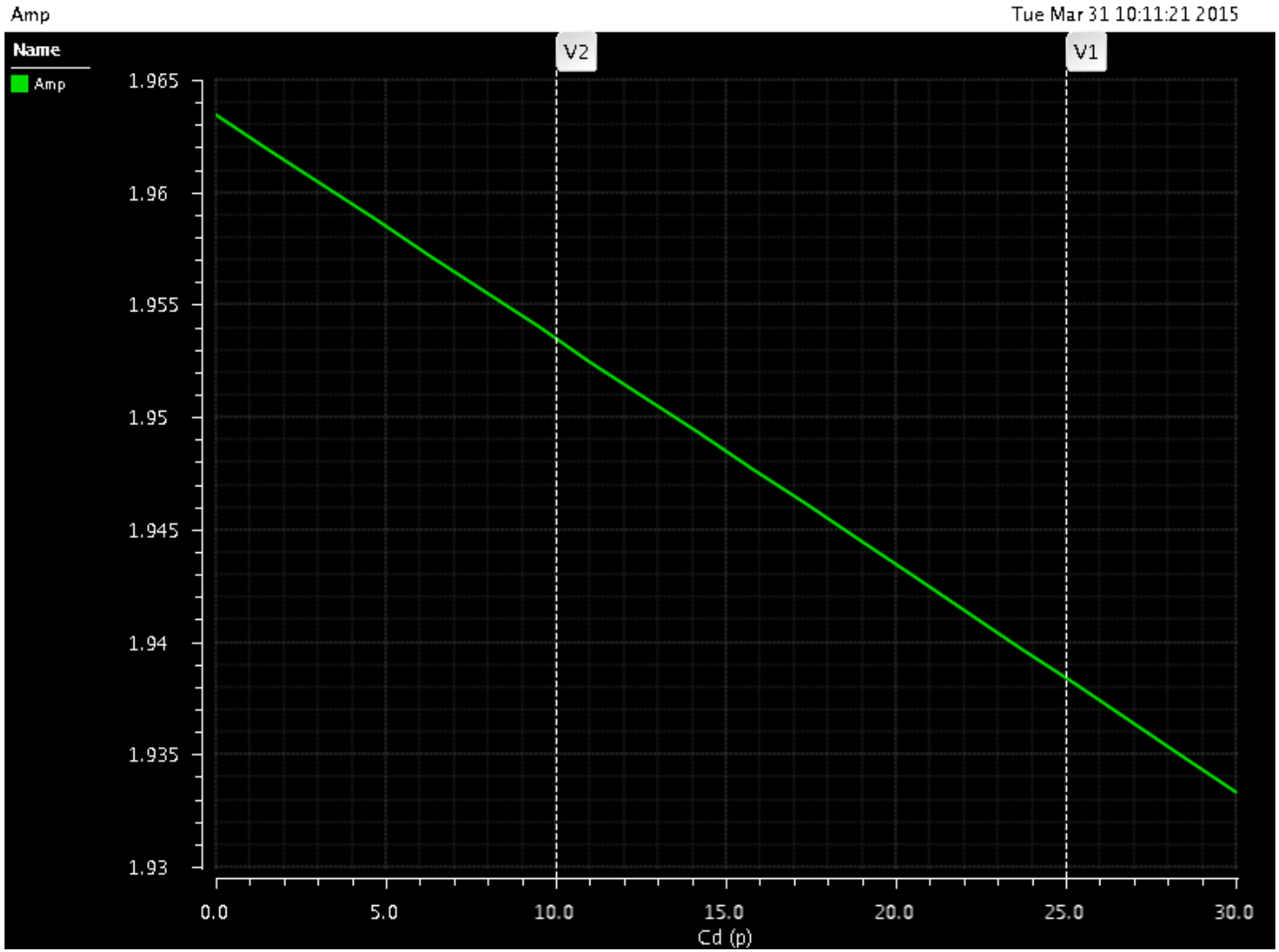
ENC vs Cd: PASA

Amplitude variation of the PASA impulse response as a function of total detector capacitance = 1.85% (12pF-25pF)



ENC vs Cd: SAMPA 160ns@20mV/fC

Amplitude variation of the SAMPA impulse response as a function of total detector capacitance = 0.76% (12pF-25pF)



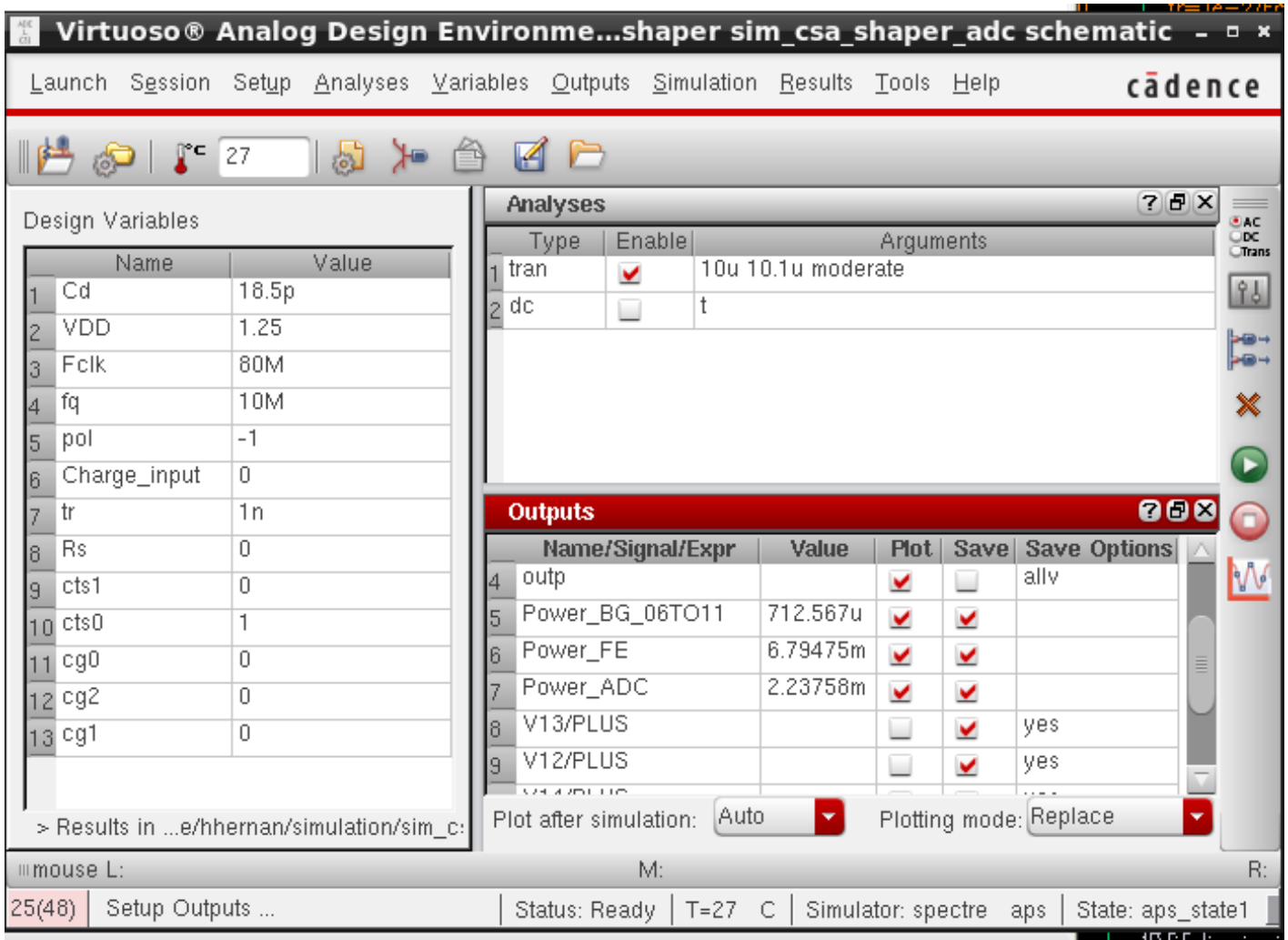
Question

- **There could be room for power consumption reduction. The CSA part of the circuit is nearly the same as TPC PASA and had 11 mW with 3.3 V power supply. So theoretically, the SAMPA CSA should be around 4-5 mW, and still fulfill the requirements**
- **The power consumption must be detailed for different building blocks and the power domains.**

Power: Frontend - ADC - Bandgap

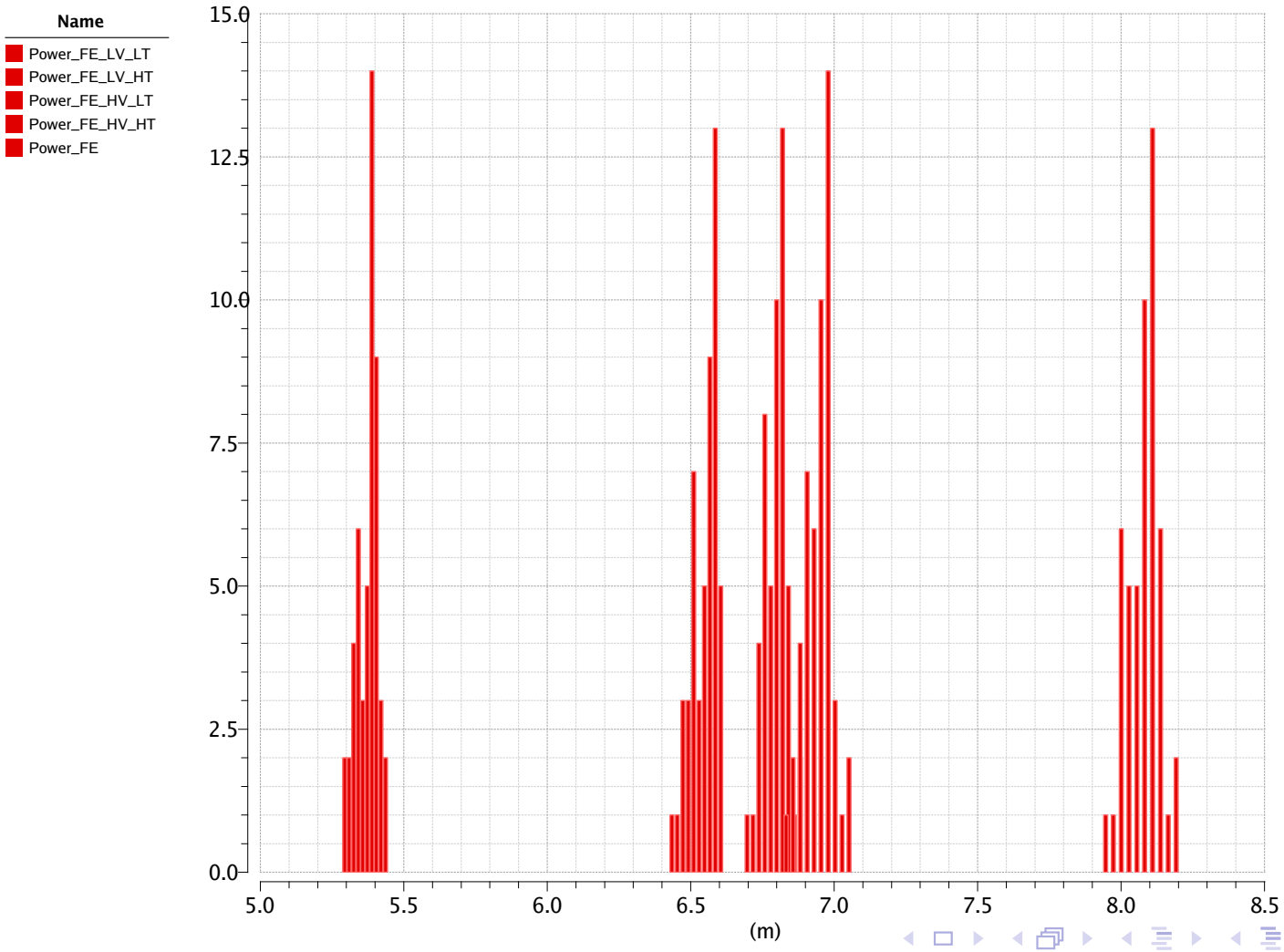
view: extracted **Model**: typ **Temp**:27C **VDD**:1.25V

Power: Frontend + ADC = 8.9mW @ $V_{DD} = 1.25V$



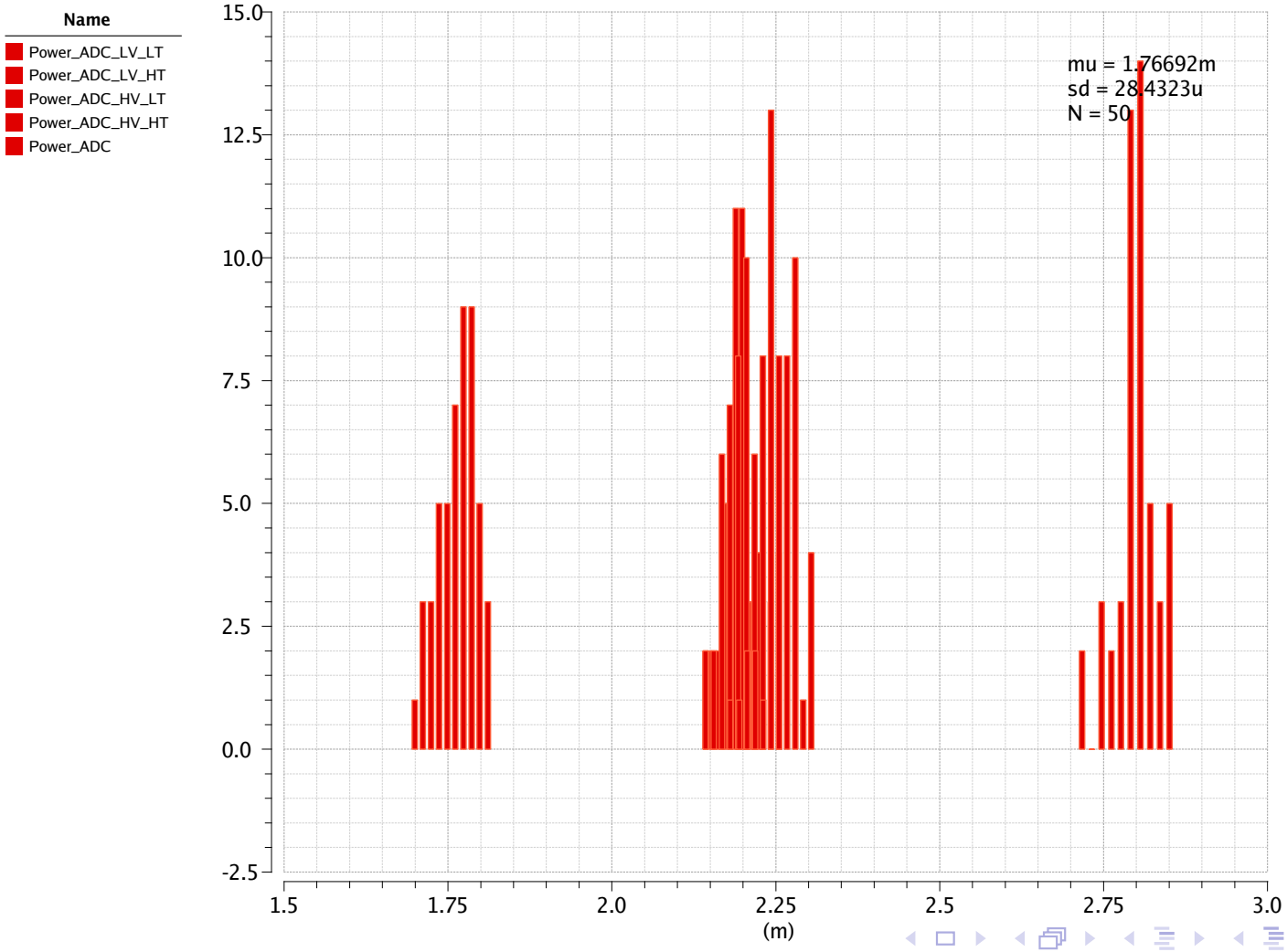
Power: Frontend

view: extracted **Model**: MC **Temp**:LT,HT **VDD**:LV,HV



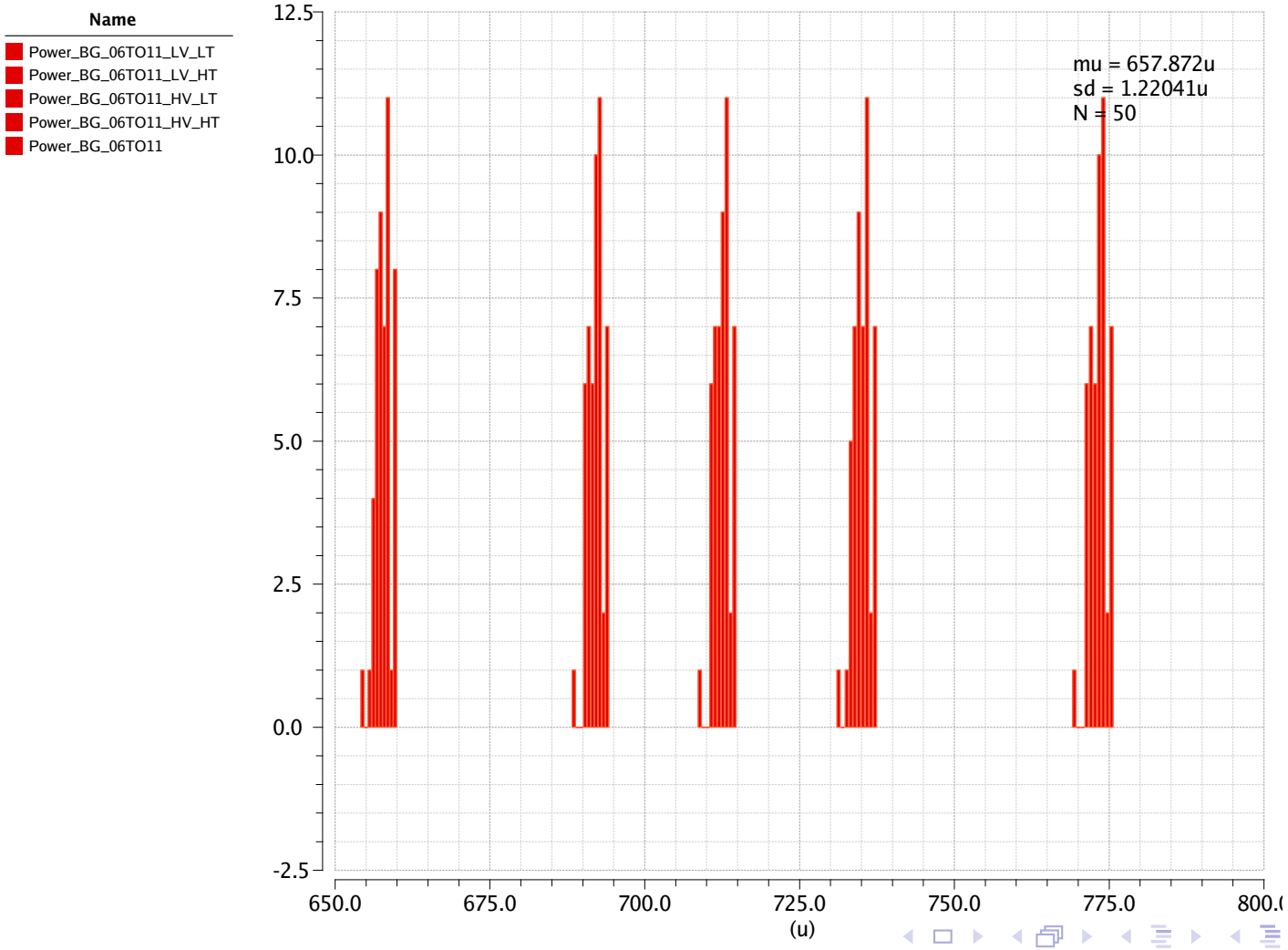
Power: ADC

view: extracted **Model**: MC **Temp**:LT,HT **VDD**:LV,HV



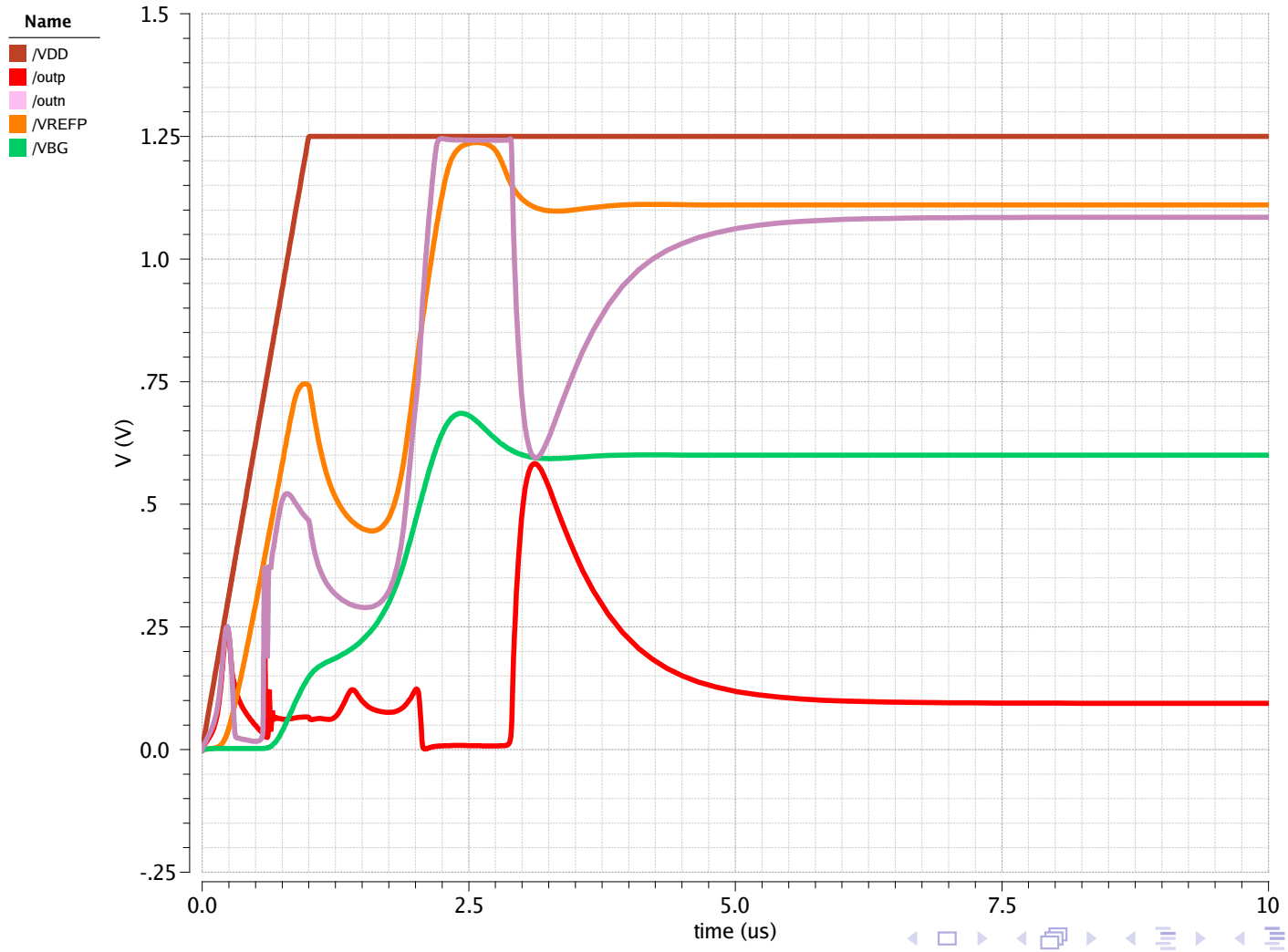
Power: Bandgap + 0.6to1.1 converter + Bias

view: extracted **Model**: MC **Temp**:LT,HT **VDD**:LV,HV



Power-on: Trasient simulation

view: extracted **Model**: tpy **Temp**:27C **VDD**:1.25V



Question

Matching simulations of common mode control and ADC buffer needs to be done with realistic corners.

Common mode variation @160ns 30mV/fC

view: extracted **Model**: MC **Temp**:LT,HT **VDD**:LV,HV

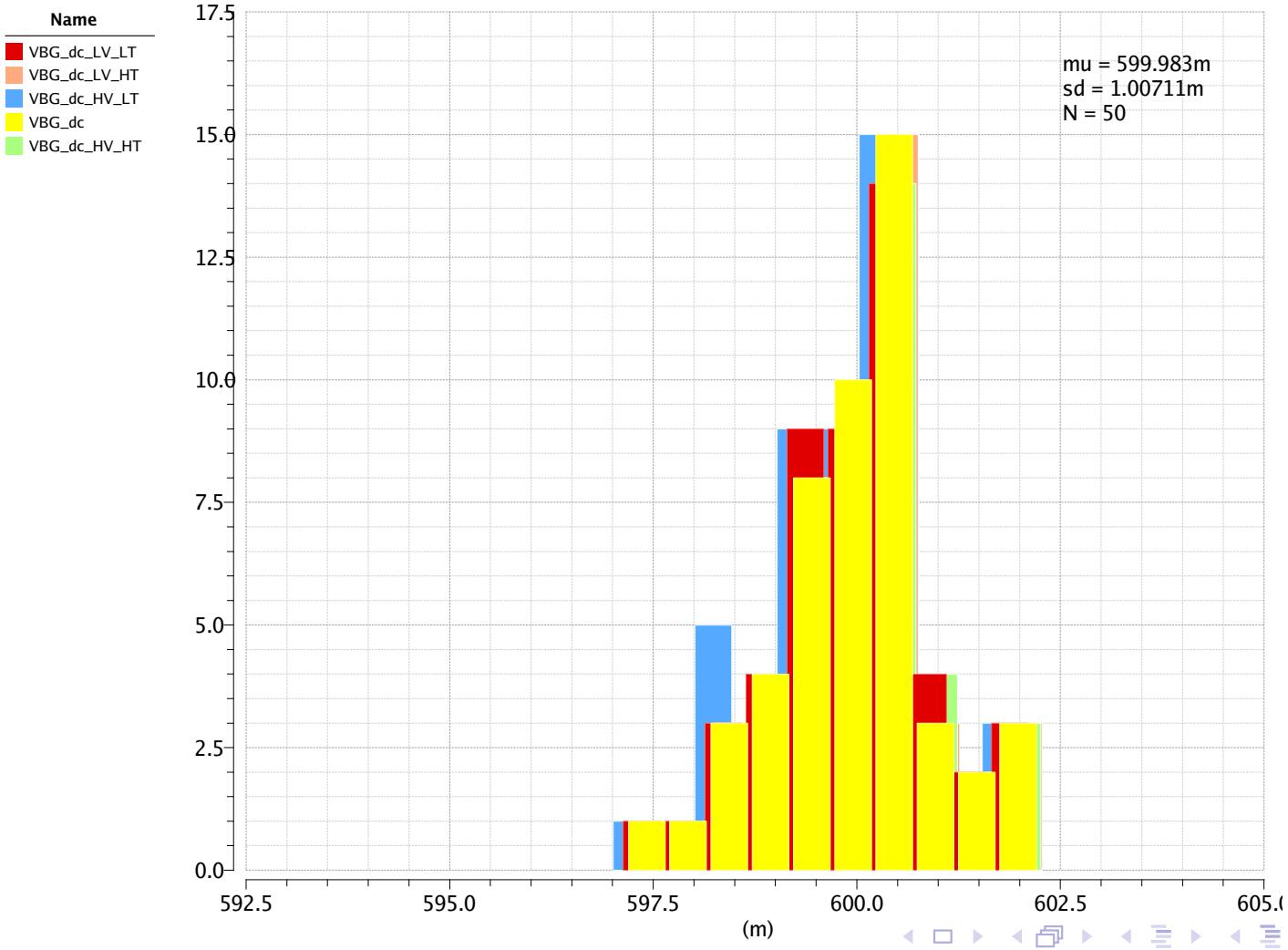
Test	Name	Yield	Min	Target	Max	Mean	Sigma to
Parameters: Yield Estimate: 100 %(50 passed/50 pts)				Confidence Level: <not set>			
–	SAMPA_voltref:sim_vrefp:1						
	– VCM(summary)	100	582.8m		604.3m	591.7m	
	VCM	100	583.6m	info	599.1m	589.8m	
	VCM_HV_HT	100	582.8m	info	598.5m	589.3m	
	VCM_HV_LT	100	589.7m	info	604.3m	596.1m	
	VCM_LV_HT	100	585.6m	info	601m	592m	
	VCM_LV_LT	100	584.9m	info	600.1m	591.3m	
	– Voutn_dc(summary)	100	1.021		1.078	1.047	
	Voutn_dc	100	1.022	info	1.076	1.047	
	Voutn_dc_HV_HT	100	1.021	info	1.075	1.046	
	Voutn_dc_HV_LT	100	1.025	info	1.078	1.049	
	Voutn_dc_LV_HT	100	1.022	info	1.076	1.047	
	Voutn_dc_LV_LT	100	1.023	info	1.077	1.047	
	– Voutp_dc(summary)	100	105.4m		167m	136.3m	
	Voutp_dc	100	106.2m	info	159.1m	133.1m	
	Voutp_dc_HV_HT	100	105.4m	info	159m	132.7m	
	Voutp_dc_HV_LT	100	119.7m	info	167m	142.9m	
	Voutp_dc_LV_HT	100	111.4m	info	162.9m	137.4m	
	Voutp_dc_LV_LT	100	109.1m	info	160.7m	135.1m	

Question

- **The effect of the bandgap reference variation due to process variation needs to be translated to impact in gain/pulse width.**
- **Simulation of individual blocks and the full system must be presented in more detail**

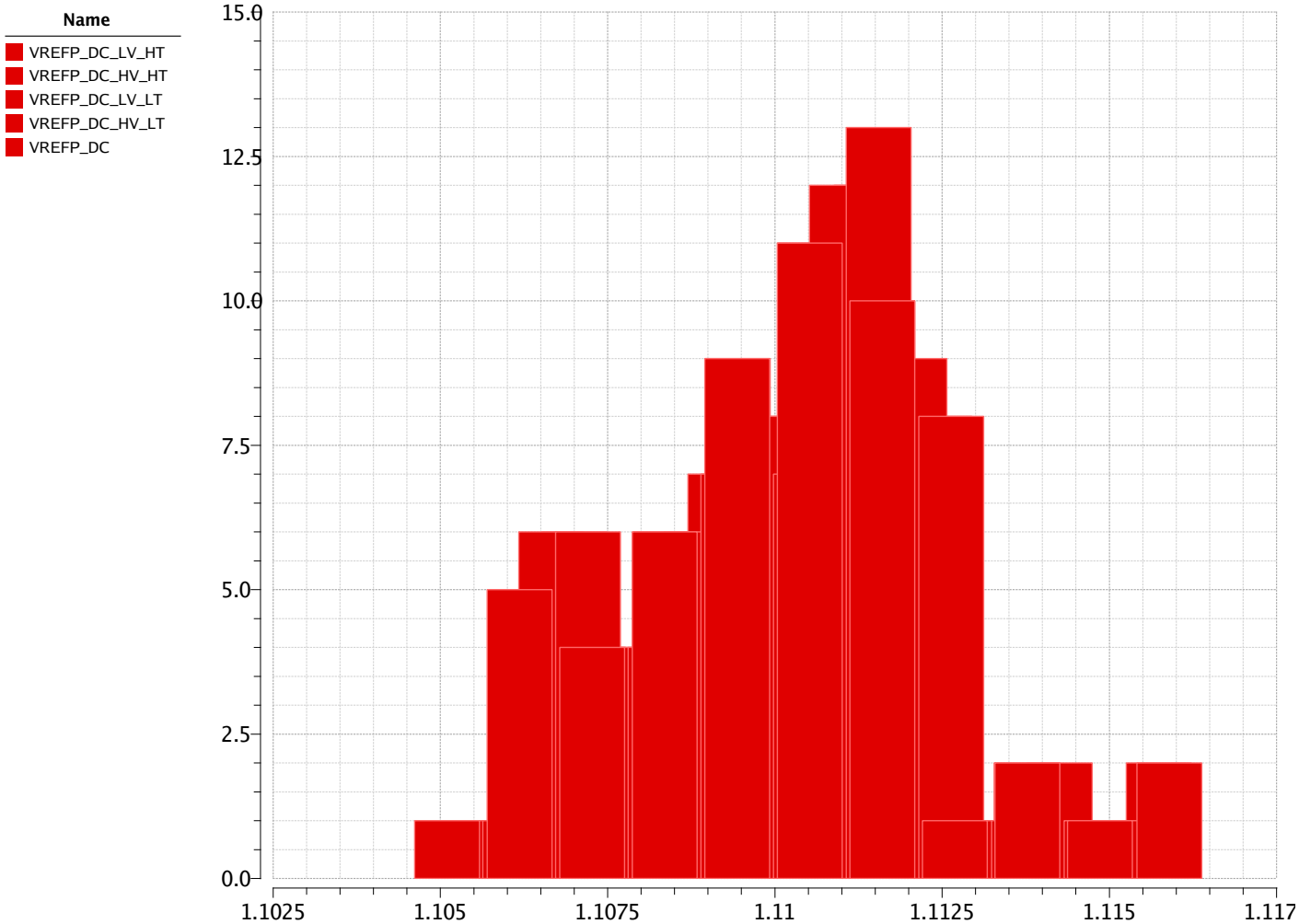
Bandgap voltage variation in the system simulation

view: extracted **Model**: MC **Temp**:LT,HT **VDD**:LV,HV



VREFP variation in the system simulation

view: extracted **Model**: MC **Temp**:LT,HT **VDD**:LV,HV



Frontend sim: FE + Bias + Bandgap (-) 160ns@20mV/fC

view: extracted **Model**: MC **Temp**:LT,HT **VDD**:LV,HV

Test	Name	Yield	Min	Target	Max	Mean	Sigma to Target	Sigma
Parameters: Yield Estimate: 100 %(50 passed/50 pts) Confidence Level: <not set>								
–	sampa_csa_shaper:sim_csa_shaper:1							
	– Amp(summary)	100	992.4m		1.022	1.008		2.737m
	– ENC(summary)	100	366.8		435.3	404.3		4.025
	– In_charge(summary)	100	47.54f		47.66f	47.6f		8.371a
	– Peaking time(summary)	100	143n		168n	154.9n		2.353n
	– Sensitivity(summary)	100	20.84		21.49	21.18		57.69m
	– Vout_max(summary)	100	-52.13m		63.55m	12.07m		21.37m
	– Vout_min(summary)	100	-1.05		-948m	-996.1m		19.84m
	– onoise(summary)	100	1.243m		1.465m	1.372m		16.17u

Frontend sim: FE + Bias + Bandgap (+) 300ns@4mV/fC

view: extracted **Model**: MC **Temp**:LT,HT **VDD**:LV,HV

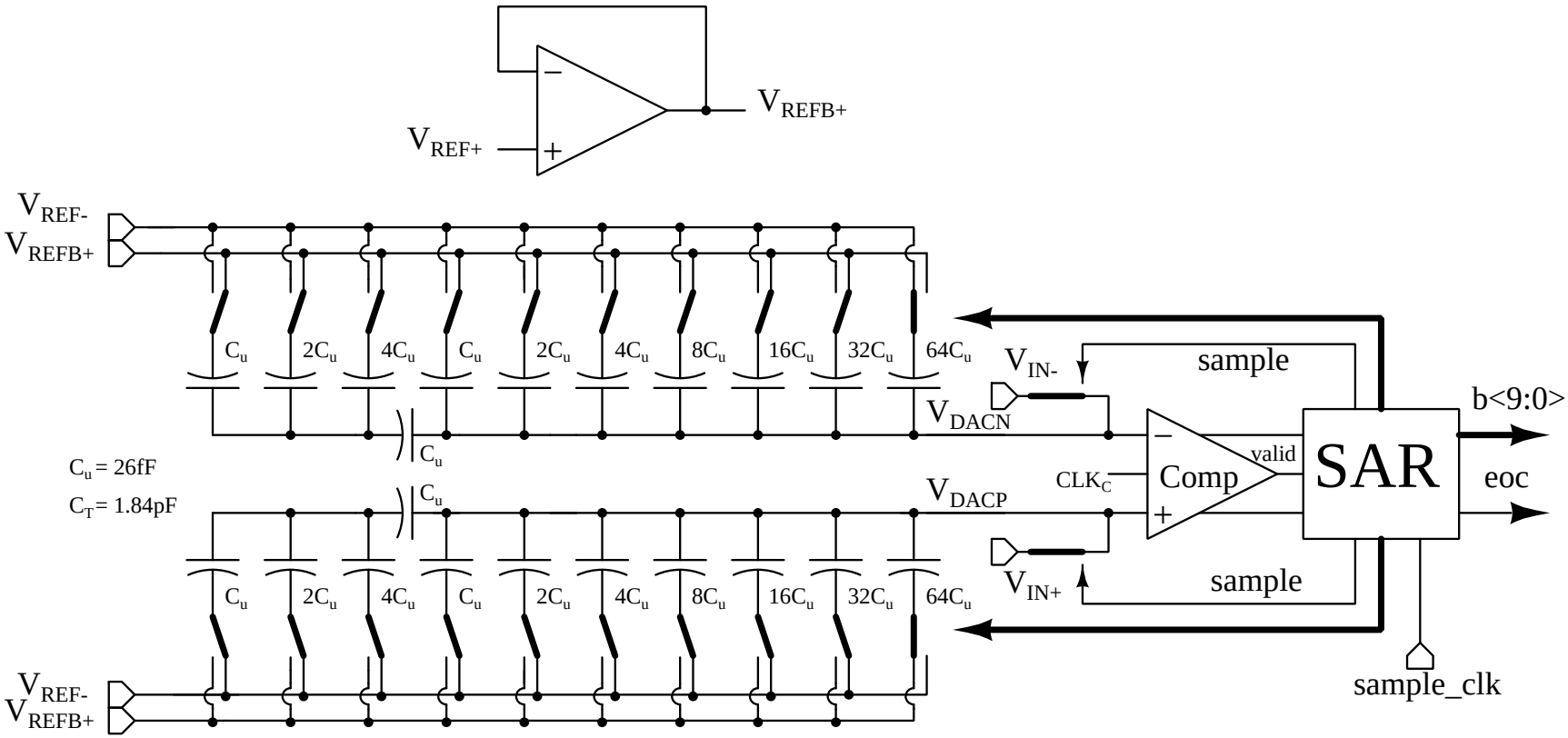
Test	Name	Yield	Min	Target	Max	Mean	Sigma to Target	Sigma
Parameters: Yield Estimate: 100 %(50 passed/50 pts) Confidence Level: <not set>								
–	sampa_csa_shaper:sim_csa_shaper:1							
	– Amp(summary)	100	992.4m		1.022	1.008		2.737m
	– ENC(summary)	100	366.8		435.3	404.3		4.025
	– In_charge(summary)	100	47.54f		47.66f	47.6f		8.371a
	– Peaking time(summary)	100	143n		168n	154.9n		2.353n
	– Sensitivity(summary)	100	20.84		21.49	21.18		57.69m
	– Vout_max(summary)	100	-52.13m		63.55m	12.07m		21.37m
	– Vout_min(summary)	100	-1.05		-948m	-996.1m		19.84m
	– onoise(summary)	100	1.243m		1.465m	1.372m		16.17u

Question

- **ADC performance must be studied in post-layout simulations (9.2 bit come from schematic simulations)**
- **Input capacitance to ADC is very high (20 pF), thus the buffer needs to be strong and the consumption is higher. In comparable design 2 pF can be achieved.**

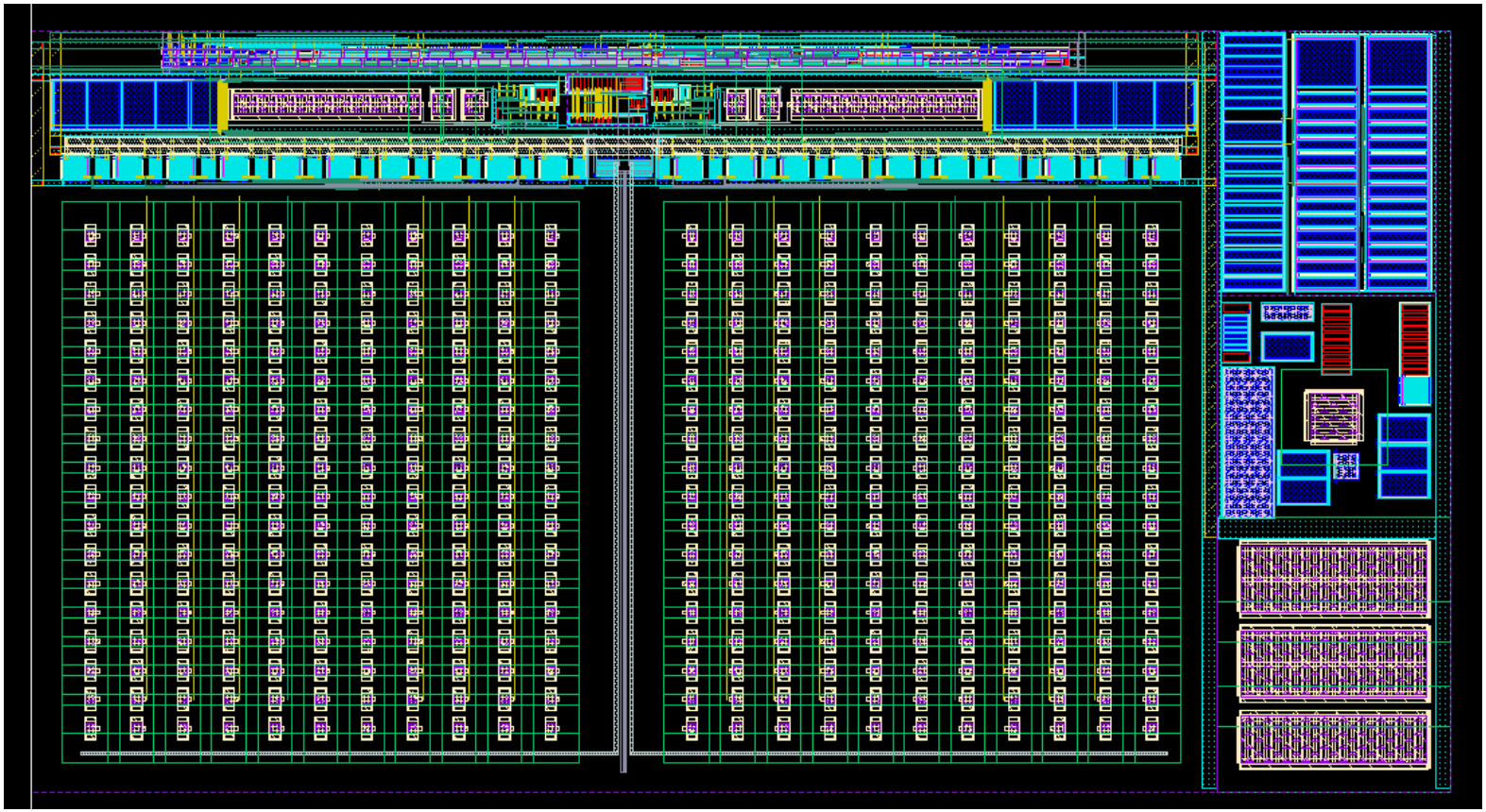
MPW2: New ADC capacitor array

Split Capacitor Array

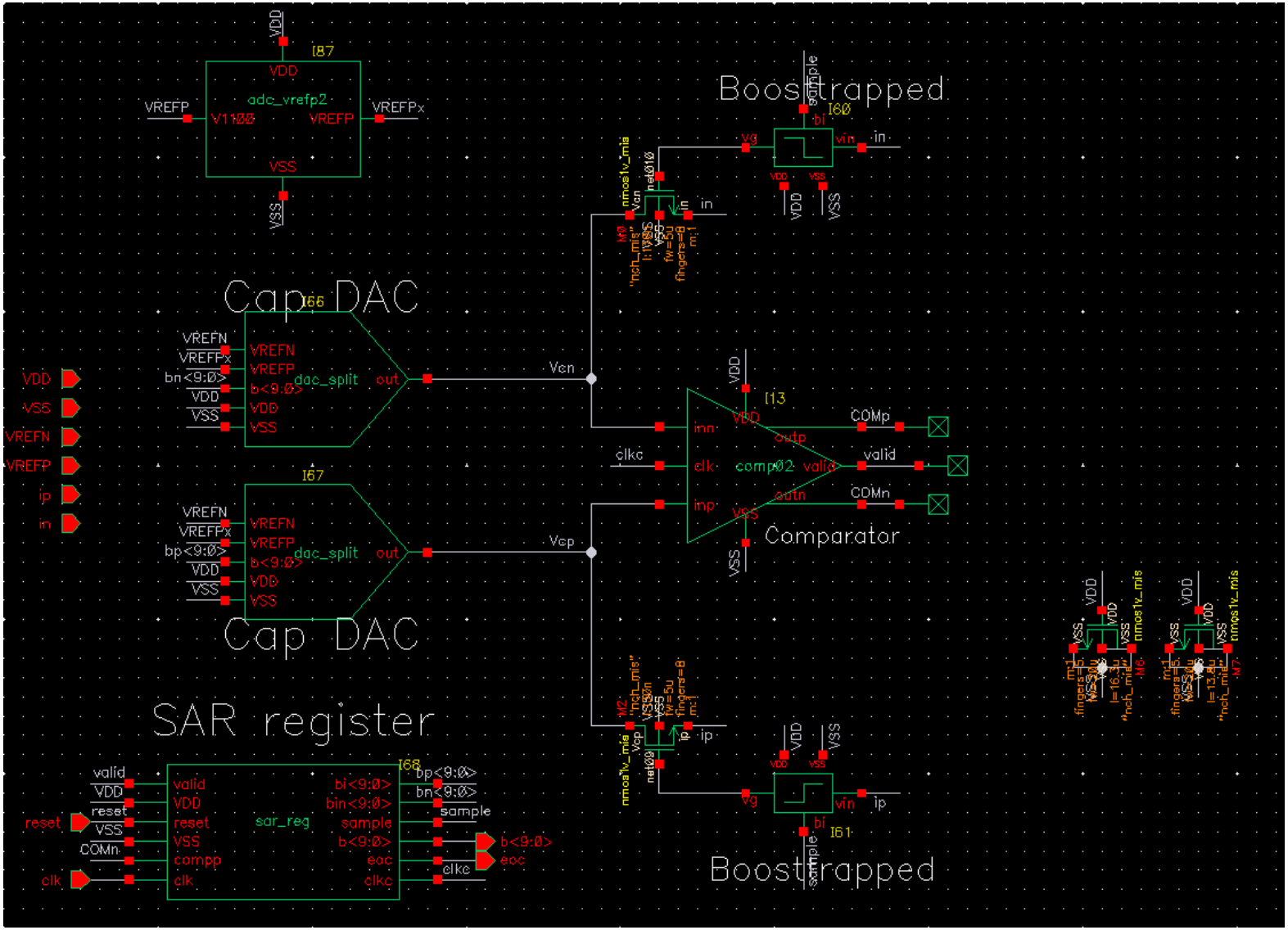


MPW2: New ADC capacitor array (Layout)

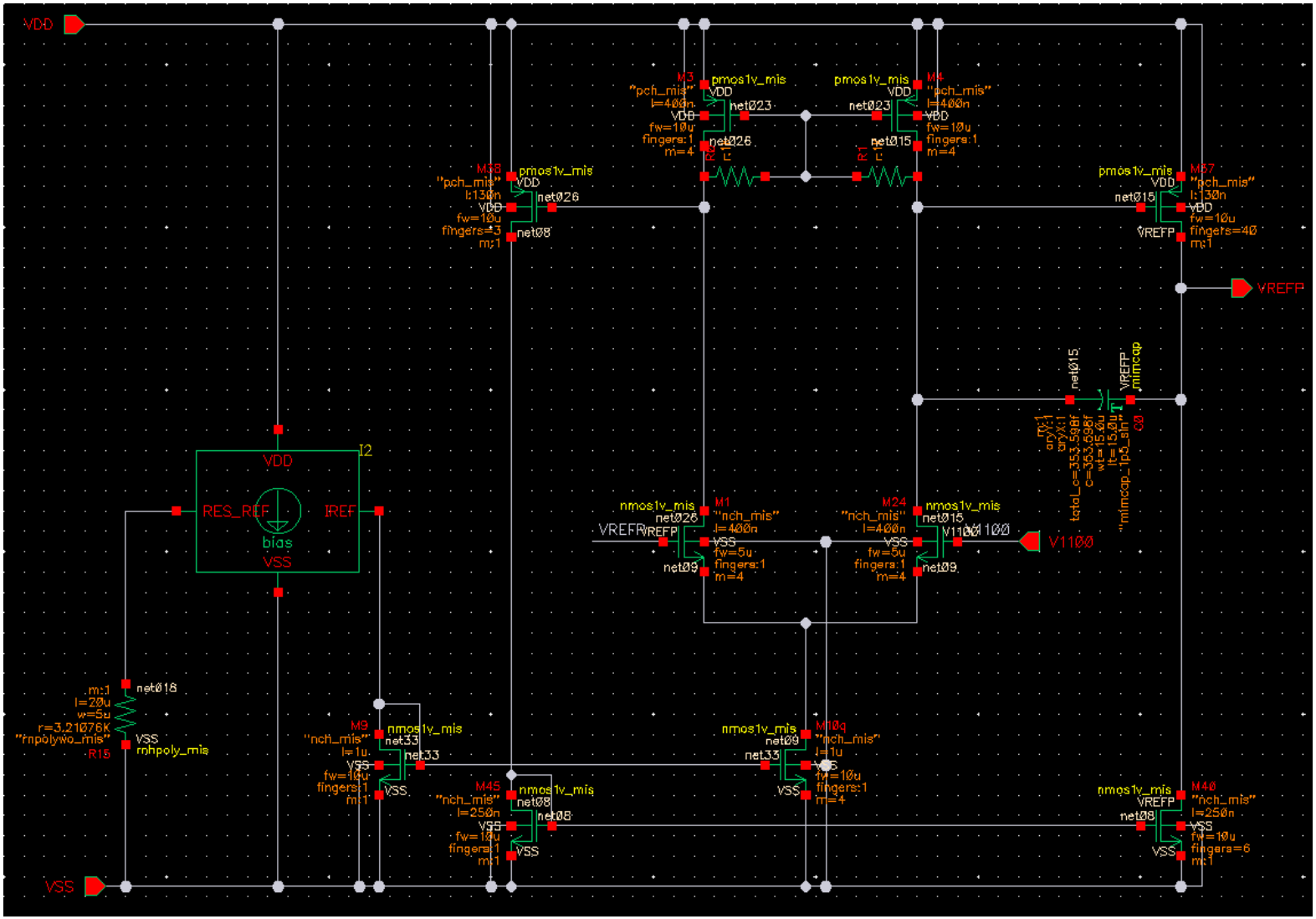
Split Capacitor Array



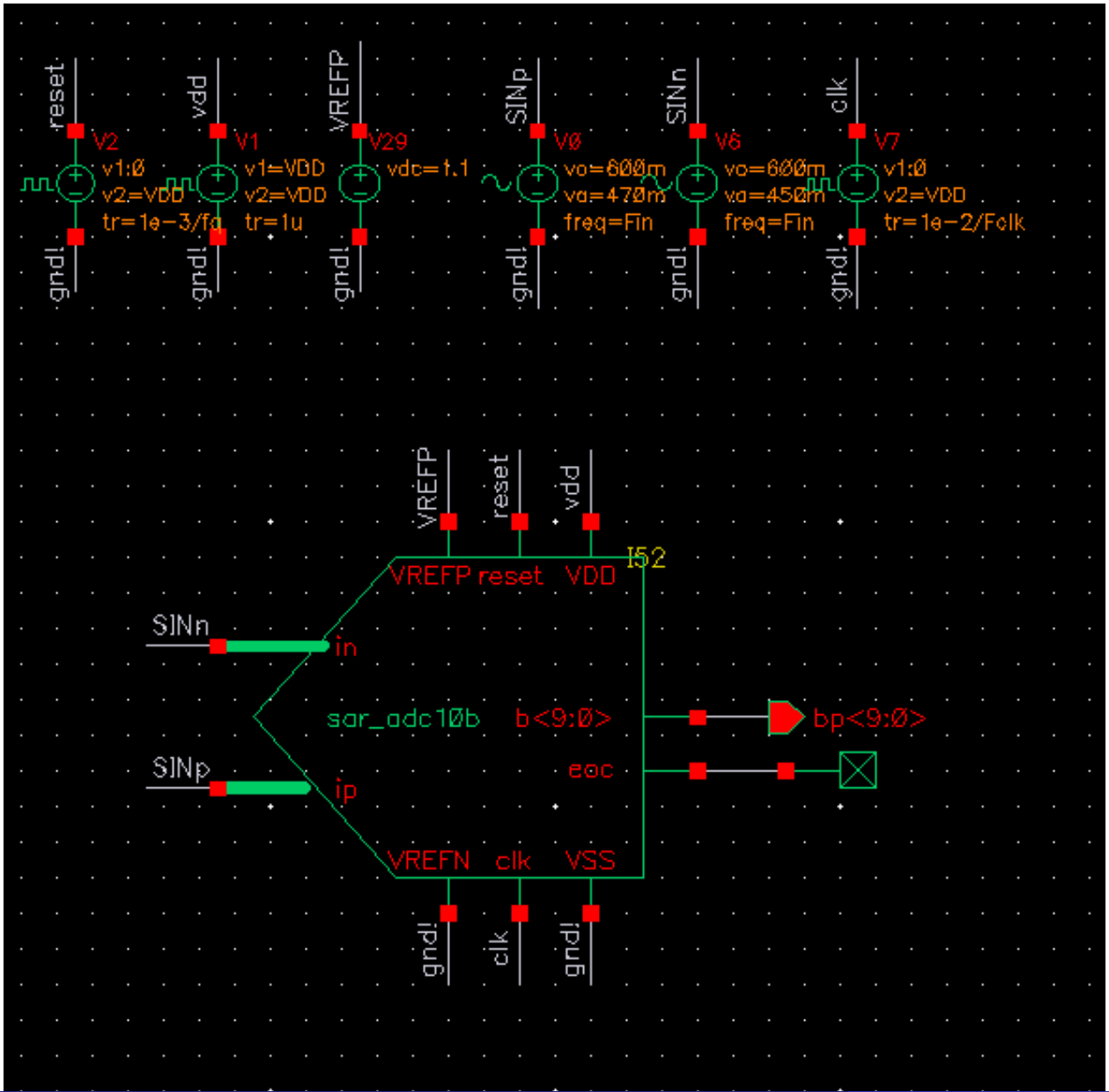
MPW2: ADC schematic



MPW2: Volatge reference Buffer



MPW2: ADC simulation testbench



MPW2: ADC simulations

View: extracted
Model: Corners: typ-ff-ss
Temp: 0C-50C
VDD: 1.1875V
OBS: Ns=64 Fs=20Msps VREFP=1.1V VREFN=0V

temperature 27

	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	L
:1	ENOB	9.745				9.723	9.942	
:1	SFDR	68.25				66.63	70.13	

MPW2: ADC simulations

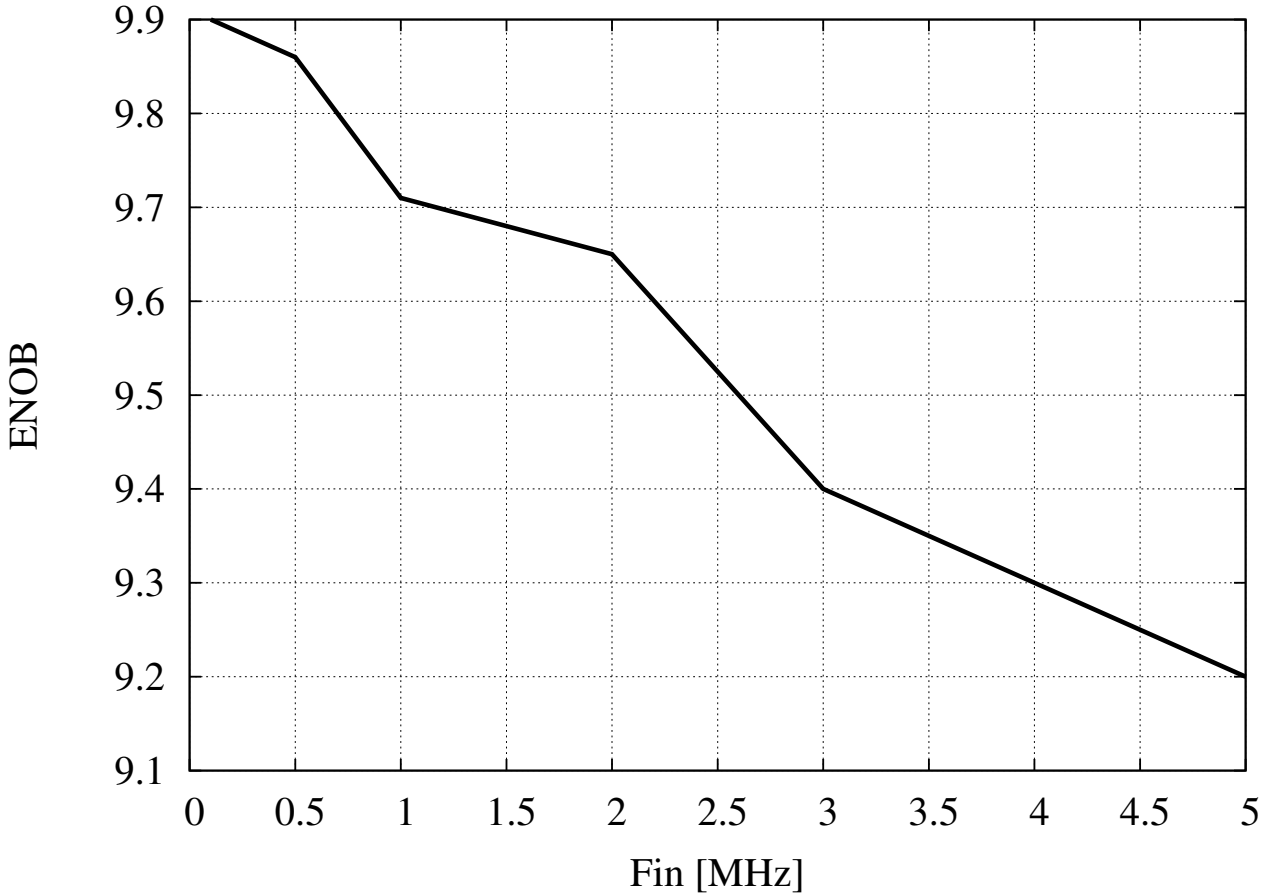
View: extracted
Model: Corners: typ-ff-ss
Temp: 0C-50C
VDD: 1.325V
OBS: Ns=64 Fs=10Msps VREFP=1.1V VREFN=0V

temperature 27

	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	L
:1	ENOB	9.745				9.723	9.942	
:1	SFDR	68.25				66.63	70.13	

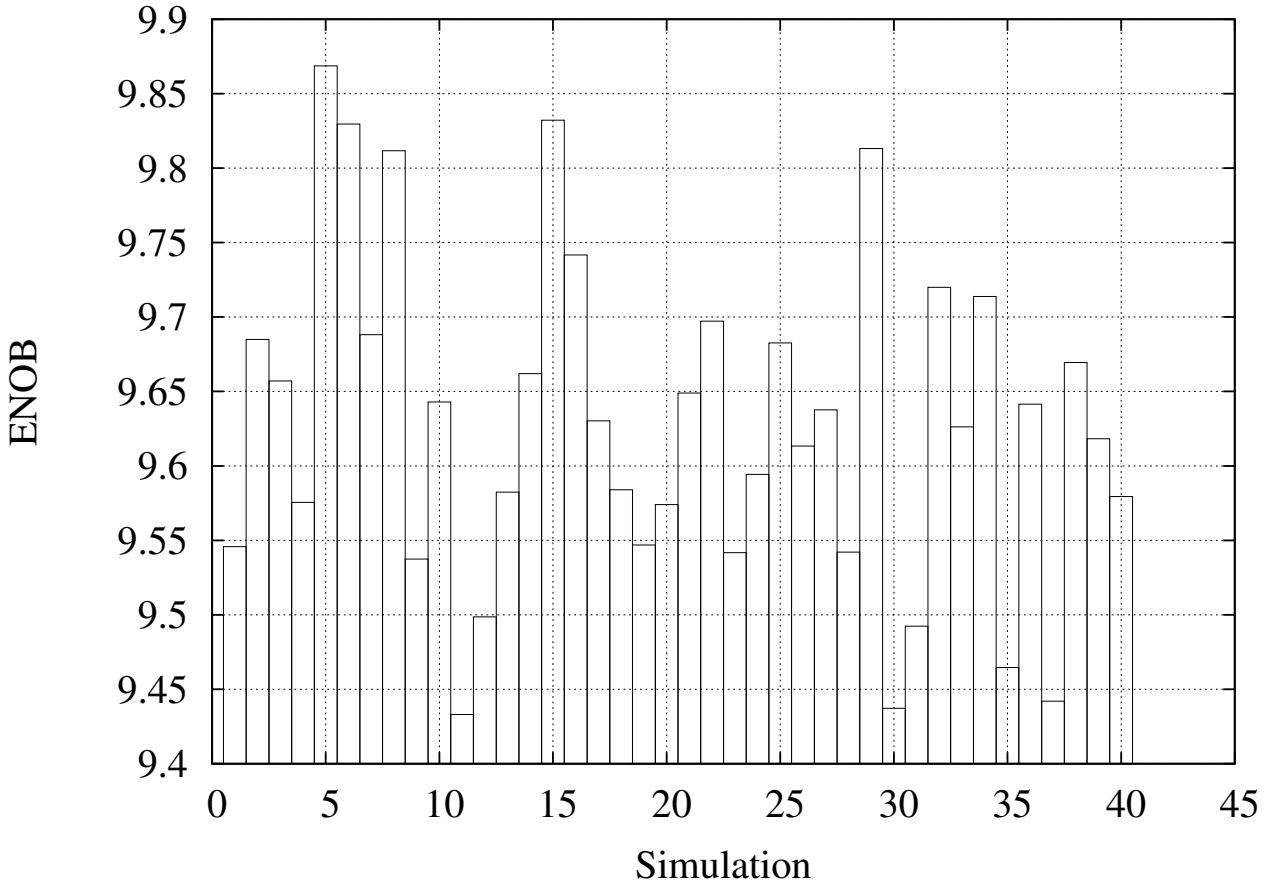
MPW2:ENOB vs Fin

N=256, Fs=10MHz, VDD=1.25V , VREFP=1.1V, model=typ



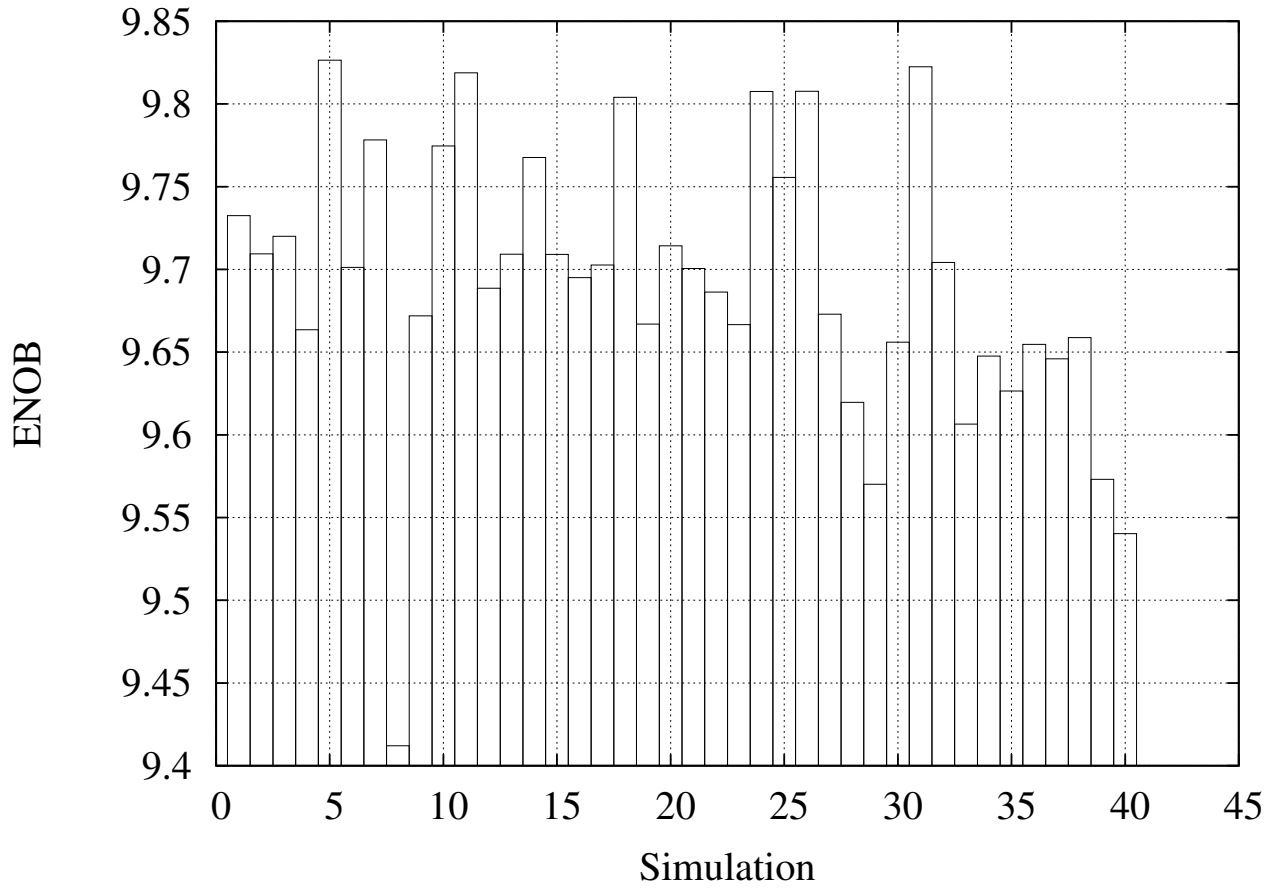
MPW2:ENOB Fin=2e6

N=256, Fs=10MHz, VDD=1.25V , VREFP=1.1V, model=MC

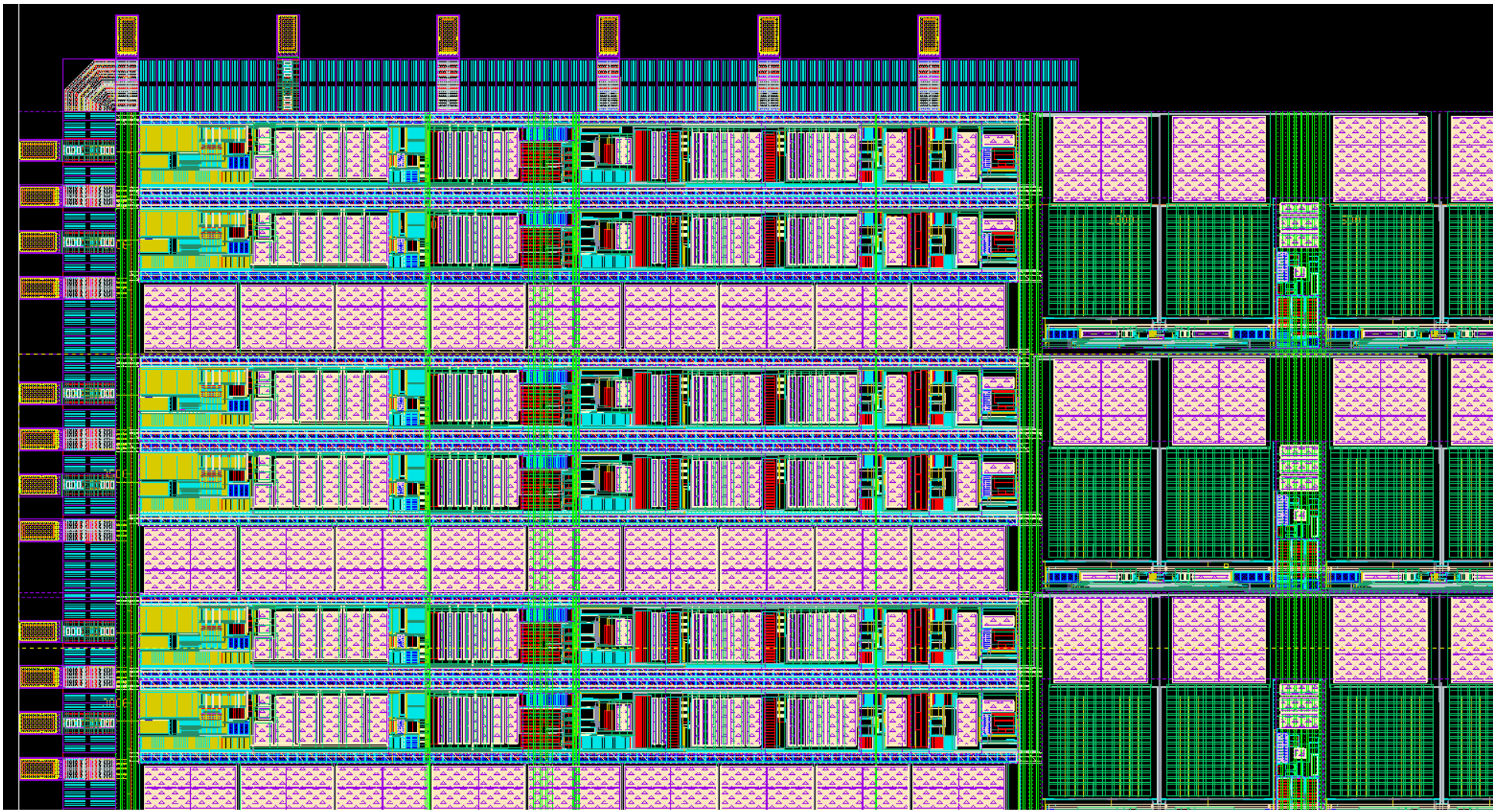


MPW2:ENOB Fin=1e6

N=256, Fs=10MHz, VDD=1.25V , VREFP=1.1V, model=MC



MPW2 Status: layout



MPW2 Status

- Layout of Frontend - ADC - Analog Block: ready
- Layout SLVDS driver (Rx and Tx) is being performed
- System post-layout simulations to calculate the decoupling capacitors from the noise requirements are being performed.
- More post-layout simulations including packages and board effects are being performed.

SAMPA:Voltage Reference Design

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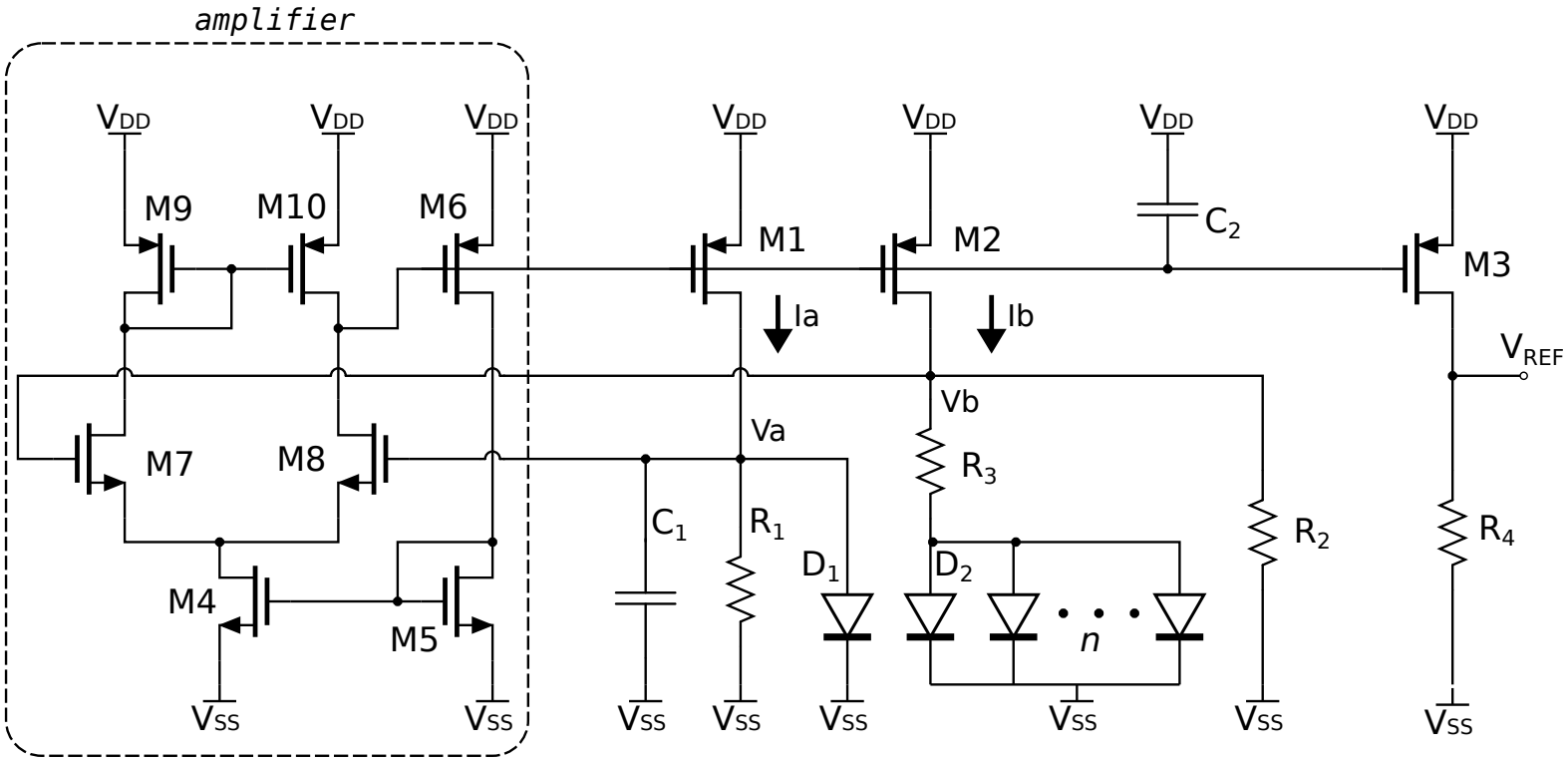
April 1, 2015

Voltage Reference Design

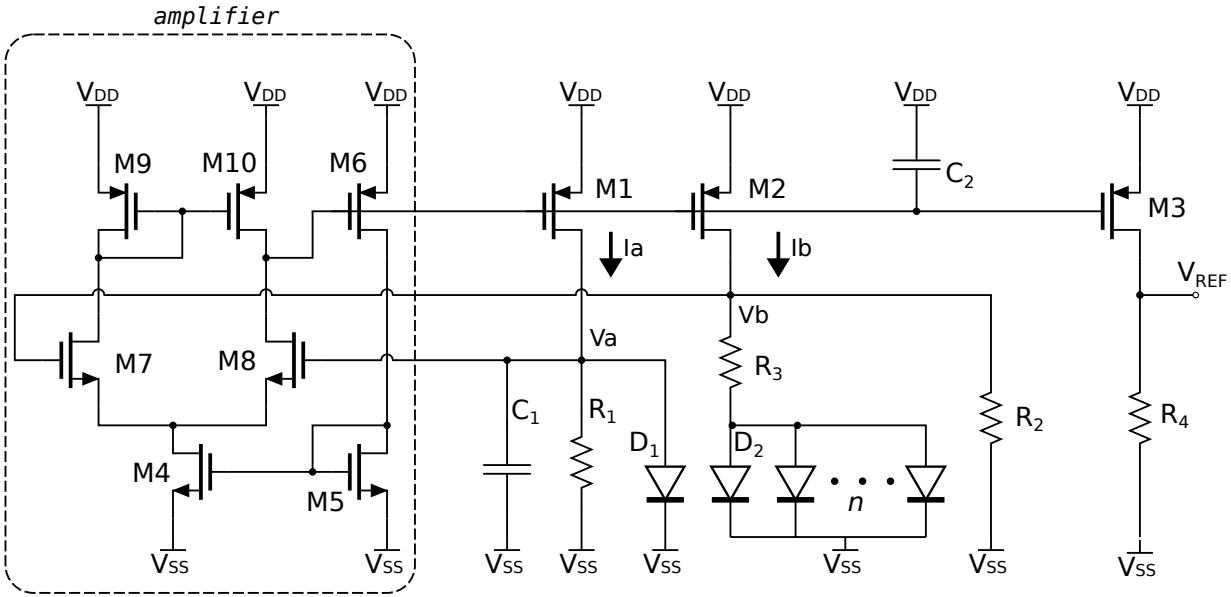
Name	Target
Output Voltage (mV)	600
Temperature Coefficient (ppm V/ºC)	<30
Line Regulation (mV/V)	<10
Output Noise (µV)	<5
Power Supply Rejection Ration (dB)	>35

Voltage Reference - Topology



[Banba et al., 1999]: Hironori Banba, Hitoshi Shiga, Akira Umezawa, Takeshi Miyaba, Toru Tanzawa, Shigeru Atsumi, and Koji Sakui, A CMOS bandgap reference circuit with sub-1-V operation JSSC, vol. 34, no. 5, may 1999

Voltage Reference - Dimensions

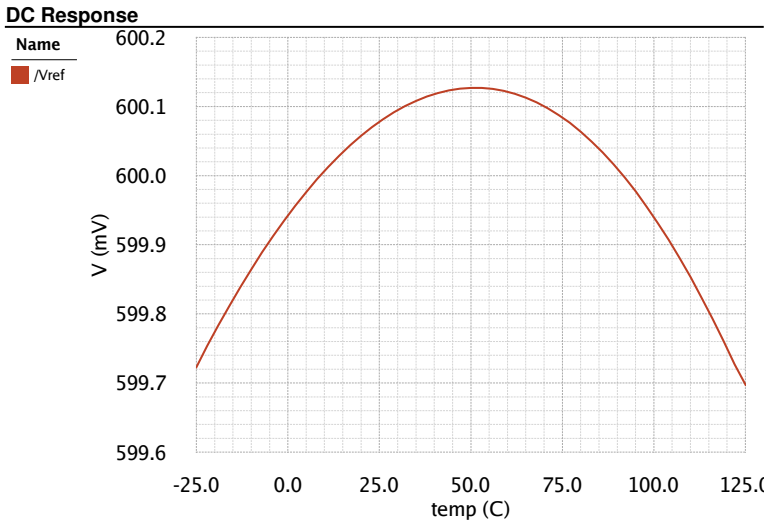


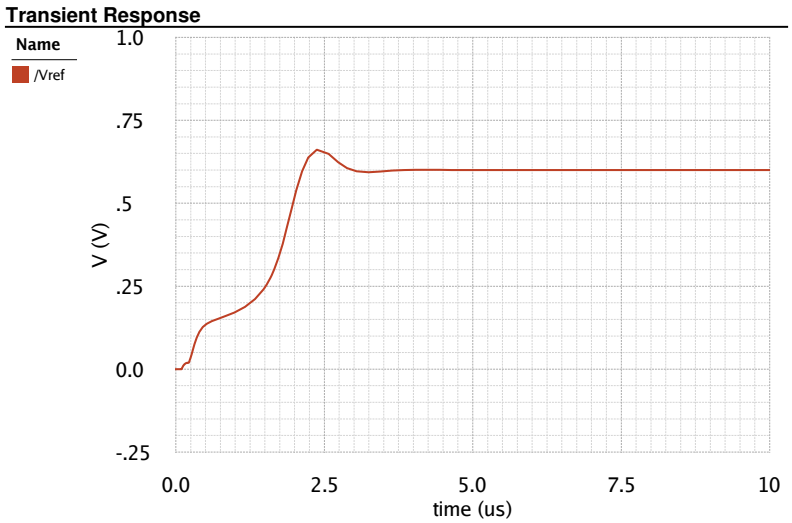
Device	Dimensions (µm)
M1, M2, M3	53.5 / 6.63 (X5)
M4	2.33 / 0.92 (X2)
M5	2.33 / 0.92 (X3)
M6	53.5 / 6.63 (X2)
M7, M8	22.95 / 19.8 (X4)
M9, M10	30.8 / 7.43 (X10)
D1,D2	29.7 / 29.7
n	17
R1, R2	Resistance: 12.6 [kΩ]
R3	Resistance: 1.7 [kΩ]
R4	Resistance: 6.1 [kΩ]
C1, C2	Capacitance: 4 [pF]

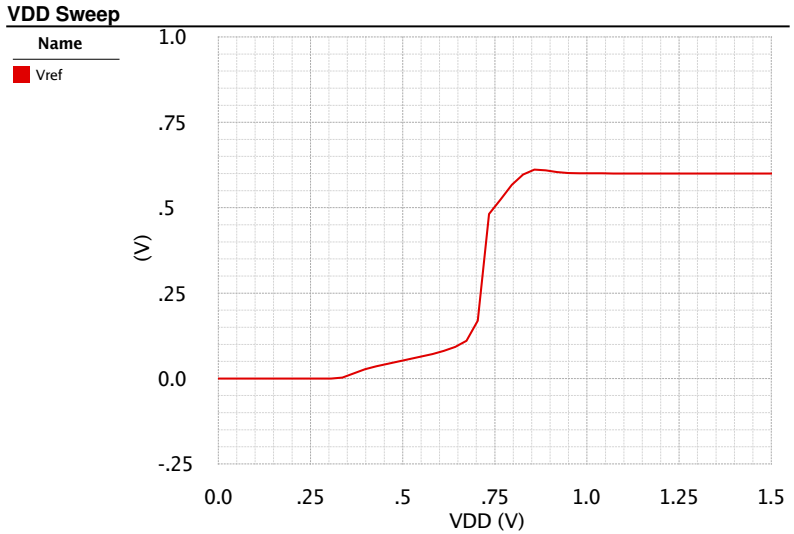
Voltage Reference - Nominal Results

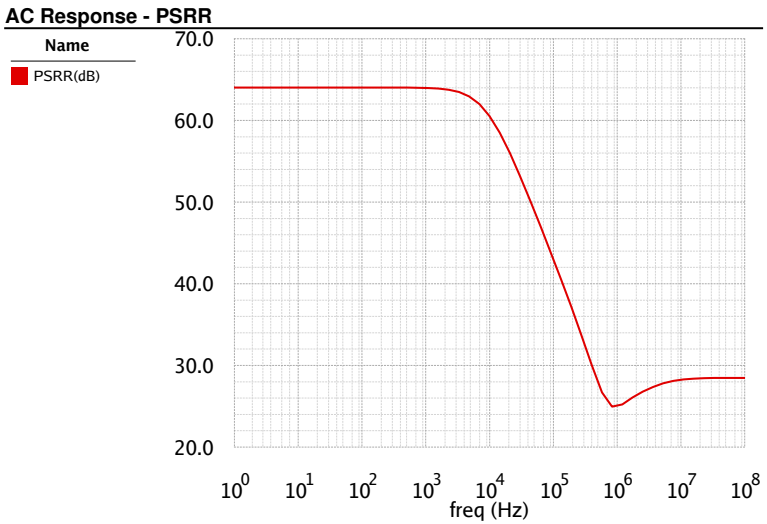
Name	Simulation Results
Output Voltage	600.097 mV
Temperature Coefficient	4.29 ppm V/ºC
Line Regulation	629 µV/V
Output Noise	844,6 nV
Power Supply Rejection Ration	64 dB
Power Comsumption	432.7 µW

Voltage Reference - Output Waveforms

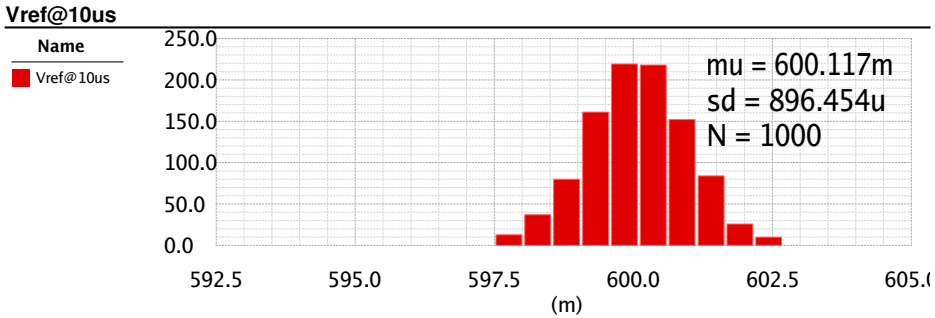


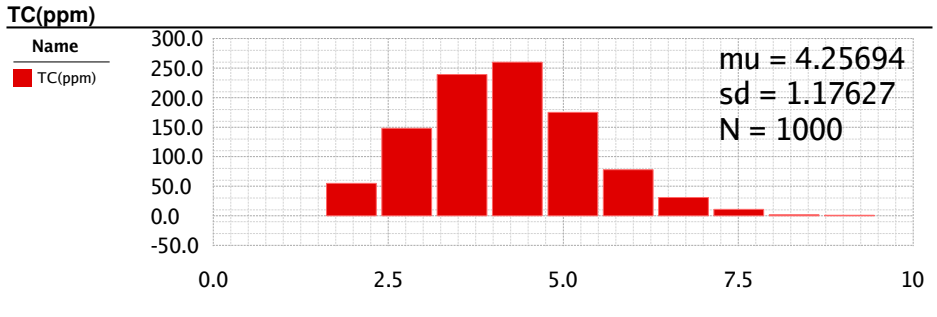


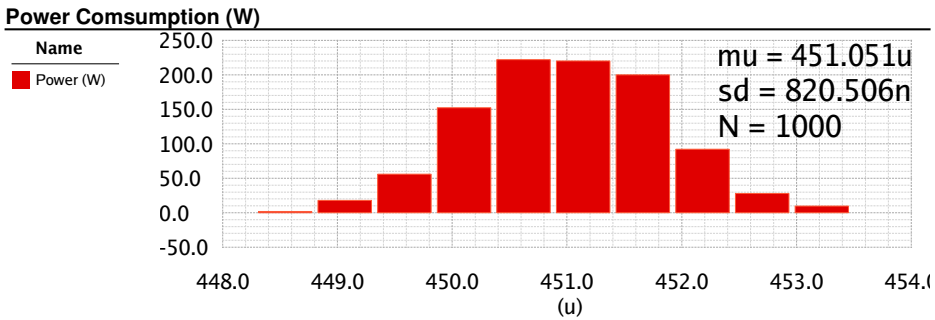


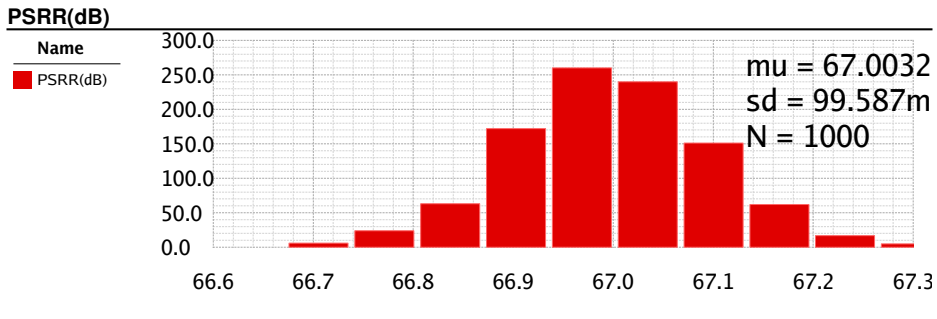


Voltage Reference - Montecarlo

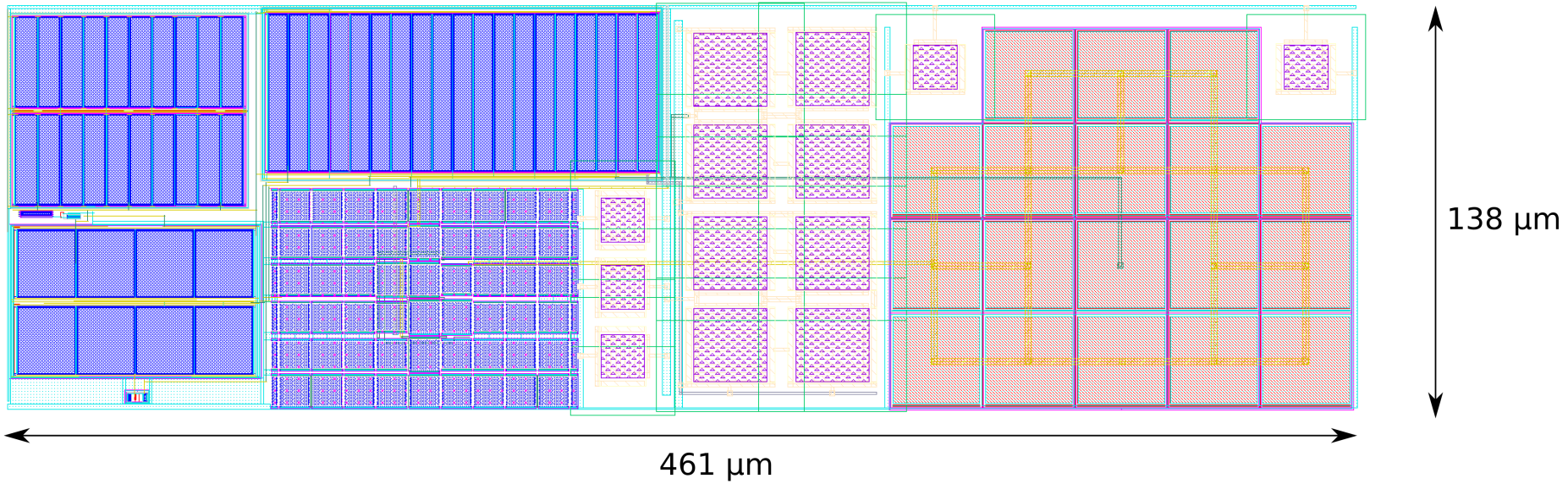








Voltage Reference - Layout



Voltage Reference - Layout (regions)