

# SAMPA: MPW2 Design review

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# Definitions

## **Corners:**

LV=1.1875V

HV=1.325V

LT=0°C

HT=50°C

## **Models:**

typ= Typical

ss= Slow

ff = fast

MC=Monte Carlo

**The analog power domain needs to be protected from the digital noise environment. NT\_N division trenches need to be implemented. The use of triple well transistors should be considered.**

# Triple-well implementation: TSMC recommendation

Applications Places System Tue Jan 27, 10:40 AM Hugo Daniel Hernandez Herrera

T013L0DR001\_2\_5.pdf - Konqueror (on Inxmic3)

Location Edit View Go Bookmarks Tools Settings Window Help

Location: /usr/local/admicsoft/TSMC130/fimcc-20140314/doc/T013L0DR001\_2\_5.pdf

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If the MW of the checked PUJOS interacts with the DNW, the space needs to follow A or C.

If voltage  $V_a \gg V_b$ , the space can be  $< A$  or  $< C$

Guard ring is not necessary  $V_a \gg V_b$ , but P+ STRAP is still required.

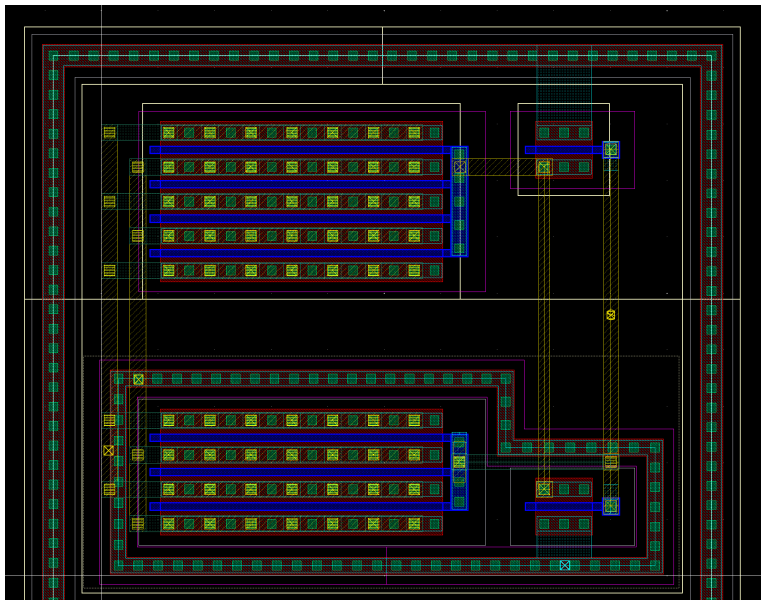
Guard ring and P+ STRAP are not necessary if  $V_a \gg V_b$ .

Figure 10.1.2.3.2

TSMC Confidential Information ©2014 International Rectifier/Infineon Technologies AG

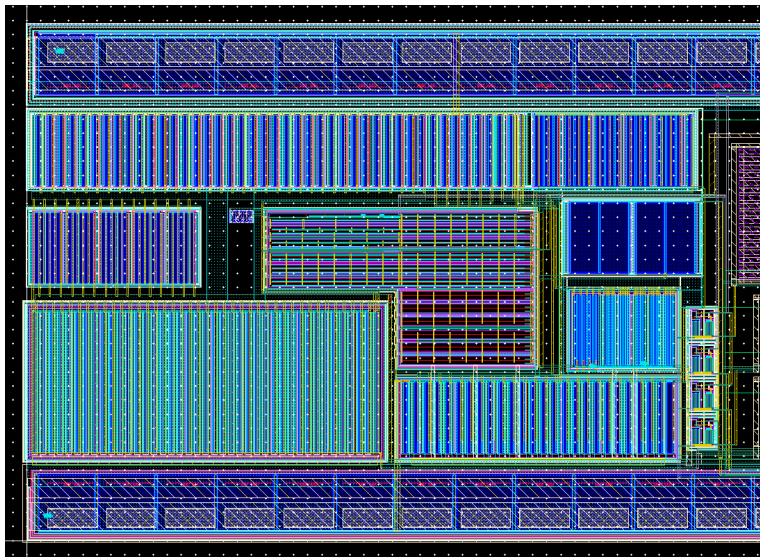
hueman@pc... Project SAMPA... virtuoso (on In... Triple Well Isol... [Cadence Libr... tr\_gate\* (on I... T013L0DR001... /projects/TSM... [VLSV (on Inxmic... tr\_gate (on Inxmic...

# Triple-well implementation: Example



# NMOS transistors of the frontend are triple\_well

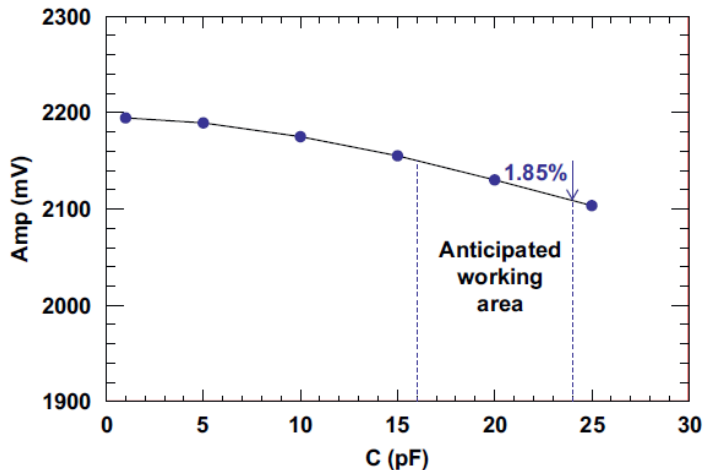
CSA layout implemented with triple-well option



**It was commented that the CSA has no boosting transistors. According to the experience of the reviewers they are necessary in TSMC 130 as the transistor gain is not sufficient. The concern is that the CSA response depends strongly on the detector capacitance. Thus, it is required to study in simulation and test (MPW1), the dependence on capacitance**

# ENC vs Cd: PASA

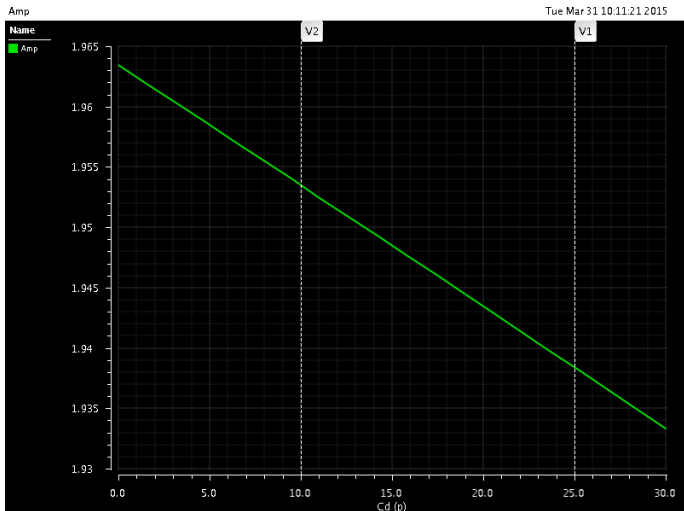
Amplitude variation of the PASA impulse response as a function of total detector capacitance = 1.85% (12pF-25pF)





# ENC vs Cd: SAMPA 160ns@20mV/fC

Amplitude variation of the SAMPA impulse response as a function of total detector capacitance = 0.76% (12pF-25pF)



- **There could be room for power consumption reduction. The CSA part of the circuit is nearly the same as TPC PASA and had 11 mW with 3.3 V power supply. So theoretically, the SAMPA CSA should be around 4-5 mW, and still fulfill the requirements**
- **The power consumption must be detailed for different building blocks and the power domains.**

# Power: Frontend - ADC - Bandgap

**view:** extracted **Model:** typ **Temp:**27C **VDD:**1.25V

**Power:** Frontend + ADC = 8.9mW @  $V_{DD} = 1.25V$

The screenshot shows the Cadence Virtuoso Analog Design Environment interface. The main window title is "Virtuoso® Analog Design Environme...shaper sim\_csa\_shaper\_adc schematic". The menu bar includes "Launch", "Session", "Setup", "Analyses", "Variables", "Outputs", "Simulation", "Results", "Tools", and "Help". The "Design Variables" table is visible on the left, and the "Analyses" and "Outputs" panels are on the right.

Name	Value
1 Cd	18.5p
2 VDD	1.25
3 Fclk	80M
4 fq	10M
5 pol	-1
6 Charge_input	0
7 tr	1n
8 Rs	0
9 cts1	0
10 cts0	1
11 cg0	0
12 cg2	0
13 cg1	0

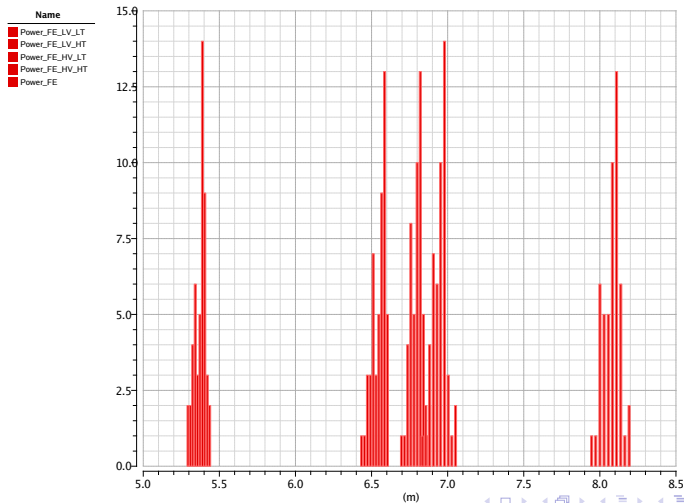
Type	Enable	Arguments
1 tran	<input checked="" type="checkbox"/>	10u 10.1u moderate
2 dc	<input type="checkbox"/>	t

Name/Signal/Expr	Value	Plot	Save	Save Options
4 outp		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
5 Power_BG_06TO11	712.567u	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
6 Power_FE	6.79475m	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
7 Power_ADC	2.23758m	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
8 V13/PLUS		<input type="checkbox"/>	<input checked="" type="checkbox"/>	yes
9 V12/PLUS		<input type="checkbox"/>	<input checked="" type="checkbox"/>	yes

Plot after simulation: Auto Plotting mode: Replace

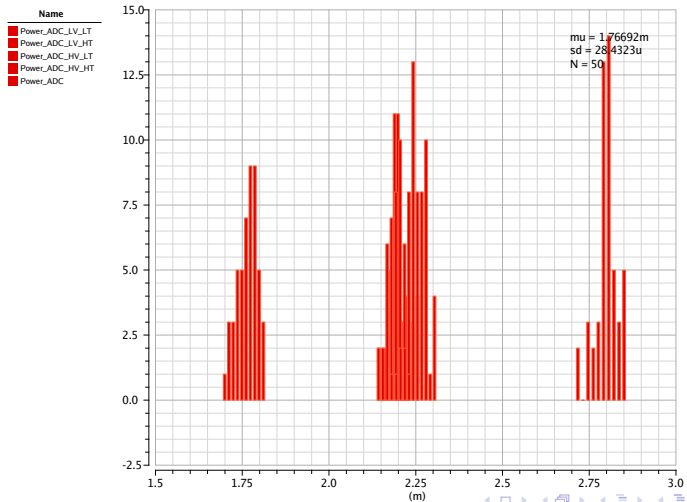
# Power: Frontend

**view:** extracted **Model:** MC **Temp:**LT,HT **VDD:**LV,HV



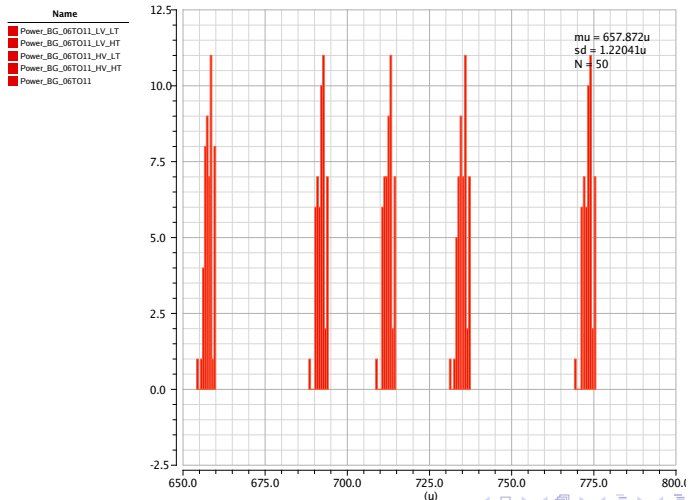
# Power: ADC

**view:** extracted **Model:** MC **Temp:**LT,HT **VDD:**LV,HV



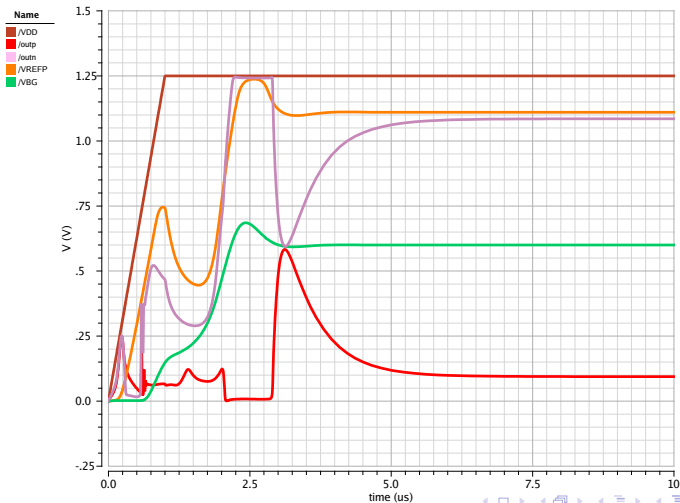
# Power: Bandgap + 0.6to1.1 converter + Bias

**view:** extracted **Model:** MC **Temp:**LT,HT **VDD:**LV,HV



# Power-on: Transient simulation

**view:** extracted **Model:** tpy **Temp:**27C **VDD:**1.25V



**Matching simulations of common mode control and ADC buffer needs to be done with realistic corners.**



# Common mode variation @160ns 30mV/fC

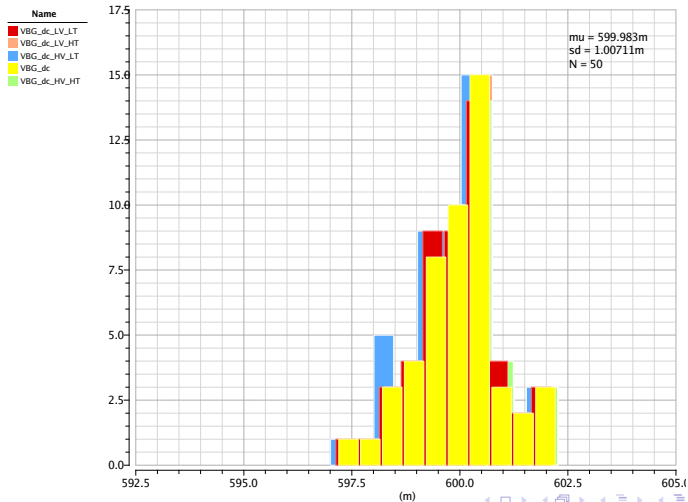
**view:** extracted **Model:** MC **Temp:**LT,HT **VDD:**LV,HV

Test	Name	Yield	Min	Target	Max	Mean	Sigma to
Parameters: Yield Estimate: 100 %(50 passed/50 pts) Confidence Level: <not set>							
-	⚙ SAMPA_voltref.sim_vrefp:1						
-	⚙ VCM(summary)	100	582.8m		604.3m	591.7m	
	VCM	100	583.6m	info	599.1m	589.8m	
	VCM_HV_HT	100	582.8m	info	598.5m	589.3m	
	VCM_HV_LT	100	589.7m	info	604.3m	596.1m	
	VCM_LV_HT	100	585.6m	info	601m	592m	
	VCM_LV_LT	100	584.9m	info	600.1m	591.3m	
-	⚙ Voutn_dc(summary)	100	1.021		1.078	1.047	
	Voutn_dc	100	1.022	info	1.076	1.047	
	Voutn_dc_HV_HT	100	1.021	info	1.075	1.046	
	Voutn_dc_HV_LT	100	1.025	info	1.078	1.049	
	Voutn_dc_LV_HT	100	1.022	info	1.076	1.047	
	Voutn_dc_LV_LT	100	1.023	info	1.077	1.047	
-	⚙ Voutp_dc(summary)	100	105.4m		167m	136.3m	
	Voutp_dc	100	106.2m	info	159.1m	133.1m	
	Voutp_dc_HV_HT	100	105.4m	info	159m	132.7m	
	Voutp_dc_HV_LT	100	119.7m	info	167m	142.9m	
	Voutp_dc_LV_HT	100	111.4m	info	162.9m	137.4m	
	Voutp_dc_LV_LT	100	109.1m	info	160.7m	135.1m	

- **The effect of the bandgap reference variation due to process variation needs to be translated to impact in gain/pulse width.**
- **Simulation of individual blocks and the full system must be presented in more detail**

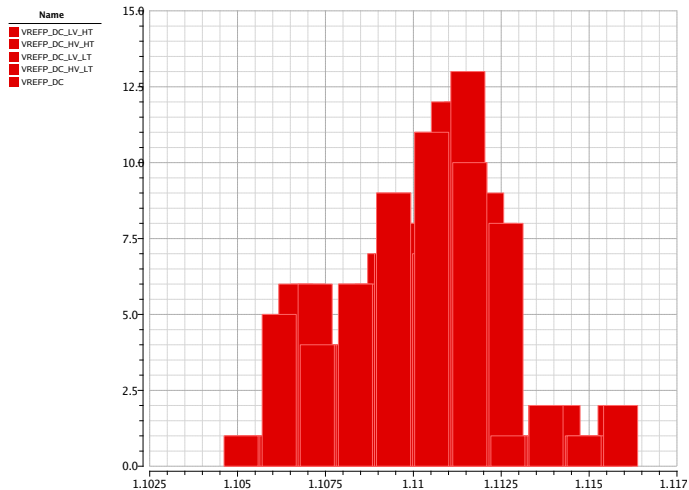
# Bandgap voltage variation in the system simulation

**view:** extracted **Model:** MC **Temp:**LT,HT **VDD:**LV,HV



# VREFP variation in the system simulation

**view:** extracted **Model:** MC **Temp:**LT,HT **VDD:**LV,HV



# Frontend sim: FE + Bias + Bandgap (-)

## 160ns@20mV/fC

**view:** extracted **Model:** MC **Temp:**LT,HT **VDD:**LV,HV

Test	Name	Yield	Min	Target	Max	Mean	Sigma to Target	Sigma
Parameters: Yield Estimate: 100 %(50 passed/50 pts) Confidence Level: <not set>								
-	⚙ sampa_csa_shaper:sim_csa_shaper:1							
-	⚙ Amp(summary)	100	992.4m		1.022	1.008		2.737m
-	⚙ ENC(summary)	100	366.8		435.3	404.3		4.025
-	⚙ In_charge(summary)	100	47.54f		47.66f	47.6f		8.371a
-	⚙ Peaking time(summary)	100	143n		168n	154.9n		2.353n
-	⚙ Sensitivity(summary)	100	20.84		21.49	21.18		57.69m
-	⚙ Vout_max(summary)	100	-52.13m		63.55m	12.07m		21.37m
-	⚙ Vout_min(summary)	100	-1.05		-948m	-996.1m		19.84m
-	⚙ onoise(summary)	100	1.243m		1.465m	1.372m		16.17u

# Frontend sim: FE + Bias + Bandgap (+)

## 300ns@4mV/fC

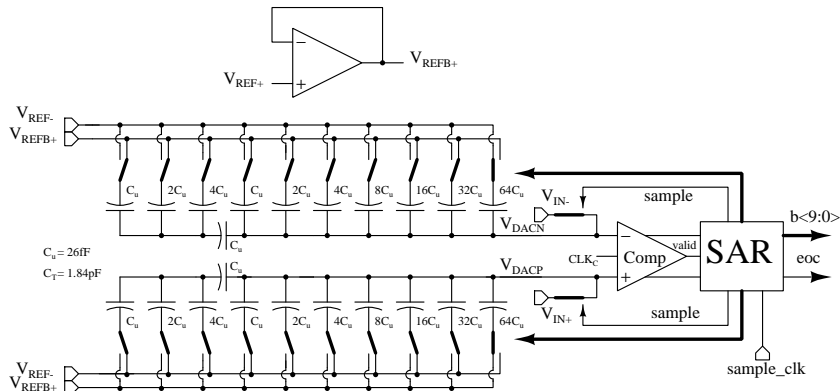
**view:** extracted **Model:** MC **Temp:**LT,HT **VDD:**LV,HV

Test	Name	Yield	Min	Target	Max	Mean	Sigma to Target	Sigma
Parameters: Yield Estimate: 100 %(50 passed/50 pts) Confidence Level: <not set>								
-	⚙ sampa_csa_shaper:sim_csa_shaper:1							
-	⚙ Amp(summary)	100	992.4m		1.022	1.008		2.737m
-	⚙ ENC(summary)	100	366.8		435.3	404.3		4.025
-	⚙ In_charge(summary)	100	47.54f		47.66f	47.6f		8.371a
-	⚙ Peaking time(summary)	100	143n		168n	154.9n		2.353n
-	⚙ Sensitivity(summary)	100	20.84		21.49	21.18		57.69m
-	⚙ Vout_max(summary)	100	-52.13m		63.55m	12.07m		21.37m
-	⚙ Vout_min(summary)	100	-1.05		-948m	-996.1m		19.84m
-	⚙ onoise(summary)	100	1.243m		1.465m	1.372m		16.17u

- **ADC performance must be studied in post-layout simulations (9.2 bit come from schematic simulations)**
- **Input capacitance to ADC is very high (20 pF), thus the buffer needs to be strong and the consumption is higher. In comparable design 2 pF can be achieved.**

# MPW2: New ADC capacitor array

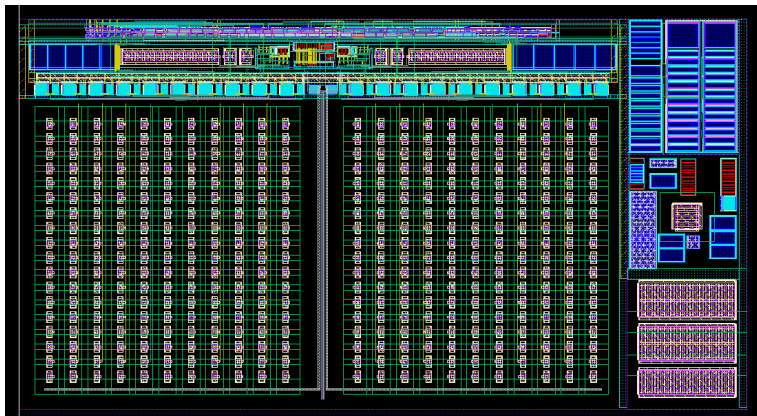
## Split Capacitor Array



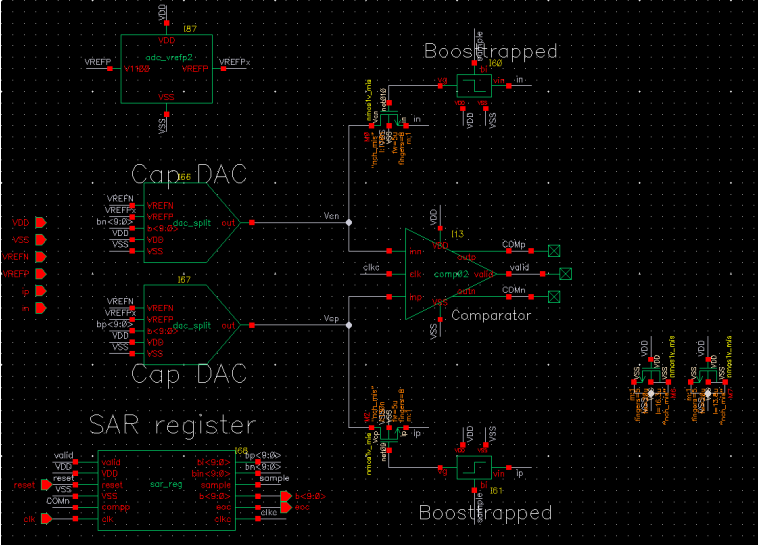


# MPW2: New ADC capacitor array (Layout)

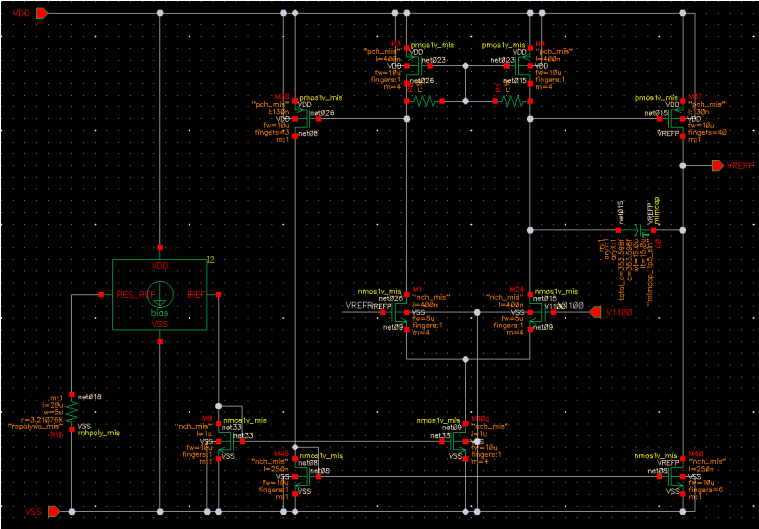
## Split Capacitor Array



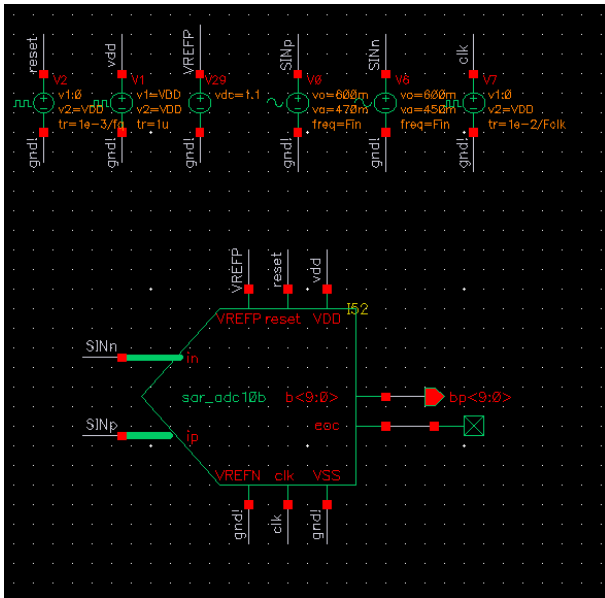
# MPW2: ADC schematic



# MPW2: Volatge reference Buffer



# MPW2: ADC simulation testbench



# MPW2: ADC simulations

View: extracted

Model: Corners: typ-ff-ss

Temp: 0C-50C

VDD: 1.1875V

OBS:  $N_s=64$   $F_s=20\text{Msps}$   $V_{REFP}=1.1\text{V}$   $V_{REFN}=0\text{V}$

temperature 27

	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	L
:1	ENOB	9.745				9.723	9.942	
:1	SFDR	68.25				66.63	70.13	

# MPW2: ADC simulations

View: extracted

Model: Corners: typ-ff-ss

Temp: 0C-50C

VDD: 1.325V

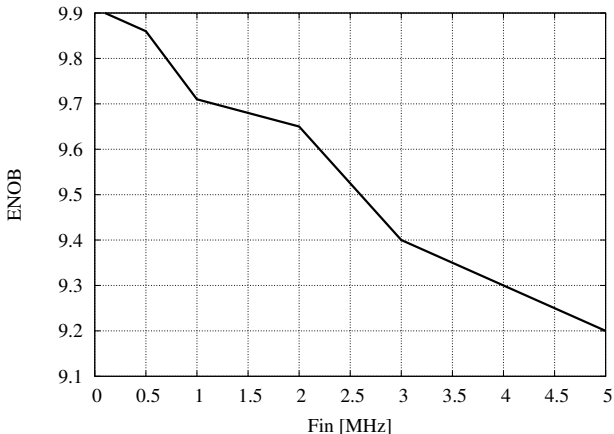
OBS:  $N_s=64$   $F_s=10\text{Msps}$   $V_{REFP}=1.1\text{V}$   $V_{REFN}=0\text{V}$

temperature 27

	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	L
:1	ENOB	9.745				9.723	9.942	
:1	SFDR	68.25				66.63	70.13	

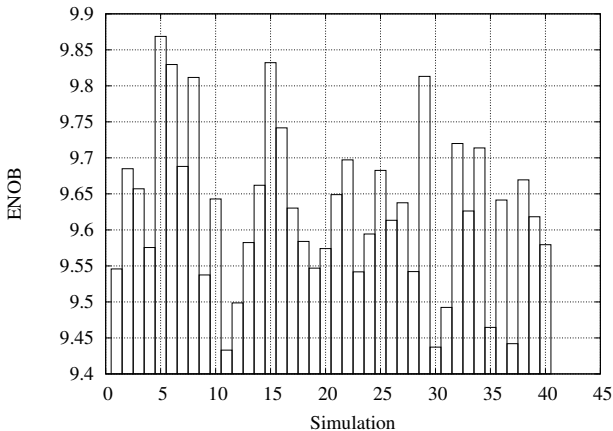
# MPW2:ENOB vs Fin

$N=256$ ,  $F_s=10\text{MHz}$ ,  $V_{DD}=1.25\text{V}$ ,  $V_{REFP}=1.1\text{V}$ ,  $\text{model}=\text{typ}$



# MPW2:ENOB $F_{in}=2e6$

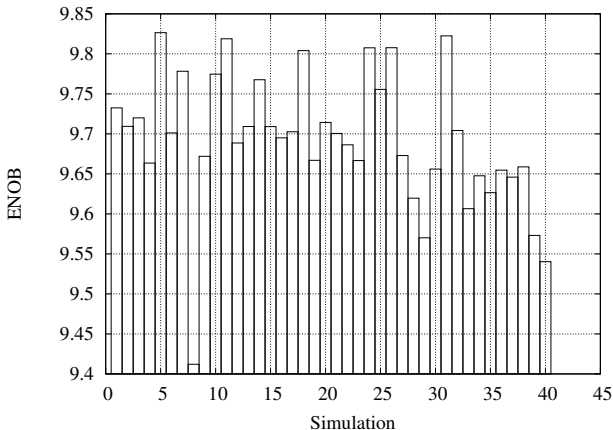
$N=256$ ,  $F_s=10\text{MHz}$ ,  $V_{DD}=1.25\text{V}$ ,  $V_{REFP}=1.1\text{V}$ ,  $\text{model}=\text{MC}$



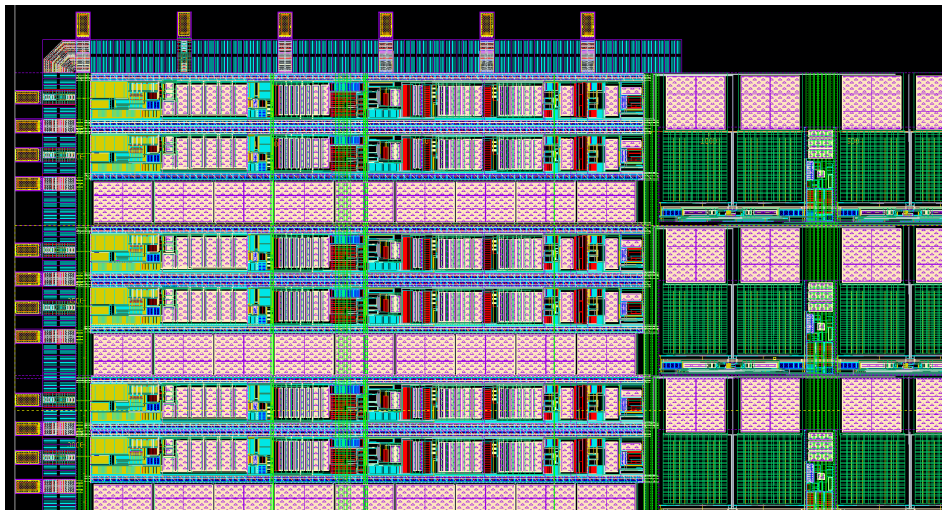


# MPW2:ENOB $F_{in}=1e6$

$N=256$ ,  $F_s=10\text{MHz}$ ,  $V_{DD}=1.25\text{V}$ ,  $V_{REFP}=1.1\text{V}$ ,  $\text{model}=\text{MC}$



# MPW2 Status: layout



# MPW2 Status

- Layout of Frontend - ADC - Analog Block: ready
- Layout SLVDS driver (Rx and Tx) is being performed
- System post-layout simulations to calculate the decoupling capacitors from the noise requirements are being performed.
- More post-layout simulations including packages and board effects are being performed.

# SAMPA:Voltage Reference Design

Tiago Oliveira Weber

Electrical Engineering Department of the Polytechnic School,  
University of São Paulo, Brazil

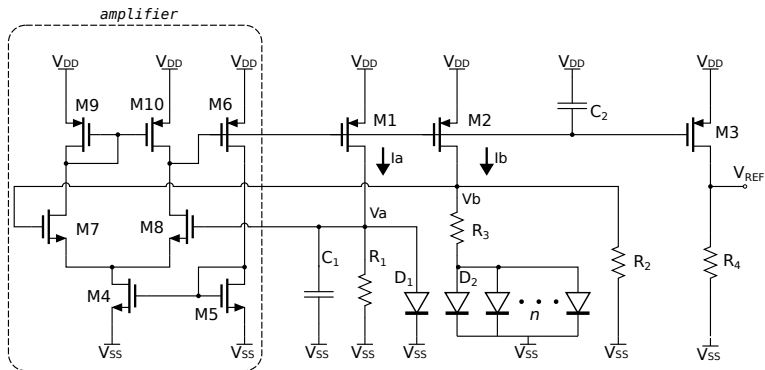
Institute of Physics, University of Sao Paulo, Brazil

April 1, 2015

# Voltage Reference Design

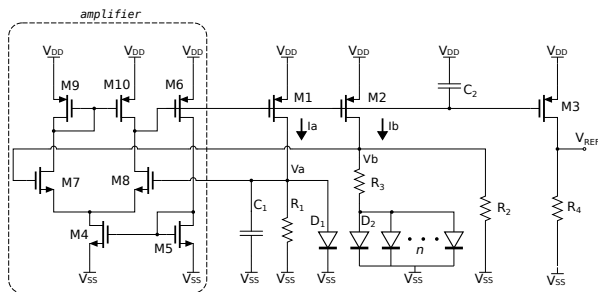
<b>Name</b>	<b>Target</b>
Output Voltage (mV)	600
Temperature Coefficient (ppm V/°C)	<30
Line Regulation (mV/V)	<10
Output Noise ( $\mu$ V)	<5
Power Supply Rejection Ration (dB)	>35

# Voltage Reference - Topology



[Banba et al., 1999]: Hironori Banba, Hitoshi Shiga, Akira Umezawa, Takeshi Miyaba, Toru Tanzawa, Shigeru Atsumi, and Koji Sakui, A CMOS bandgap reference circuit with sub-1-V operation JSSC, vol. 34, no. 5, may 1999

# Voltage Reference - Dimensions



Device	Dimensions ( $\mu\text{m}$ )
M1, M2, M3	53.5 / 6.63 (X5)
M4	2.33 / 0.92 (X2)
M5	2.33 / 0.92 (X3)
M6	53.5 / 6.63 (X2)
M7, M8	22.95 / 19.8 (X4)
M9, M10	30.8 / 7.43 (X10)
D1, D2	29.7 / 29.7
n	17
R1, R2	Resistance: 12.6 [k $\Omega$ ]
R3	Resistance: 1.7 [k $\Omega$ ]
R4	Resistance: 6.1 [k $\Omega$ ]
C1, C2	Capacitance: 4 [pF]

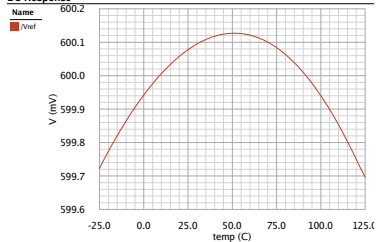
# Voltage Reference - Nominal Results

<b>Name</b>	<b>Simulation Results</b>
Output Voltage	600.097 mV
Temperature Coefficient	4.29 ppm V/°C
Line Regulation	629 $\mu$ V/V
Output Noise	844,6 nV
Power Supply Rejection Ration	64 dB
Power Comsumption	432.7 $\mu$ W

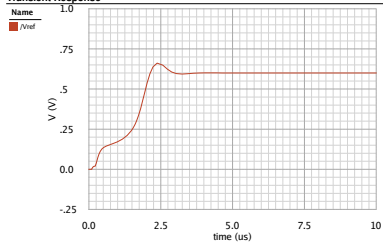


# Voltage Reference - Output Waveforms

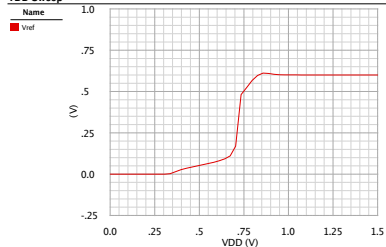
### DC Response



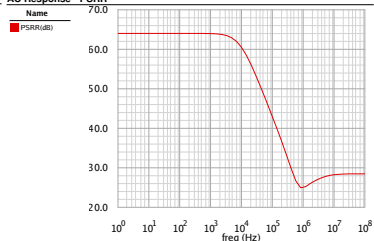
### Transient Response



### VDD Sweep

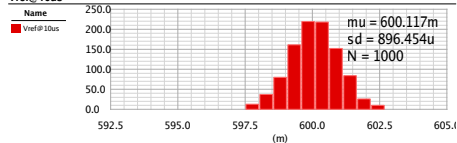


### AC Response - PSRR

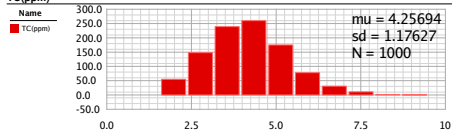


# Voltage Reference - Montecarlo

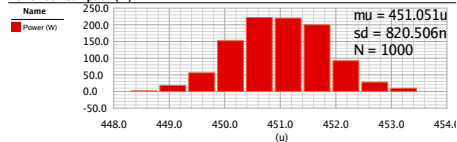
Vref@10us



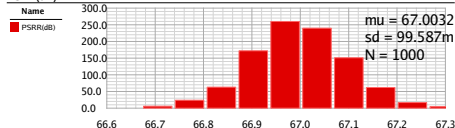
TC(ppm)



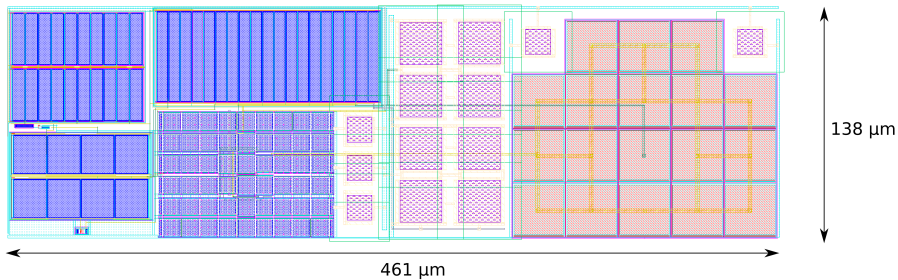
Power Consumption (W)



PSRR(dB)



# Voltage Reference - Layout



# Voltage Reference - Layout (regions)

