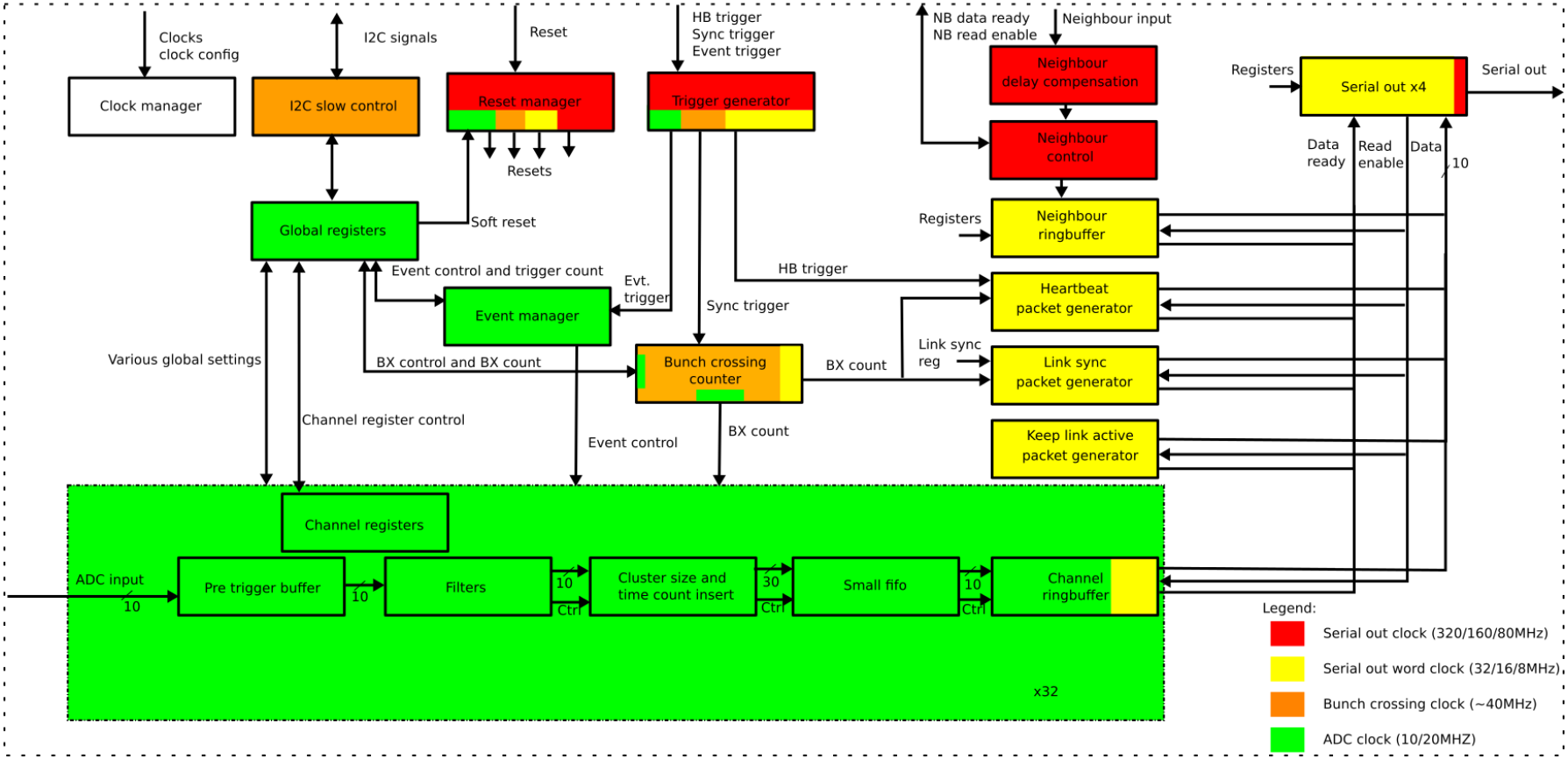
SAMPA MPW2
digital design review 2

Clock domains

- Clock domains and manager must be explained in more detail and be verified in dedicated full ASIC system simulations. It is suggested to show the clock domains in a dedicated block diagram.

- Clock manager simulated for 100% coverage
- Simulated on gate level with timing and no significant added jitter is seen

SAMPA MPW2 block diagram



Clock domain delay

- Delay of specific clocks with respect to other clocks in order to reduce noise impact need to be studied and presented.

- Postponed until layout is done

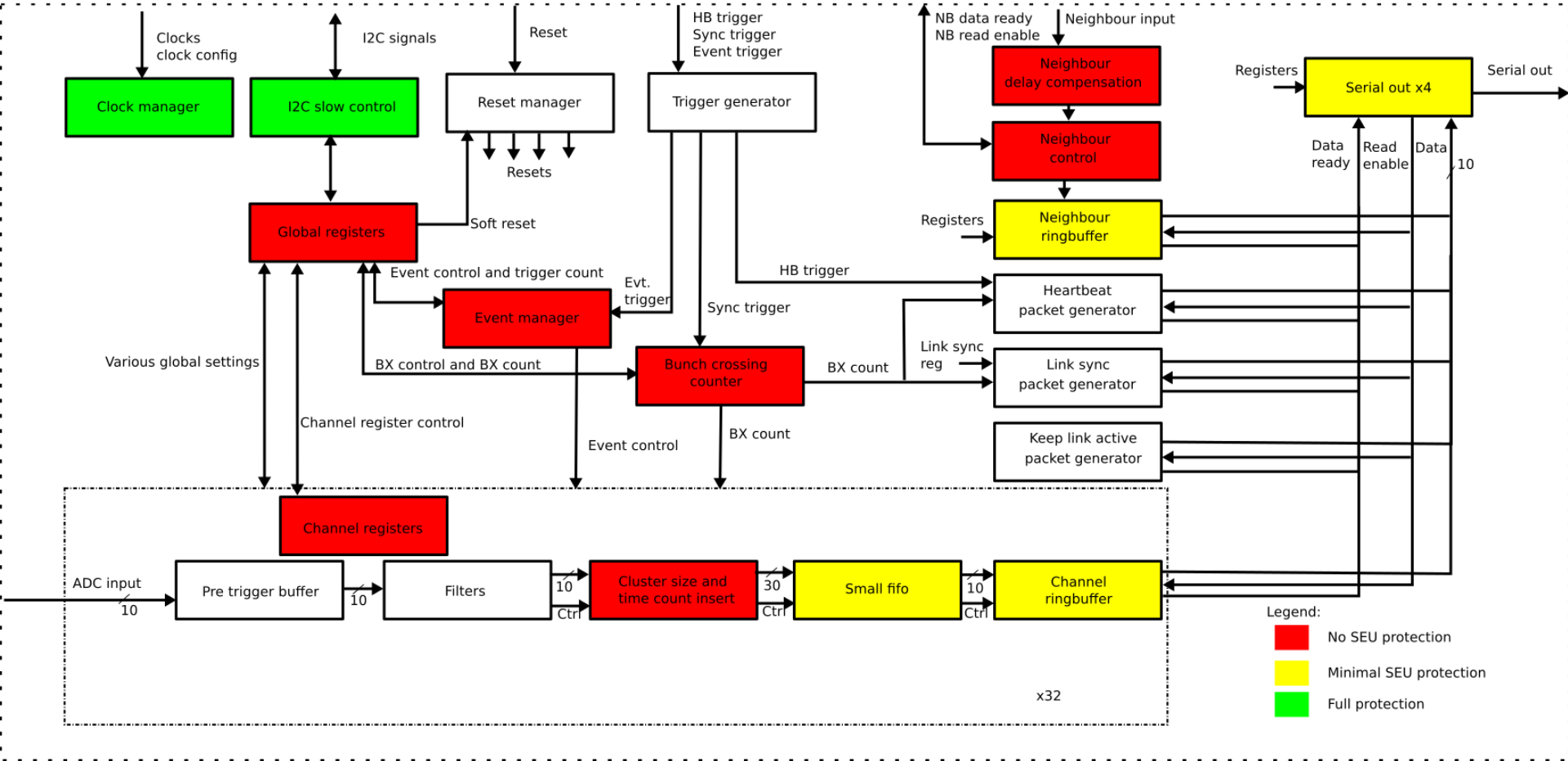
SLVS

- SLVS receiver can activate a 100 Ohm termination by programing. This should not be done for clock and reset.

- Implemented in analog driver, not yet in digital

SEU protection status

- Describe which parts are SEU protected.

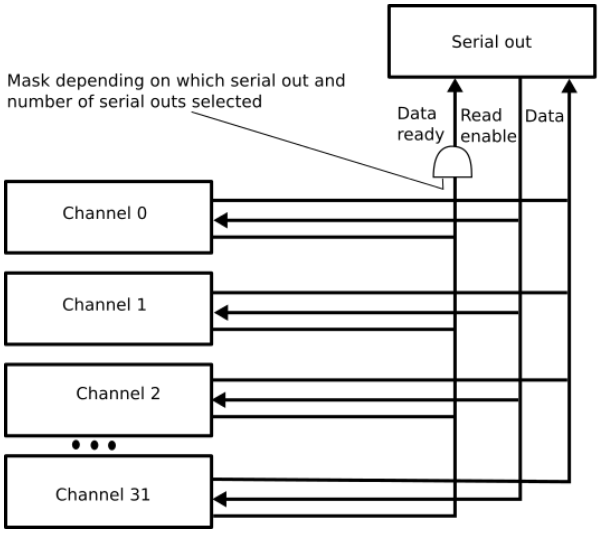


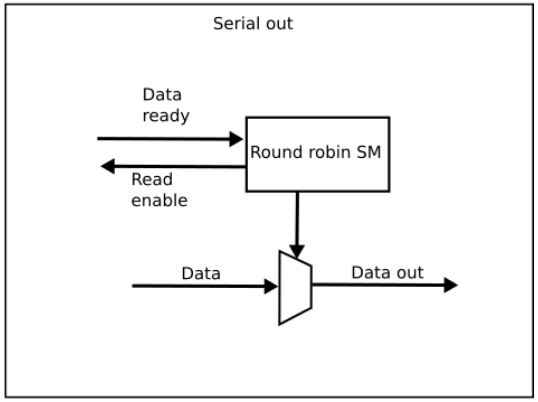
Current SEU protection

- Clock manager: TMR on word clock counter
- Ring buffer:
  - TMR on payload size stored in header
  - TMR on memory pointers
- Serial out: TMR on bit counter
- Fifo : TMR on memory pointers

TPC channel organization

- Old solution connects all channels and control signals to each serial out, but uses a mask on the data ready signal to select which channels are available for each serial out
- Serial out reads from each channel depending on data ready status in a round robin fashion from low channel number to high





TPC channel organization

- New solution will instead of doing the round robin list from low to high use a programmable list to decide the order
- The position in the list determines which channel is connected to which serial out
  - Ie for 4 serial outs, the first 8 positions are used by serial out 0