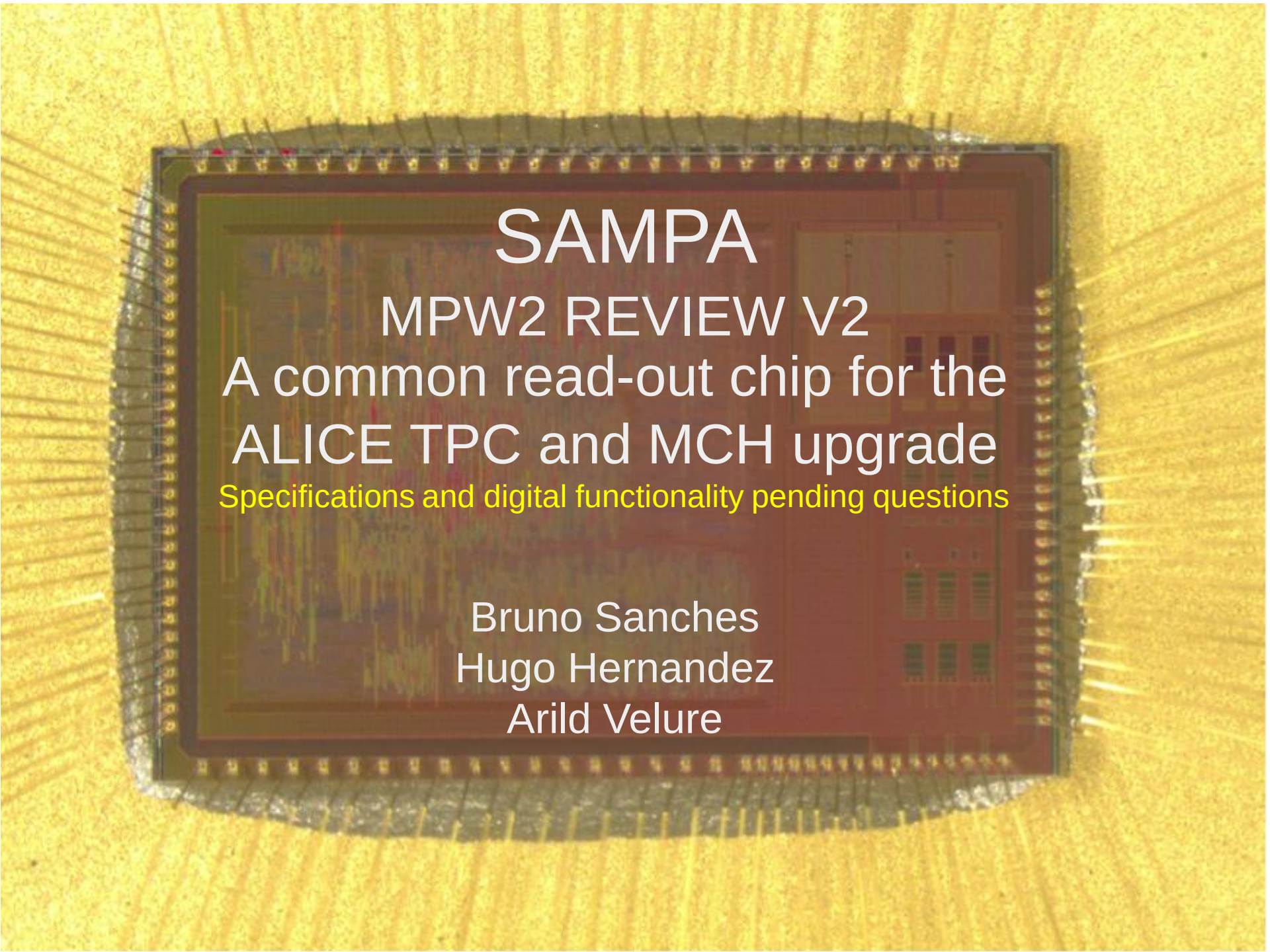

SAMPA

MPW2 REVIEW V2

A common read-out chip for the ALICE TPC and MCH upgrade

Specifications and digital functionality pending questions

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Specifications

Technology: **0.13 µm** TSMC (7 Metal Layers [last is UTM])
Channels: **32 DSP + 1 Neighbour (daisy chained)**
Data output: 4 serial outputs (SLVS 1,2V)
Data input: 1 serial output (**Neighbor**)
Trigger: **continuous** mode + **one** external SLVS trigger signal
Device Configuration:

- **I2C** (1,2 V interface)
  - For Internal Registers / Pedestal Memory R/W
- Hard wired configuration pins
  - Chip address
  - Clock selectors
  - Analog operational mode
  - SLVS Driver strength

MPW2 – SRAM Buffers

- Final Choice over the SAMPA internal Buffers/SRAMs:

- Pedestal Memory:
  - 1024 Word SRAM, one per Channel

- Trigger Delay
  - 192 Word SRAM, one per Channel

- DATA Memory
  - 6K (6*1024) Word SRAM / Channel

- Header Delay
  - 256 Word SRAM / Channel

- Neighbor Memory
  - 4096 Word SRAM for DATA + 256 Word SRAM for Headers

* Simulations?

Filters

SAMPA will have as filter datapath:

BC1:

Baseline correction 1, no big changes from last presentation

DS:

Tail cancelation, nothing changed

BC3

Baseline correction 3, Slope based filter, Now can have slopes greater than 1

BC2

Baseline Correction 2, similar than in the other presentation, Now with autoreset, and can be connected to load the reset baseline from REG, BC3, or BC2 without thresholds

ZSU

Zero Supression, Now Clipping and offset are centralized just here.

SAMPA has By Pass for each filter

So, there are several possibilities of filter datapath...

* Simulations?

SLVS

- SLVS Driver configurations:

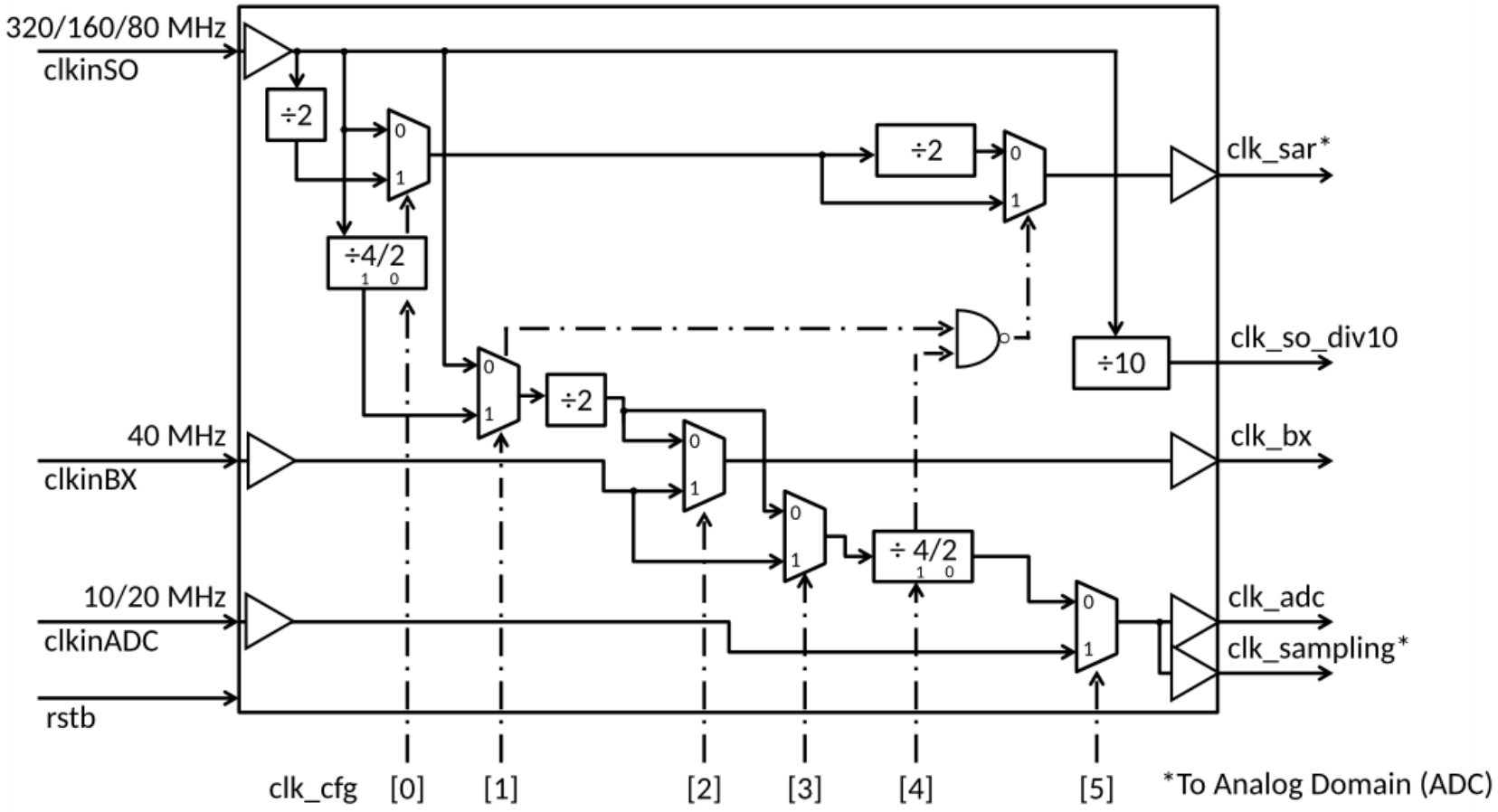
- Drive current/strength:
  - 1 External Global pin per chip

- Termination:
  - 1 internal register(bit) per chip, that works over all SLVS pins, except for clock and reset to choose the termination (100 ohm resistor).

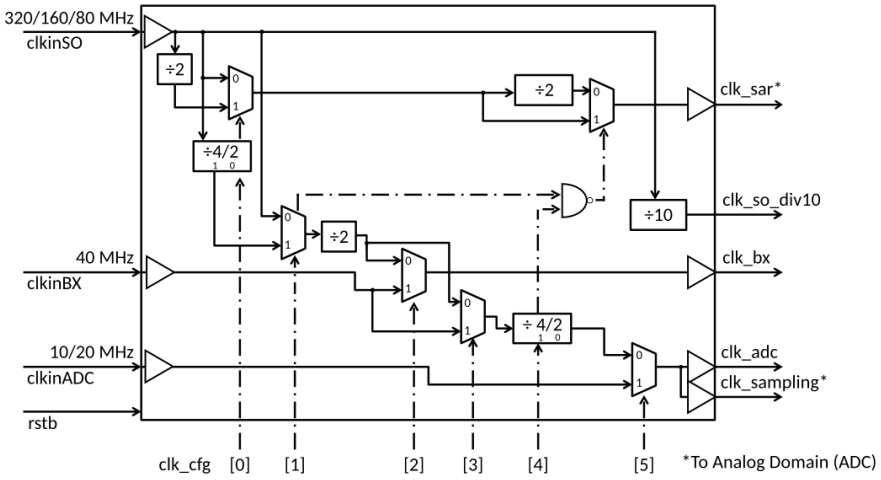
- Stand By
  - Depending on the mode, the digital block will set 0, 1, 2 or 3 SLVS drivers to be on stand by to save power...

Clock Manager

- Configurable by 6 input pins



Clock Manager



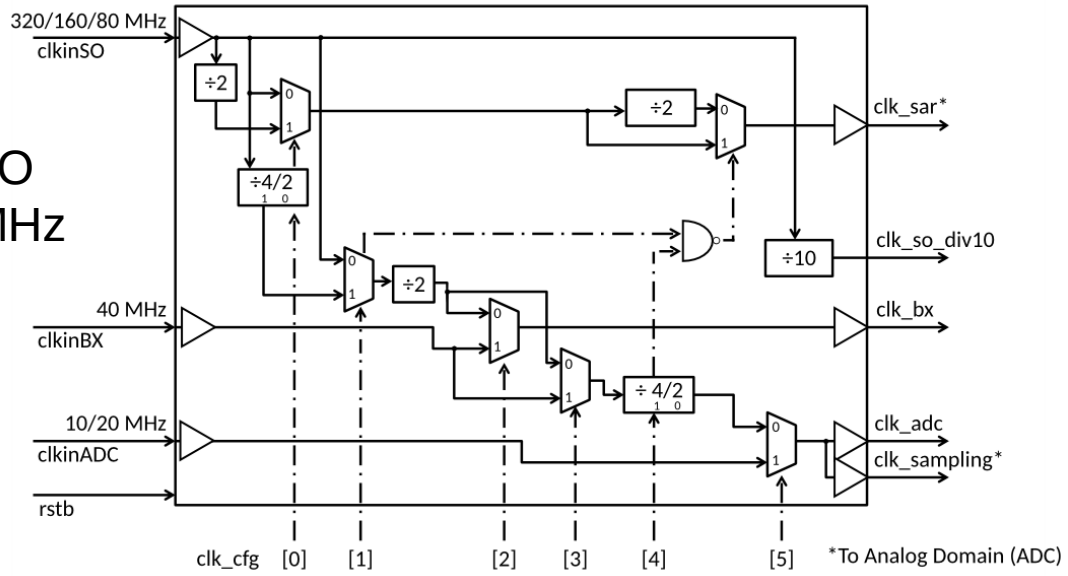
- Inputs:
  - clkinSO
    - MANDATORY SLVS Input:
      - 320 MHz, 160 MHz or 80 MHz
  - clkinBX
    - OPTIONAL SLVS Input
      - 40 MHz
  - clkinADC
    - OPTIONAL SLVS Input:
      - 20 MHz or 10 MHz

- SAMPA CAN run just with the clkinSO...

Clock Manager

- Internaly generated Outputs

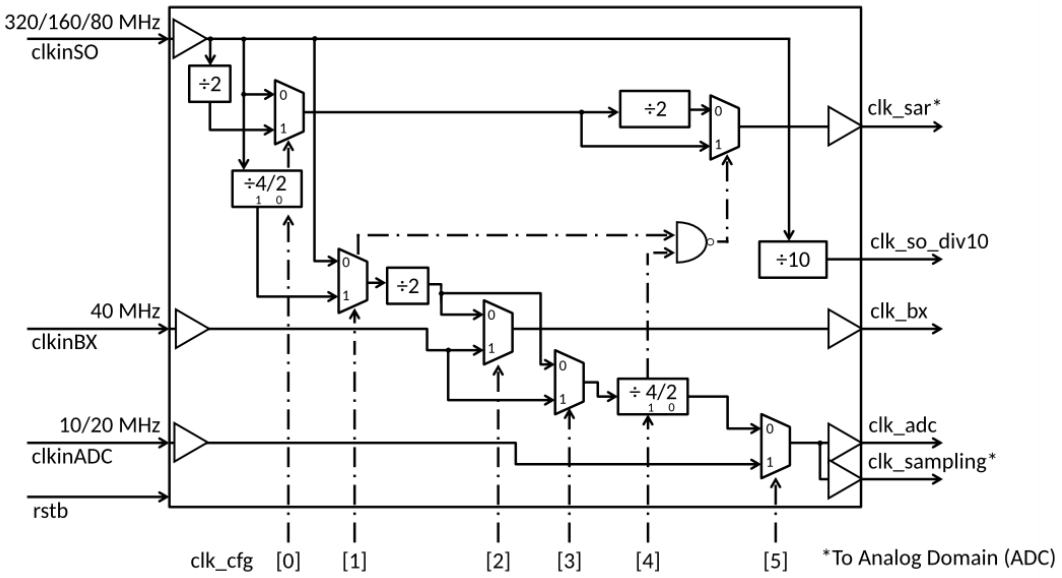
- To DIGITAL DOMAIN:
  - clk_so_div10
    - Division by 10 of clkinSO
    - 32 MHz, 16 MHz or 8 MHz
  - clk_BX
    - 40 MHz
  - Clk_adcDC
    - 20 MHz or 10 MHz



Clock Manager

- Internaly generated Outputs

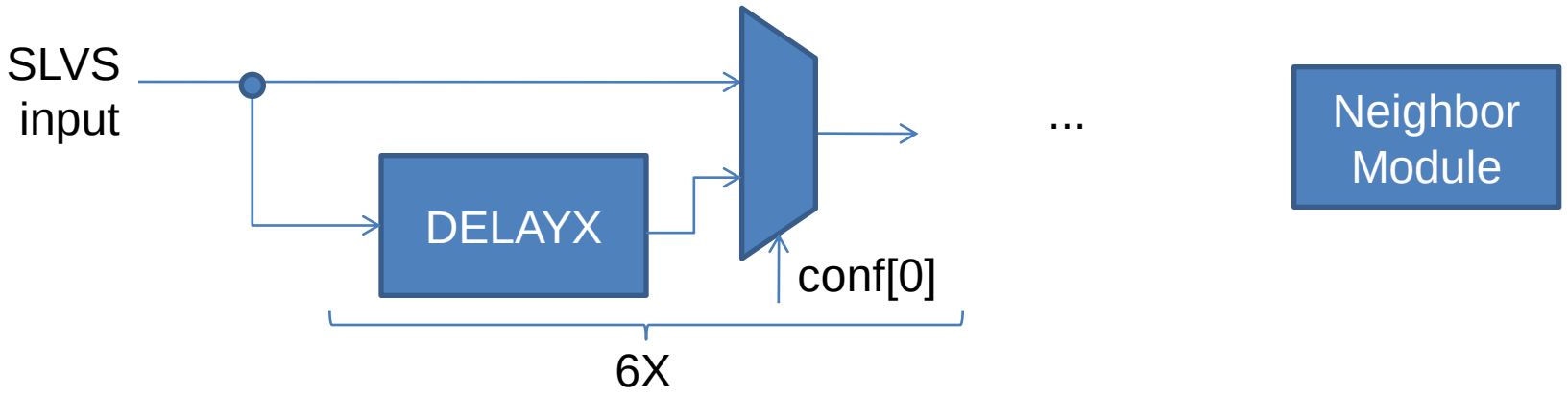
- To ANALOG DOMAIN:
  - clk_sampling
    - 20MHz or 10MHz
    - Delayed
      - From clk_adc
      - by 0.5 ns
  - clk_sar
    - 160 MHz or 80 MHz
    - Dependent on clk_adc choice
      - When running at clk_adc = 10 MHz
        - Clk_sar will be 80 MHz
      - When running at clk_adc = 20 MHz
        - Clk_sar will be 160 MHz
        - Available when clkinSO = 160MHz or 320 MHz
        - **Proibited** in clkinSO = 80MHz case (**MCH**?)



Neighbor Input- Delay Line

- SAMPA will have one input for neighbor connection
  - This input does not have clk recovery or nothing like that
  - A syncronous ckinSO is mandatory and assummed between SAMPA chips

- Sampa Neighbor input block will have a configurable (I2C) Delay line
  - Made of Delay cells of tsmc in the digital flow
  - To adjust and match fixed delays from
    - PCB
    - IO drivers / PADS
- With 6 Bit configurable inputs, with total delay from ~0ns to 12.5ns



SBE Protection

- SAMPA FSMs will be SBE (Single Bit Error) protected
  - Using hamming codes for single bit error correction

- The Number of bits necessary for the functionality is complemented with the hamming bits
  - New generated states are completed and linked with the original expented funcionality

  - Invalid States makes the FSM return to the reset state, as probably are from double (or more) bit errors... (not expected to happes often)

- The configuration registers on SAMPA will receive SBE protection
  - Two options here, depending on the case
    - TMR (We have a standard cell for votting that makes it more efficient)
    - Extra bits, with Hamming decoding, and then, send the config data to the individual modules being configured
      - Sampa already received the config data hamming encoded...

Thanks