MFT: WG6 Readout activities

LPC Clermont-Ferrand– 1st april 2015

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Outline

I. Reminder on the MFT

II. On-detector studies (Front-end Boards and integration)

    1. Ladders (FlexPrintedCircuit)

    2. Disks

    3. Power supply unit

    4. Motherboards

    5. Barrel patch panel

III. Off-detector studies (Readout Unit)

    1. Synoptic and numbers

    2. Readout Unit boards

IV. WG6 readout tasks

V. Human ressources and needs

VI. Discussions
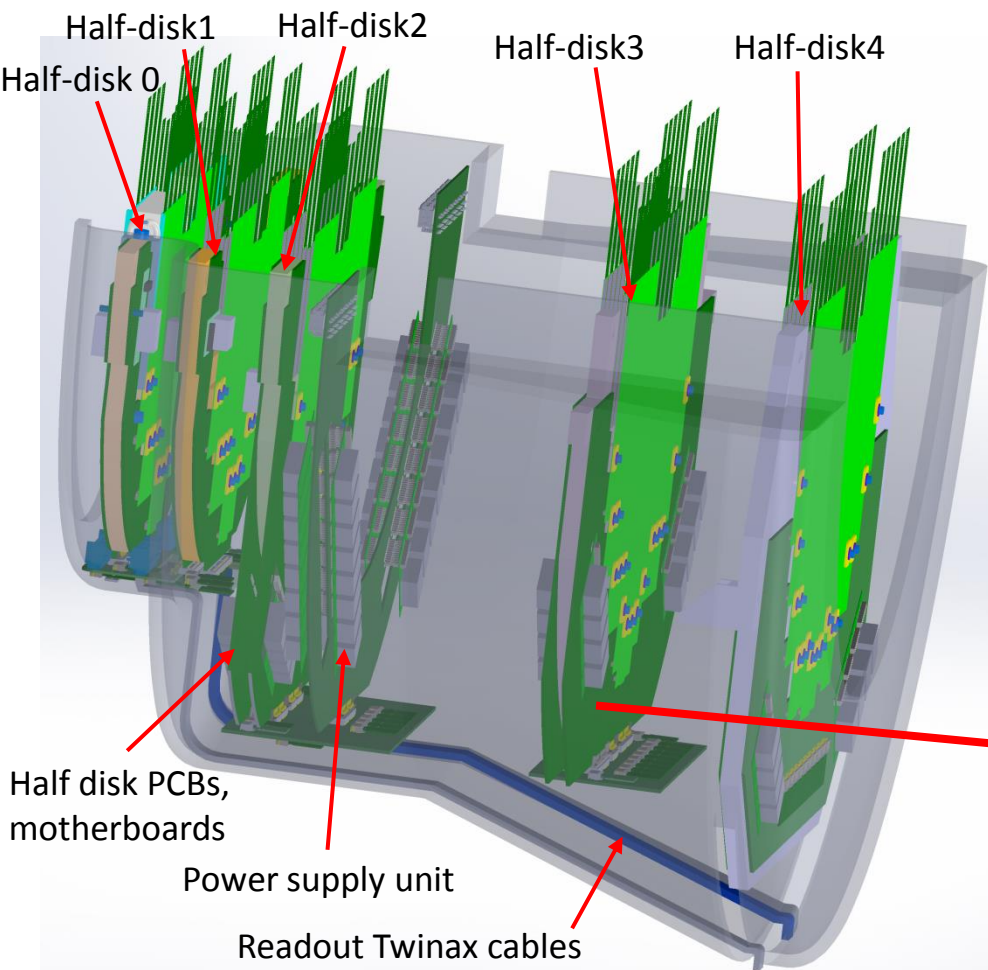
I. Reminder on the MFT
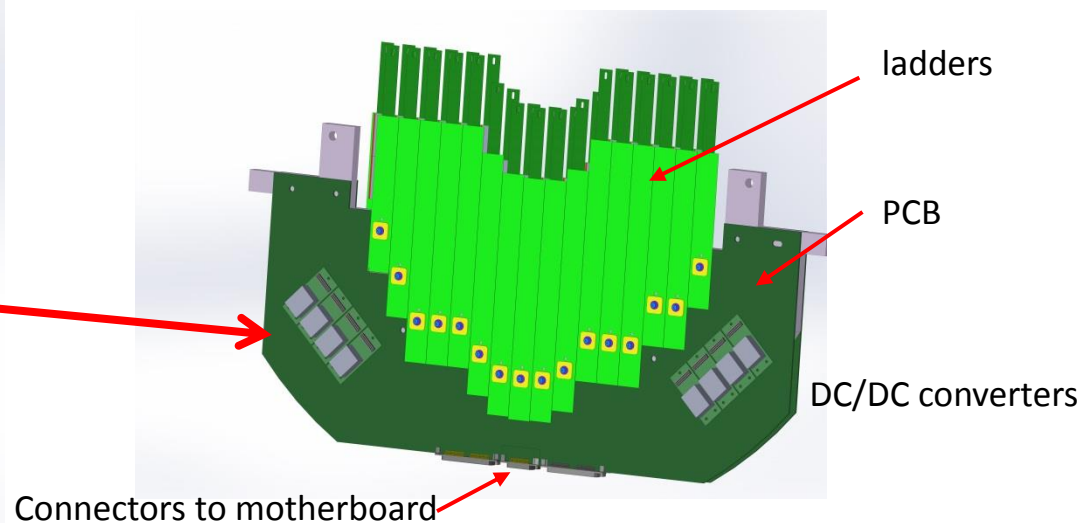
General layout of the MFT half-barrel and its environment
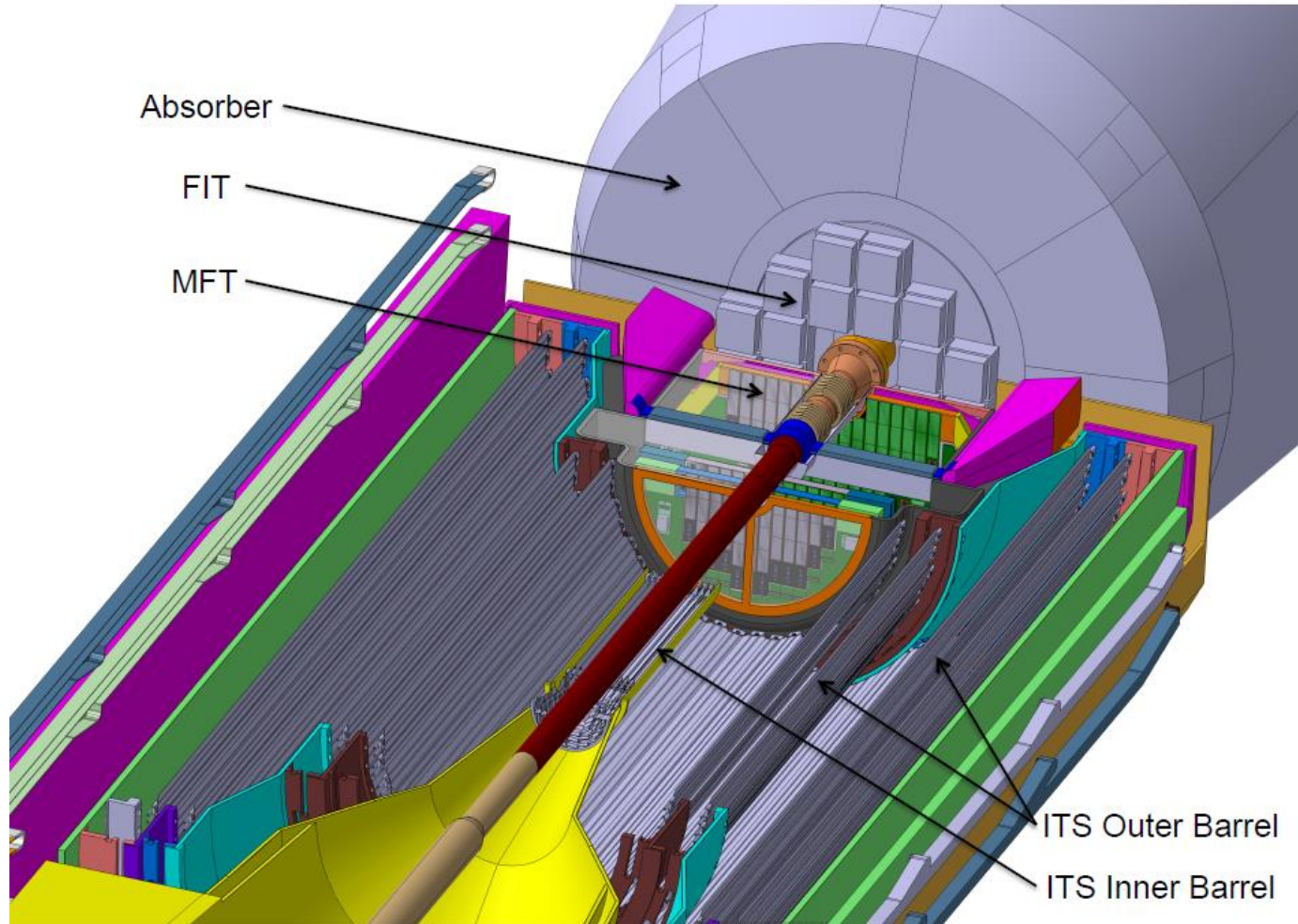
I. Reminder on the MFT

View of the MFT Half-Cone (bottom)

Half-disk1   Half-disk2
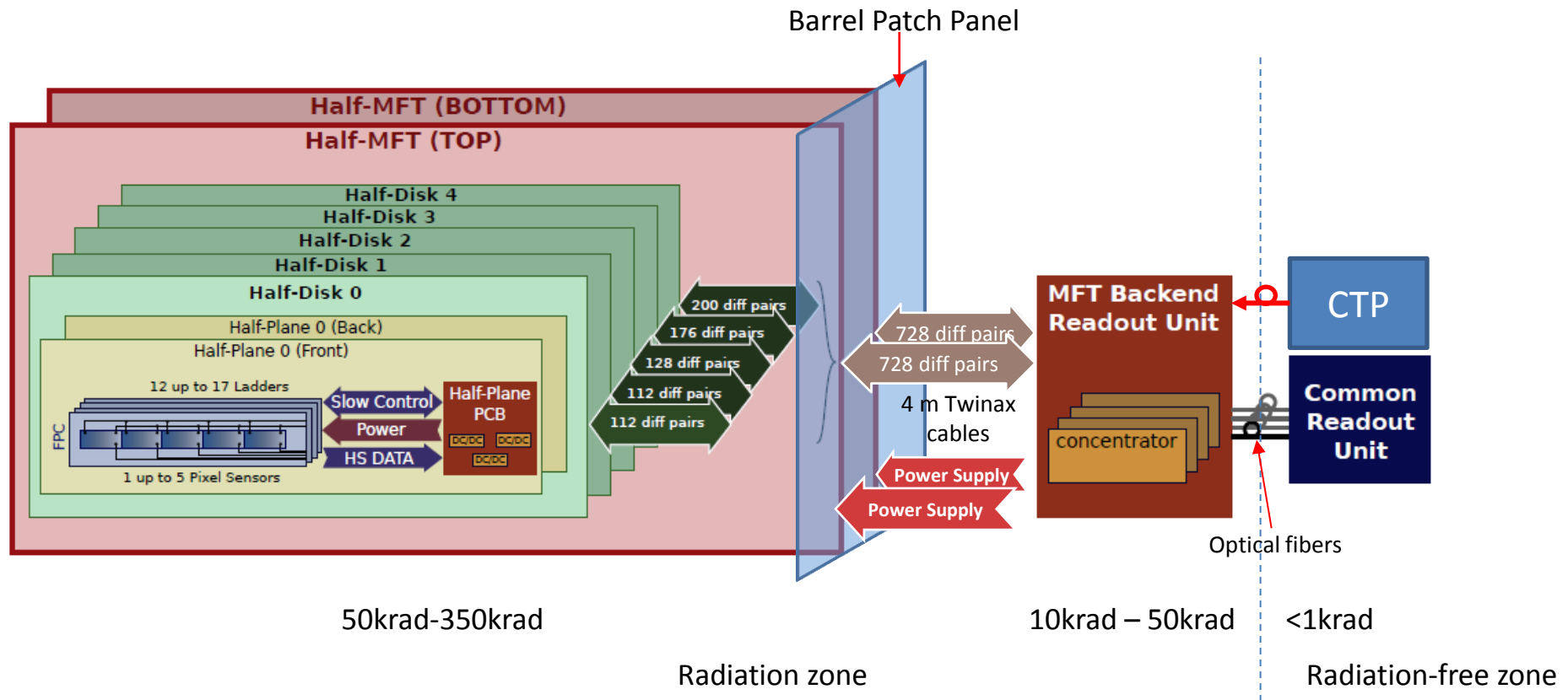
Half-disk 0

Half-disk3   Half-disk4

- 5 disks in the MFT cone
- Disks composed by a front and back detection system
- Sensor for detection is ALPIDE
- Total of 912 ALPIDE sensors for MFT

front view of the half disc3 (ladders + PCB)

ladders

PCB

DC/DC converters

Half disk PCBs, motherboards

Power supply unit

Readout Twinax cables

Connectors to motherboard

I.   Reminder on the MFT

General readout diagram of the MFT

Common ITS/MFT readout architecture (Inner Barrel + Twinax)

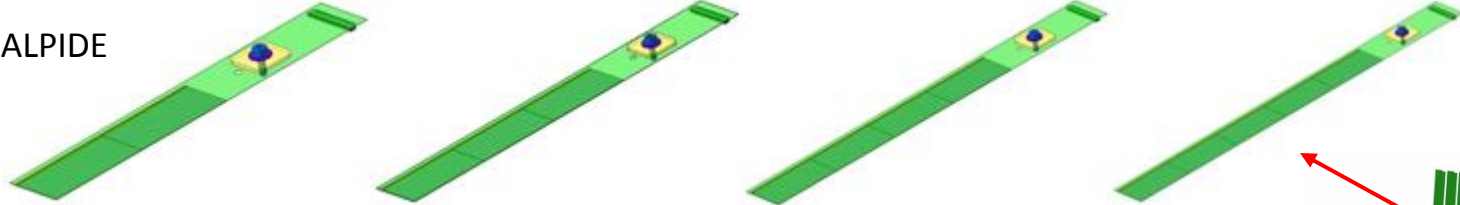50krad-350krad   10krad – 50krad   <1krad

Radiation zone   Radiation-free zone

II. On-detector studies

1. Ladders (FlexPrintedCircuit)

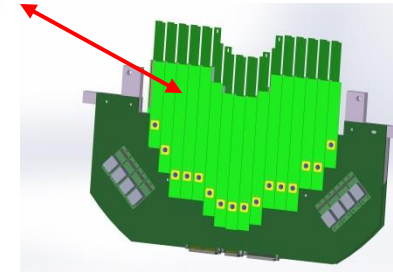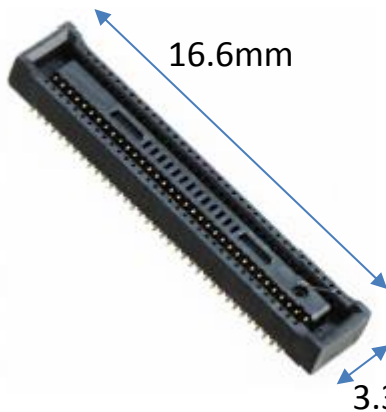**2 sensors**　　**3 sensors**　　**4 sensors**　　**5 sensors**
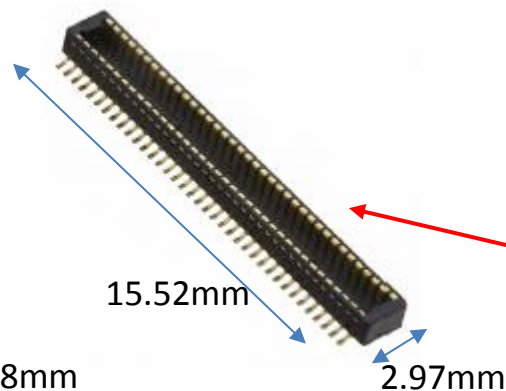
- Sensors on ladders : ALPIDE

4 sizes of ladders

PCB connector (70 contacts)
HIROSE DF40C-70DS-0.4V(51)

FPC connector (70 contacts)
HIROSE DF40C-70DP-0.4V(51)
0,4mm pitch

200 mm for 5 sensors

169,9 mm for 4 sensors

139,8 mm for 3 sensors

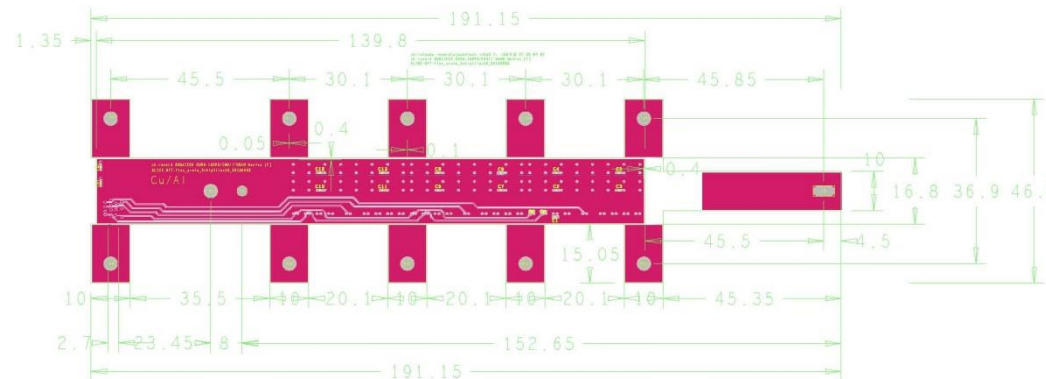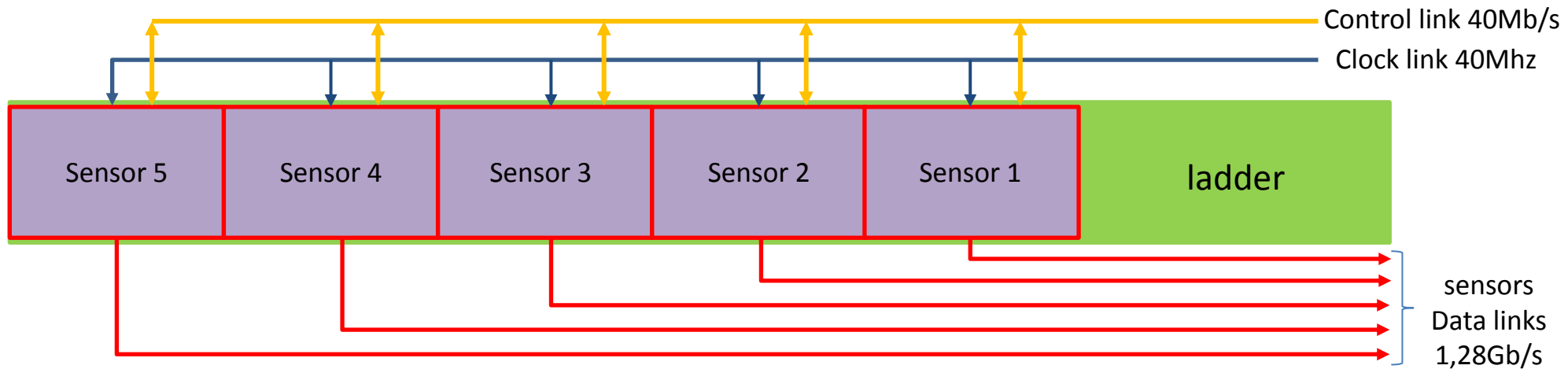109,7 mm for 2 sensors

16.6mm

15.52mm

connector

16,8 mm

3.38mm

2.97mm

MFT ladders dimensions

II. On-detector studies

1. Ladders (FlexPrintedCircuit)
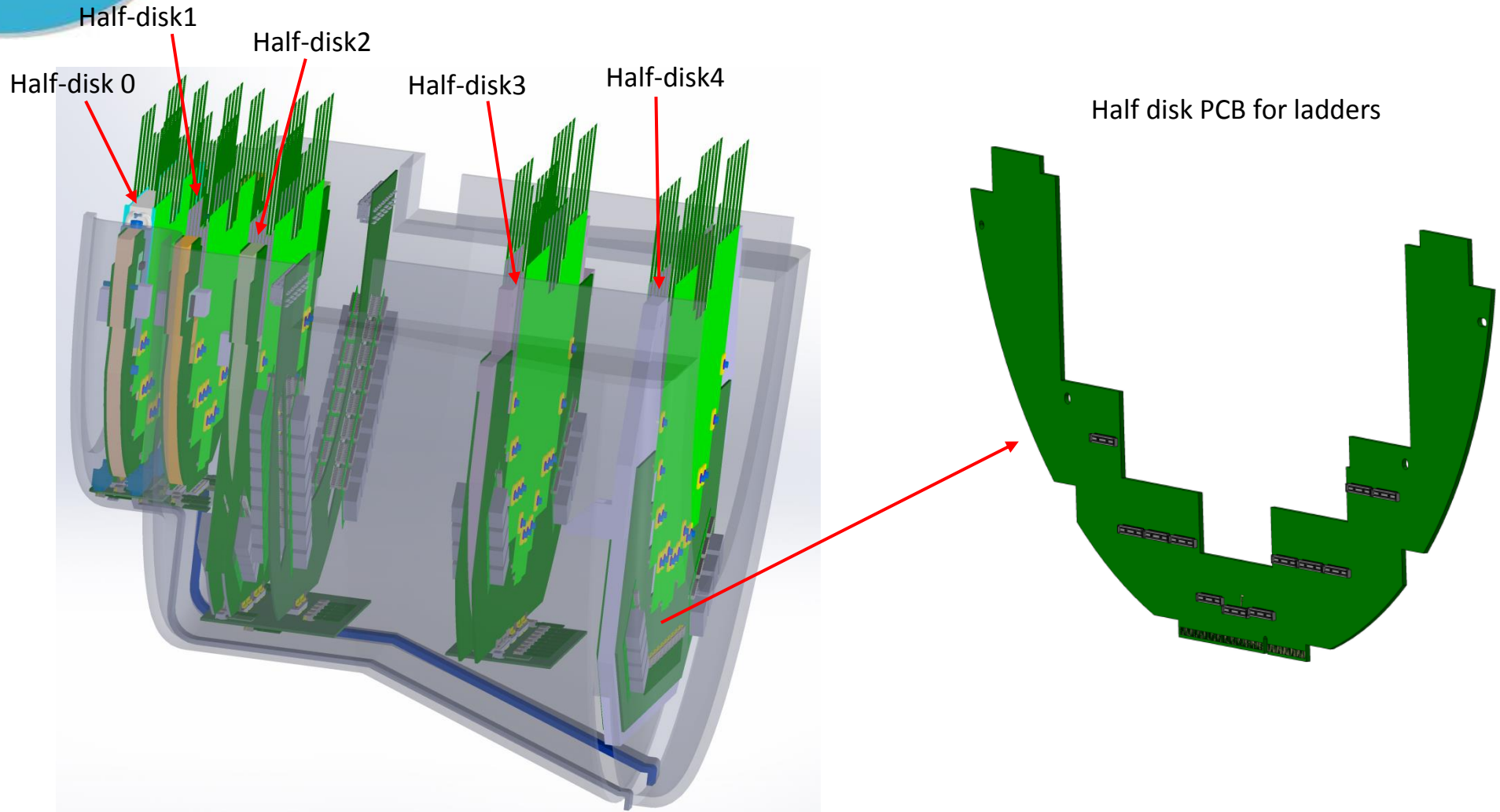
Data/Control connections on ladder

Control link 40Mb/s

Clock link 40Mhz

| Sensor 5 | Sensor 4 | Sensor 3 | Sensor 2 | Sensor 1 | ladder |

sensors
Data links
1,28Gb/s

II. On-detector studies

1. Ladders (FlexPrintedCircuit)

Signal names	Numbers	features
HSDATA	As many as sensors Up to 5	Point to point link High speed differential link (LVDS) 1.28Gb/s
DCLK	1 per ladder	Multi-drop link 40Mhz differential link (MLVDS)
DCTRL	1 per ladder	Multi-drop link 40Mb/s differential link (LVDS)
1.8V analog power	1 plan / ladder	20mA / sensor => up to 100mA / ladder
1.8V digital power	1 plan / ladder	105mA / sensor => up to 525mA /ladder
GND analog	1 plan / ladder	Connected with GND digital on the half disc ?
GND digital	1 plan / ladder	Connected with GND analog on the half disc ?
Back-bias (SUB)	1 plan / ladder	0V to -10V Must be confirmed
Back-bias (PWELL)	1 plan / ladder	0V to -10V Must be confirmed

II. On-detector studies

2. Disks

Half-disk 0

Half-disk1

Half-disk2

Half-disk3

Half-disk4

Half disk PCB for ladders

II. On-detector studies

2. Disks

Disk Power supply

View of front side Disk 0 (or Disk 1)

View of front side Disk 3 (same principle for Disk 4)

Connector for Power +1,8V

Connector for Power +12V

- Disk 1 same as Disk 0 without DC/DC converters
- Disk 2 bigger than Disk 1 but without DC/DC converters
⇒ Need Power from a Power supply Unit

- Disk 3 bigger than Disk 2 with DC/DC converters
- Disk 4 bigger than Disk 3 with DC/DC converters
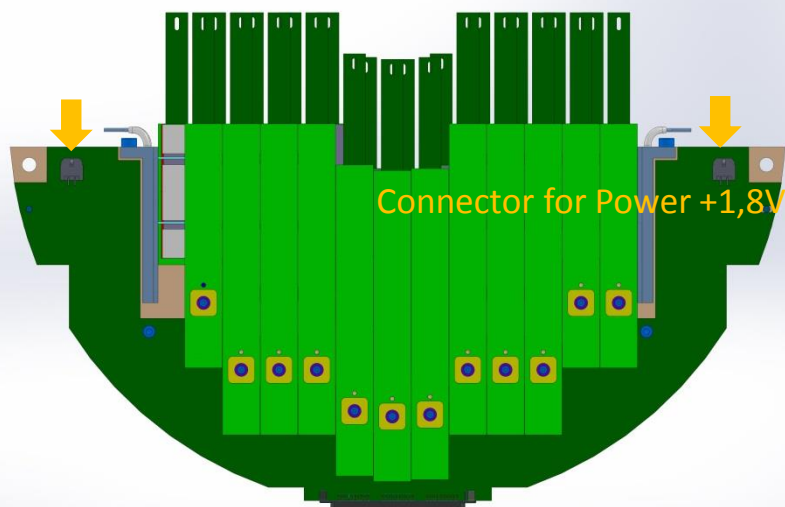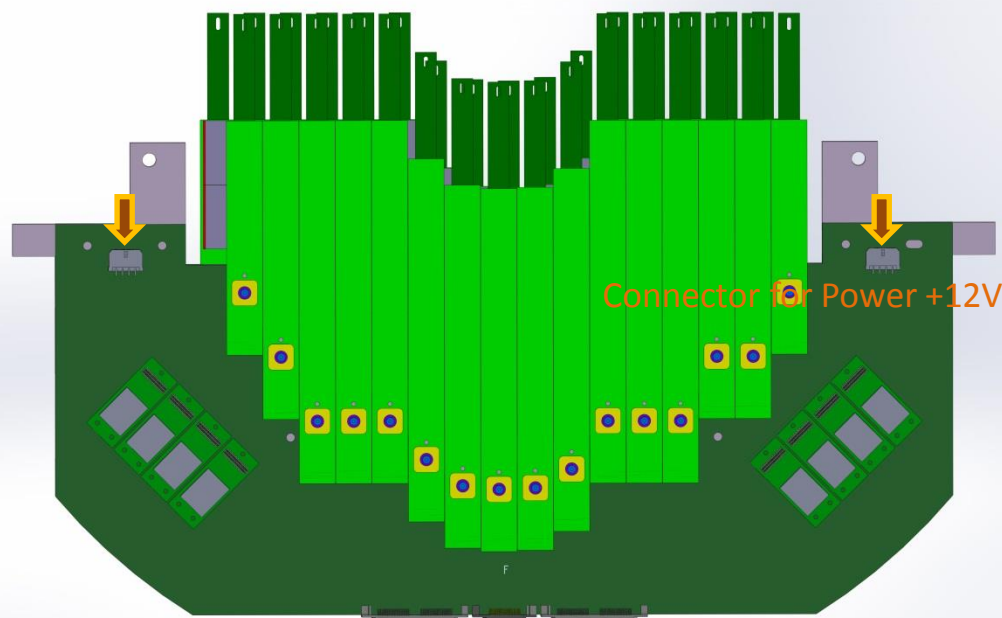⇒ Power supply directly from +12V

II. On-detector studies

2.   Disks

Disk Power supply

View of front side Disk 0 (or Disk 1)

View of front side Disk 3 (same principle for Disk 4)

Connector for Power +1,8V

Connector for Power +12V
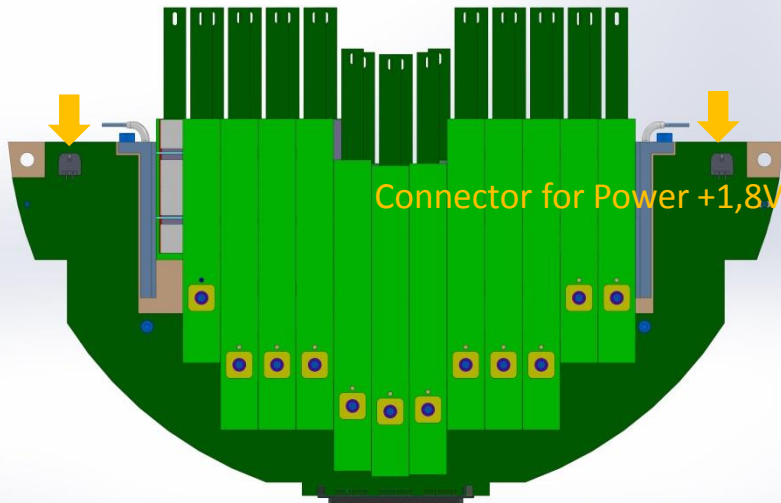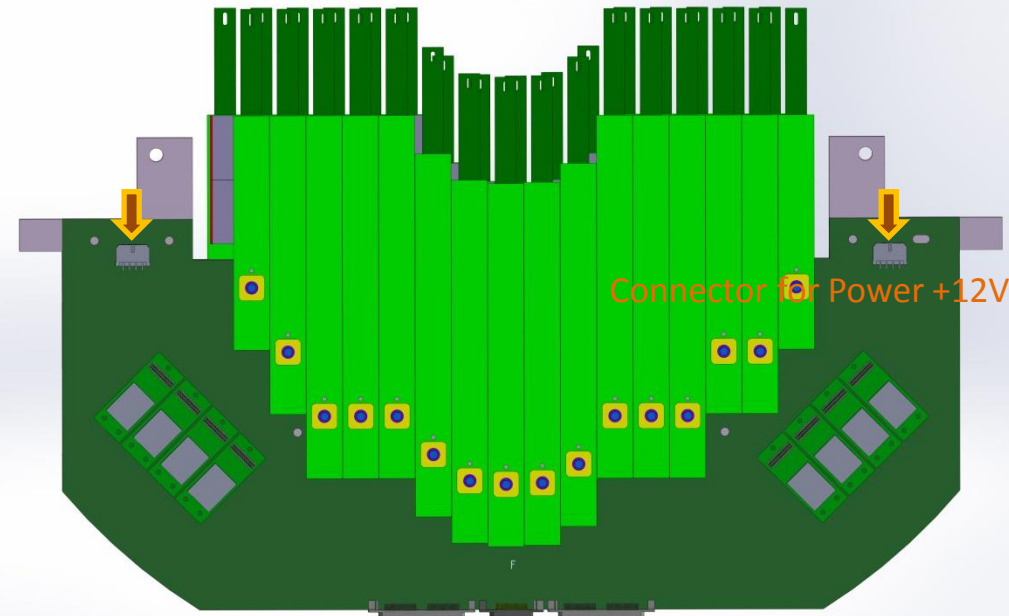
- Two DC/DC converters (analog and digital) needed for supply a quarter of a disk side

  ⇒ 8 DC/DC converters for one side of a disk

II.   On-detector studies

2.   Disks

Disk Signals connection

View of Half-disc PCB
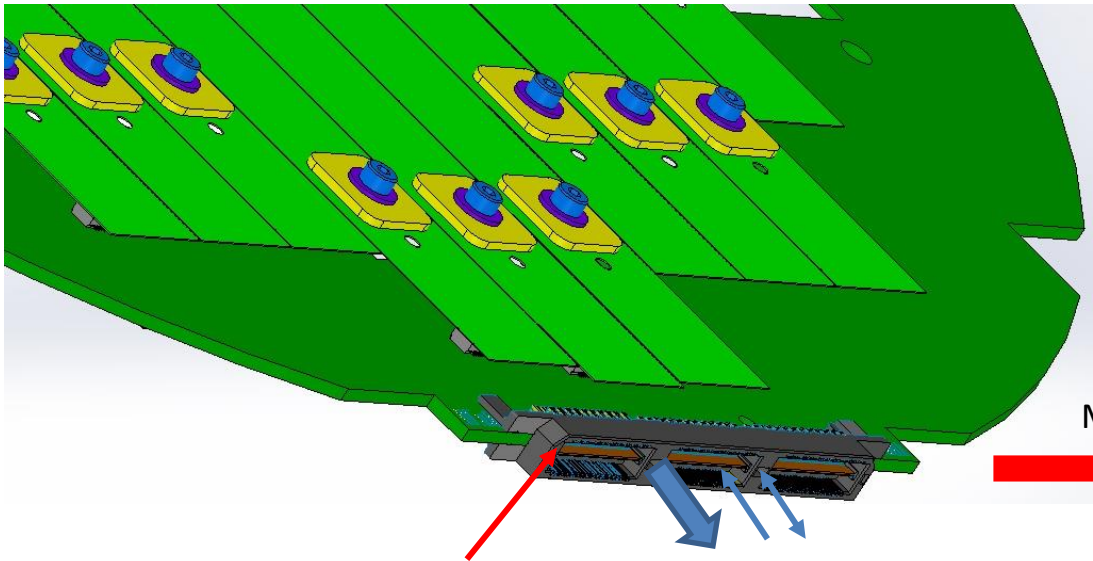
Mate with
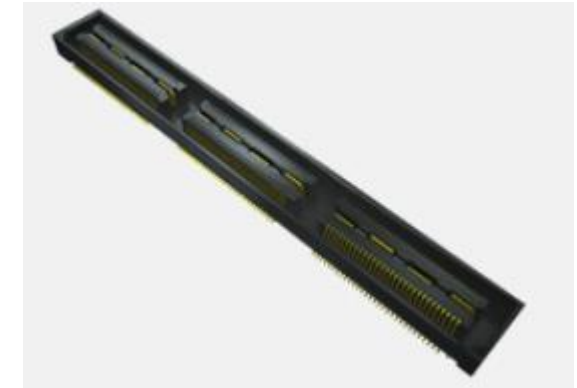
QSH-090 (SAMTEC)

On motherboard

Connectors for differential pairs QTH-EM-090 (SAMTEC)

⇒   DATA, Clock, Control links from/to sensors

⇒   Temperature measurement links (CTN)

⇒   ON/OFF signals for DC/DC converters (only for disk3 and 4)

⇒   Latchup measurement (on DC/DC converters for disk3 and 4)

II. On-detector studies

3.   Power supply unit

⇒ Provides +1,8V (analog and digital) for disk 0, 1 and 2

⇒ On board latchup measurement

⇒ Connection for +12V input and +1,8V outputs (analog and digital)

Connection for input/output voltage

8 DC/DC converters for one side of a disk

Connector for DC/DC converters slow control signals (ON/OFF, temperature and latchup measurement)
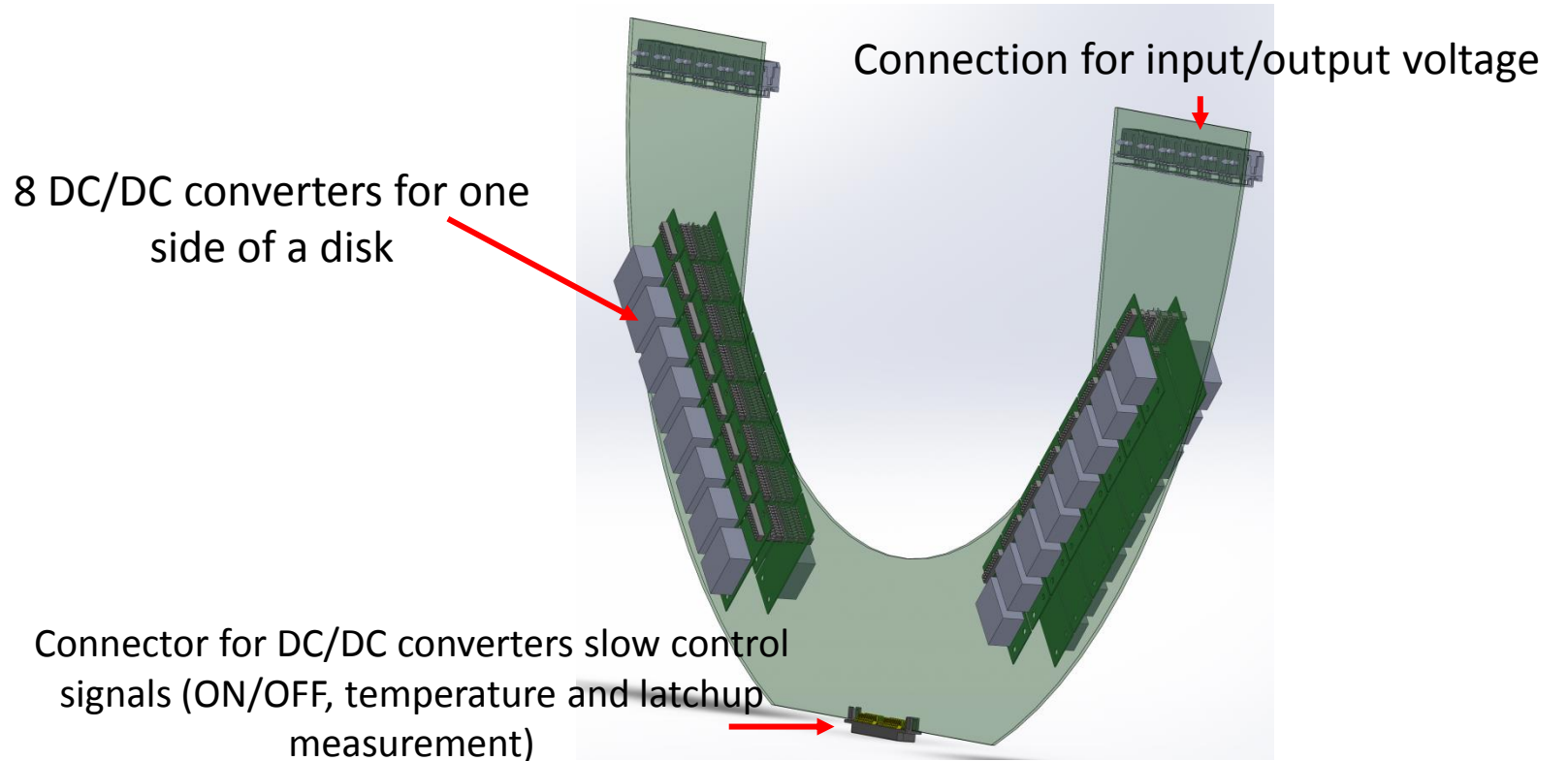
View of the first proposal power supply unit (only for disk 0 and 1)

II. On-detector studies

3. Power supply unit

Space for water cooling system between rows of DC/DC converter
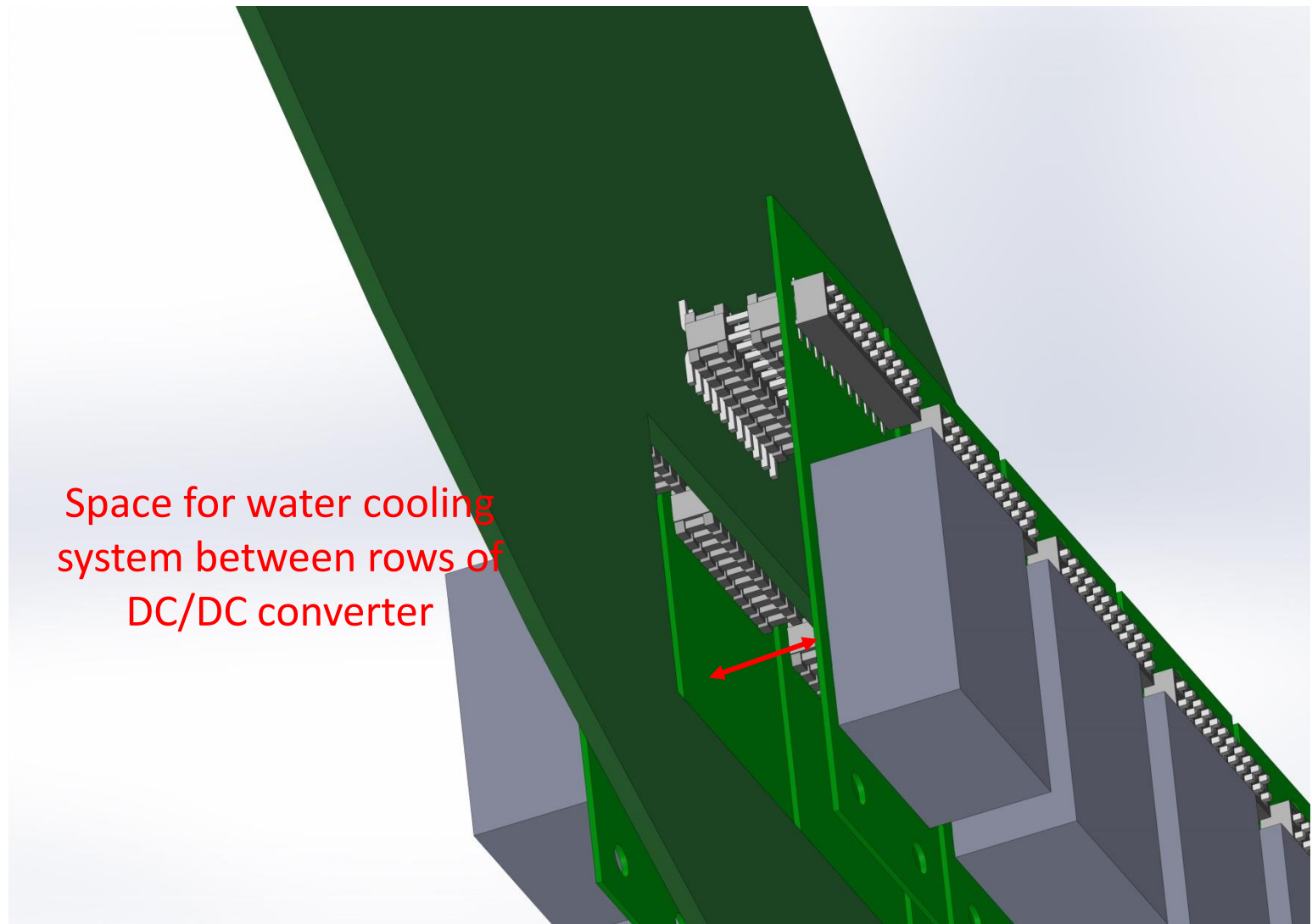
II. On-detector studies

3. Power supply unit

$\Rightarrow$ New solution under study for power supply unit

$\Rightarrow$ Like disk assembly (Mechanical spacer between 2 PCBs)

$\Rightarrow$ Better rigidity

$\Rightarrow$ Water cooling system could be integrated in the mechanical part

II. On-detector studies

4. Motherboards

Motherboards to interface disks to Twinax cables
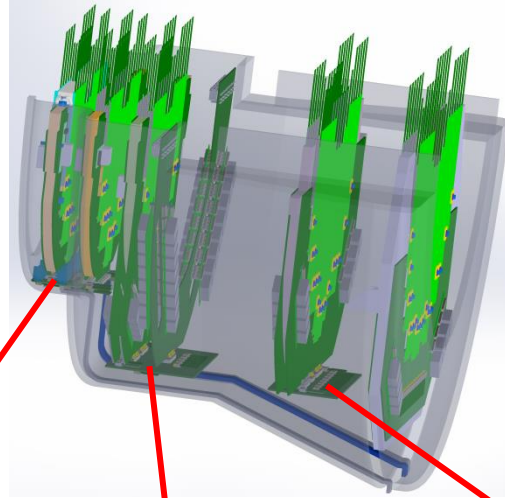
Studies of the mechanical structure are made by WG7 (Subatech Nantes)
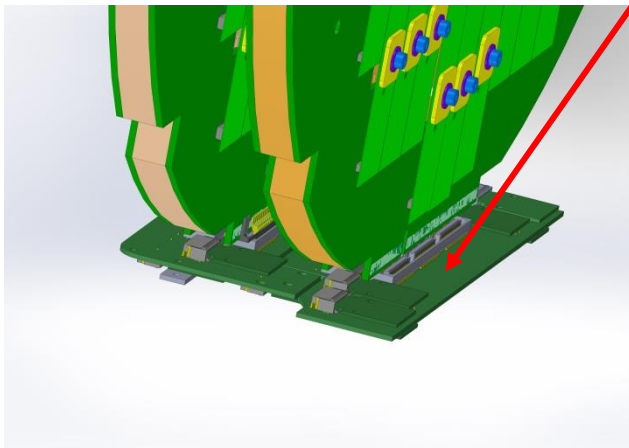
Disk 0 and Disk 1
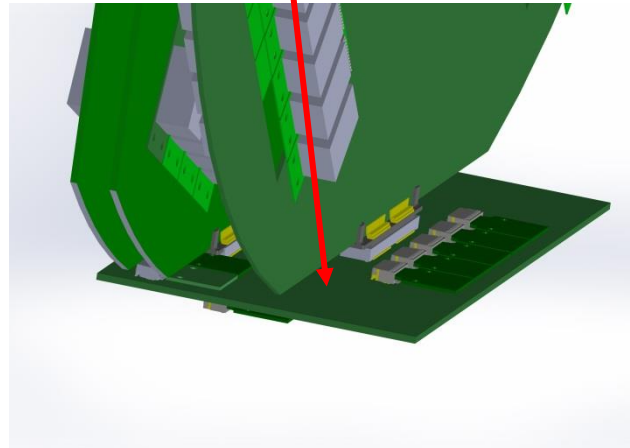
Power supply unit + Disk2
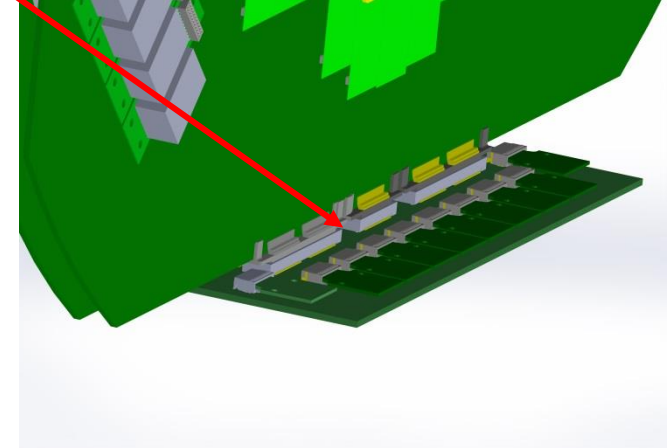
Disk3

II. On-detector studies

4. Motherboards

Twinax cables with FireFly connection (SAMTEC)

Exemple of a motherboard

Ribbon of 12 twinax cables

FireFly connector

5.25mm

15mm
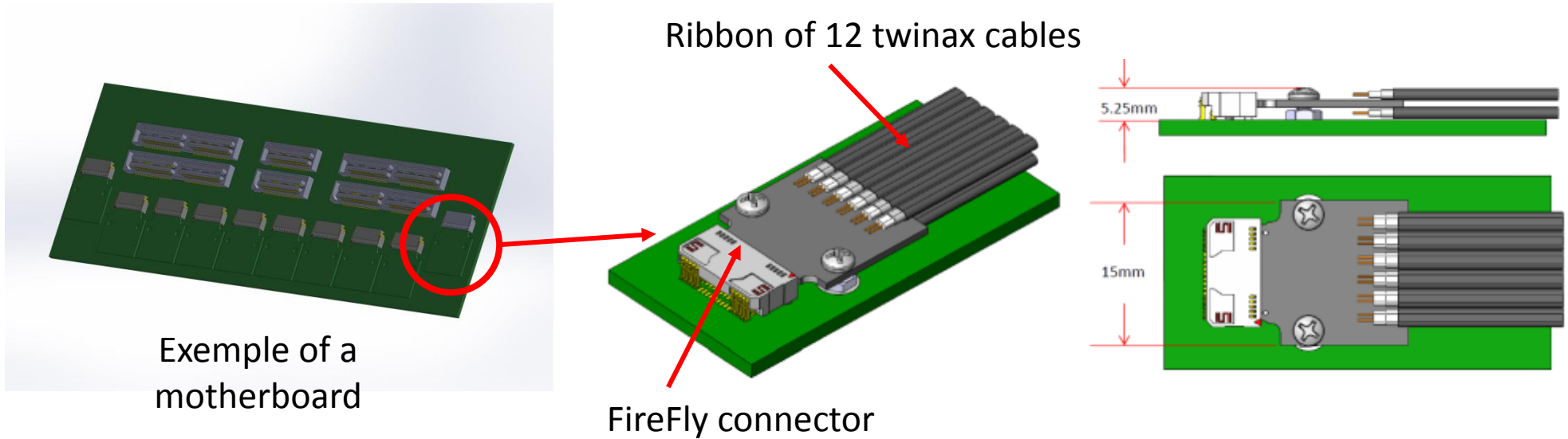
Custom prototype by SAMTEC for ITS

II. On-detector studies

5. Barrel Patch Panel

Half MFT view in the barrel

Barrel Patch panel used to interconnect twinax cables from the motherboard (inside cone) to the 4m twinax cables from the readout unit

Services repartition area
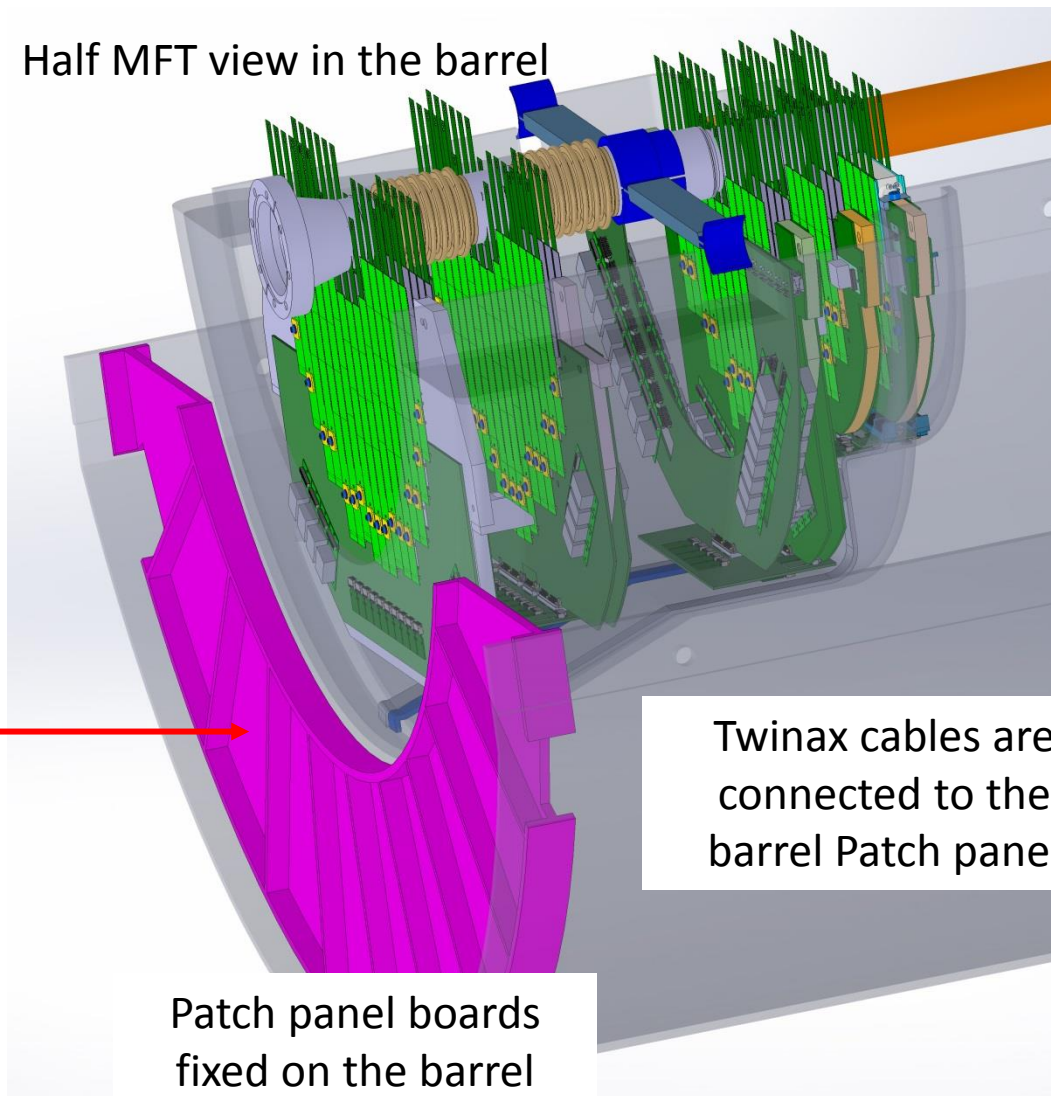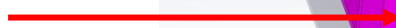
Twinax cables are connected to the barrel Patch panel

Patch panel boards fixed on the barrel

III. Off-detector studies (Readout Unit)

1. Synoptic and numbers

General readout diagram of the MFT

Common ITS/MFT readout architecture (Inner Barrel + Twinax)

III. Off-detector studies (Readout Unit)

General readout diagram of the MFT
Common ITS/MFT readout architecture (Inner Barrel + Twinax)

Barrel Patch Panel

Radiation zone | Radiation-free zone

Half-MFT (BOTTOM)
Half-MFT (TOP)

Half-Disk 4
Half-Disk 3
Half-Disk 2
Half-Disk 1
Half-Disk 0

Half-Plane 0 (Back)
Half-Plane 0 (Front)

12 up to 17 Ladders

Slow Control
Power
HS DATA

Half-Plane PCB

FPC

1 up to 5 Pixel Sensors

200 diff pairs
176 diff pairs
128 diff pairs
112 diff pairs
112 diff pairs

728 diff pairs
728 diff pairs

4 m Twinax cables

Power Supply
Power Supply

MFT Backend Readout Unit

concentrator

CTP

Common Readout Unit

Optical fibers

III. Off-detector studies (Readout Unit)

1. Synoptic and numbers

Numbers of sensors (with power consumption) and numbers of differential links at different level in the MFT

One side of
Half disc
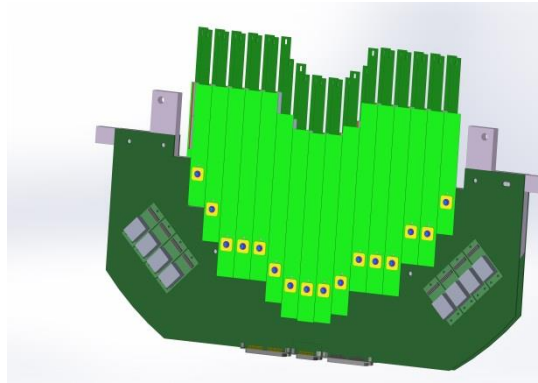
One plane
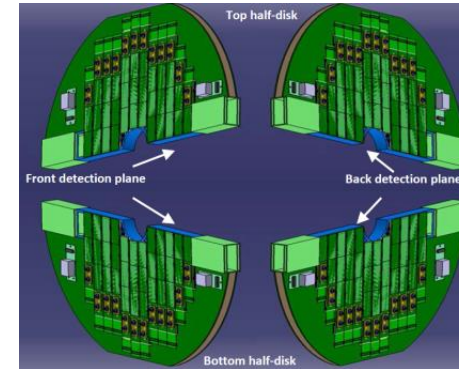
		Half-disc 0 one side	Half-disc 1 one side	Half-disc 2 one side	Half-disc 3 one side	Half-disc 4 one side	Plane 0	Plane 1	Plane 2	Plane 3	Plane 4	All MFT
sensors	Nbr ALPIDE	33	33	39	57	66	132	132	156	228	264	**912**
Power consumption	1.8V analog 20mA/sensor	660mA	660mA	780mA	1,14A	1,32A	2,64A	2,64A	3,12A	4,56A	5,28A	**18,24A**
Power consumption	1.8V digital 105mA/sensor	3,47A	3,47A	4,1A	5,99A	6,93A	13,88A	13,88A	16,4A	23,96A	27,72A	**95,84A**
Differential links	links HSDATA + DCLK links + DCTRL links	57	57	65	89	100	228	228	260	356	400	**1472**

III. Off-detector studies (Readout Unit)

1.   Synoptic and numbers

Total throughput for each disk and for whole MFT
(without safty factor)

	Throughput (Mb/sec) Front and back side
Disk 0	10283,8
Disk 1	10375
Disk 2	11377,2
Disk 3	11959,6
Disk 4	12939
Total MFT	**56934,6 Mb/s**
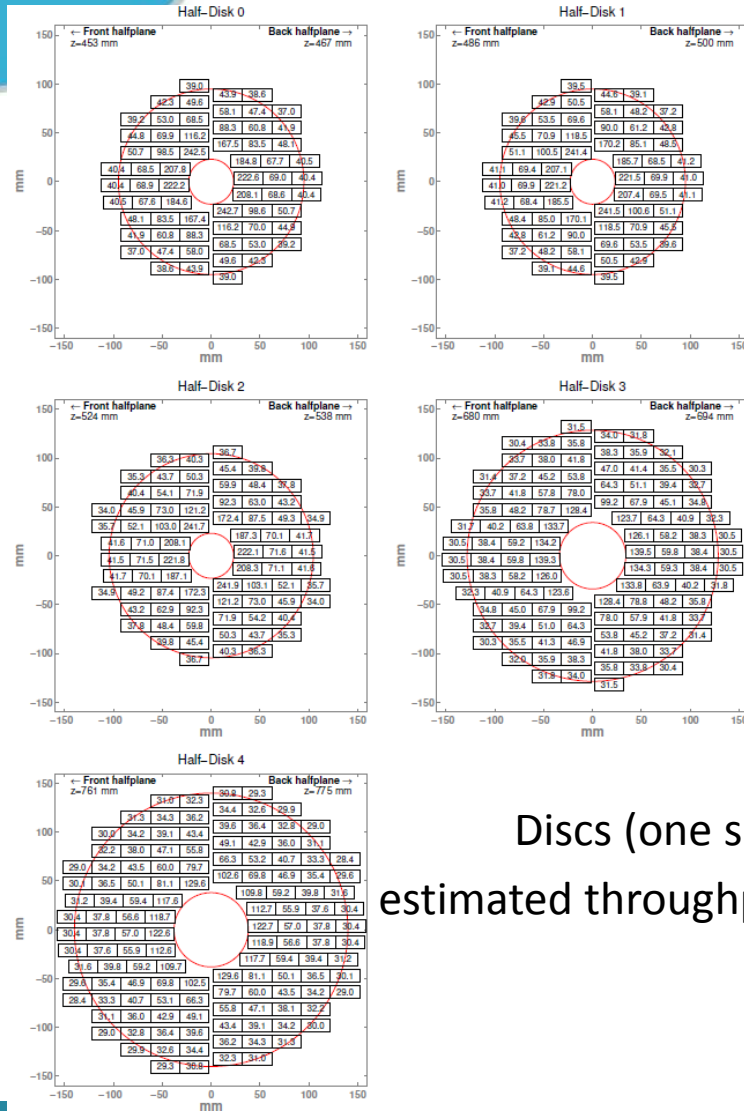
Discs (one side)
estimated throughput/sensor

III. Off-detector studies (Readout Unit)

1.   Synoptic and numbers

Estimated Data throuput

For a quarter of Disk (One PCB)
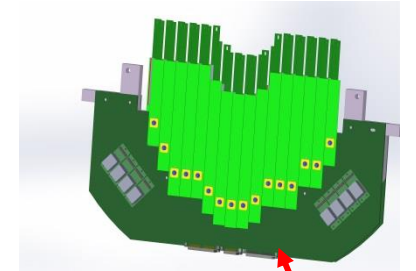
PCB disk

	PCB disk 0	PCB disk 1	PCB disk 2	PCB disk 3	PCB disk 4	Total MFT
Nbr Data links (1,2Gb/s)	33	33	39	57	66	912
Max data rate possible (Gb/s)	39,6	39,6	46,8	68,4	79,2	1094,4 Gb/s
Estimated Data throuput with safty factor of 2 (Gb/s)	5,2	5,2	5,8	6	6,6	115,2 Gb/s
Number of GBT needed (4,8Gb/s)	2	2	2	2	2	10

Readout Unit

Nbr of data links
Twinax cables

Nbr of GBT links
Optical links
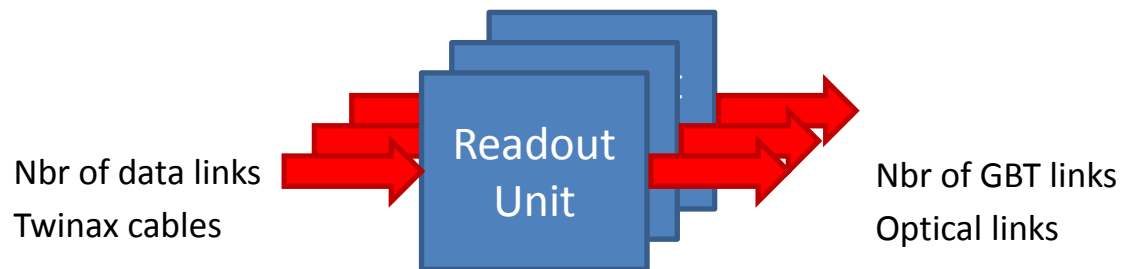
III. Off-detector studies (Readout Unit)

2. Readout Unit boards

ITS Inner Barrel Solution

RU for 1 stave (9 sensors) with 3 GBT links

IB RU with 1* IGLOO2 with 16 SERDES

9 links to receive one ITS stave
vs
MFT has not got fixed number of data links per ladder

2   3   4   5

Only one Clock & Ctrl link
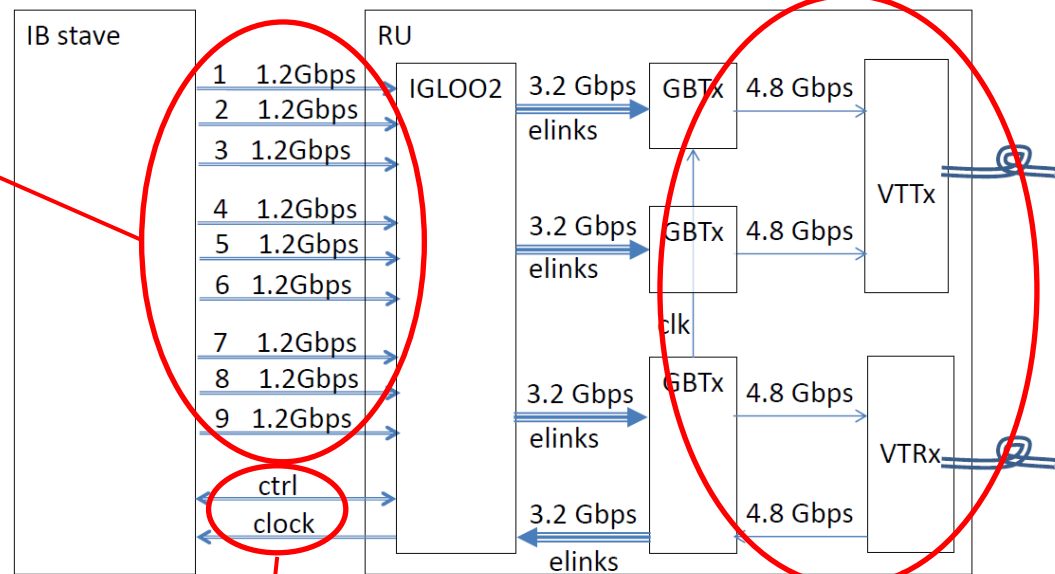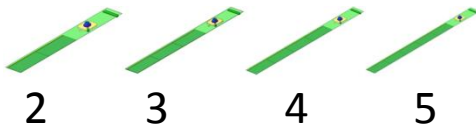
Upstream 14,4 Gbps

Downstream 4,8 Gbps

the capacity of the output data flow is oversized for MFT readout

III. Off-detector studies (Readout Unit)

2. Readout Unit boards

11 or 12 twinax cables

ITS connection
- 9 ALPIDEs data links
- 1 clock & 1 Ctrl for one stave

FireFly connection

5.25mm

15mm

9 data links

Clock Ctrl

IGLOO2 FPGA
Microsemi

GBTx

GBTx

GBTx

VTTx

VTRx

Mezzanine board (FMC connecting but not compliant with standard)
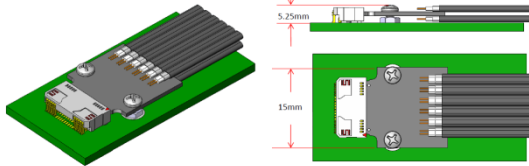
MFT connection
- Gathering of 9 sensors
- Several clocks & Ctrl links
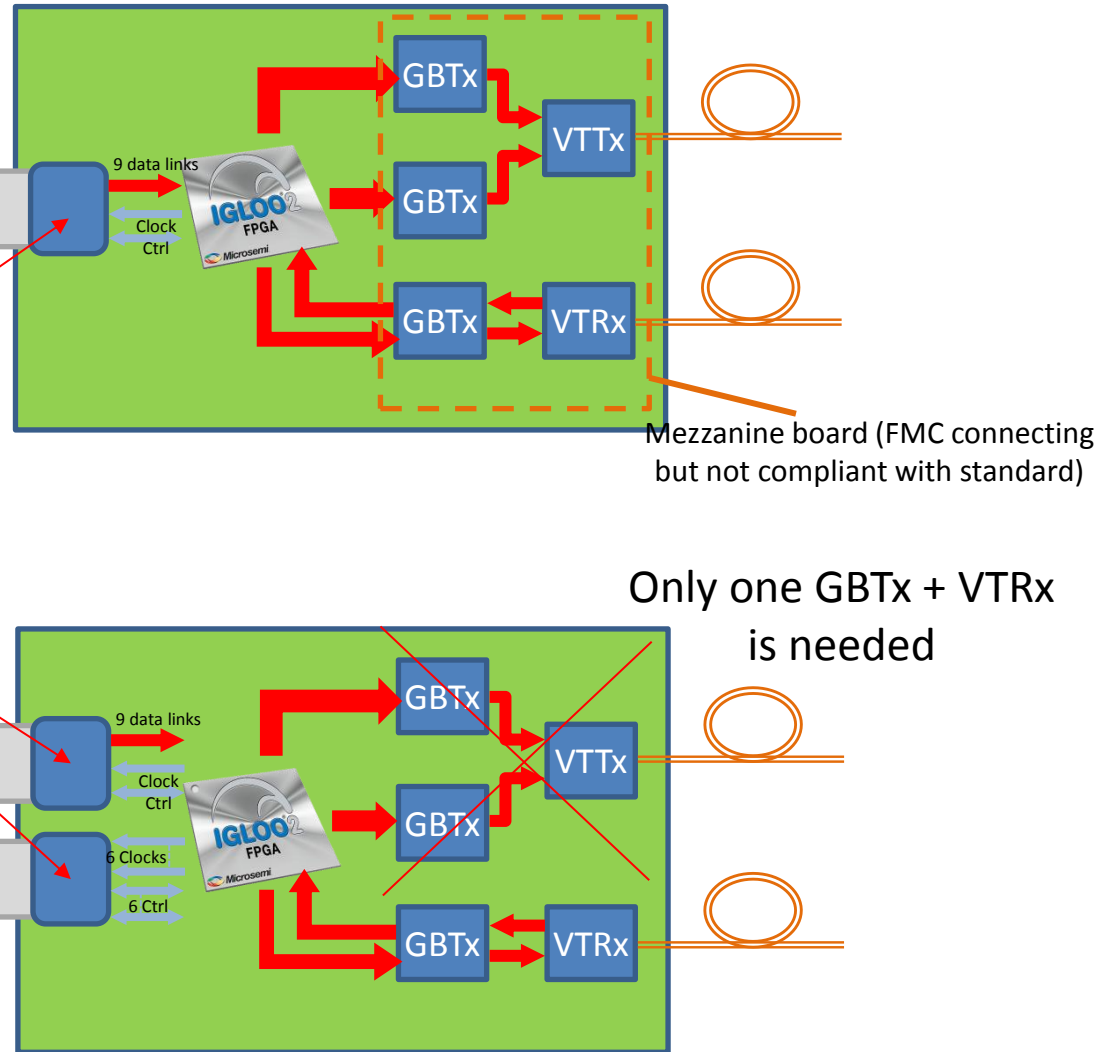
Only one GBTx + VTRx is needed

9 data links

Clock Ctrl

6 Clocks

6 Ctrl

IGLOO2 FPGA
Microsemi

GBTx

GBTx

GBTx

VTTx

VTRx

11 or 12 twinax cables

III. Off-detector studies (Readout Unit)

2.   Readout Unit boards

Exemple of gathering for ladders of one side of Disk 0
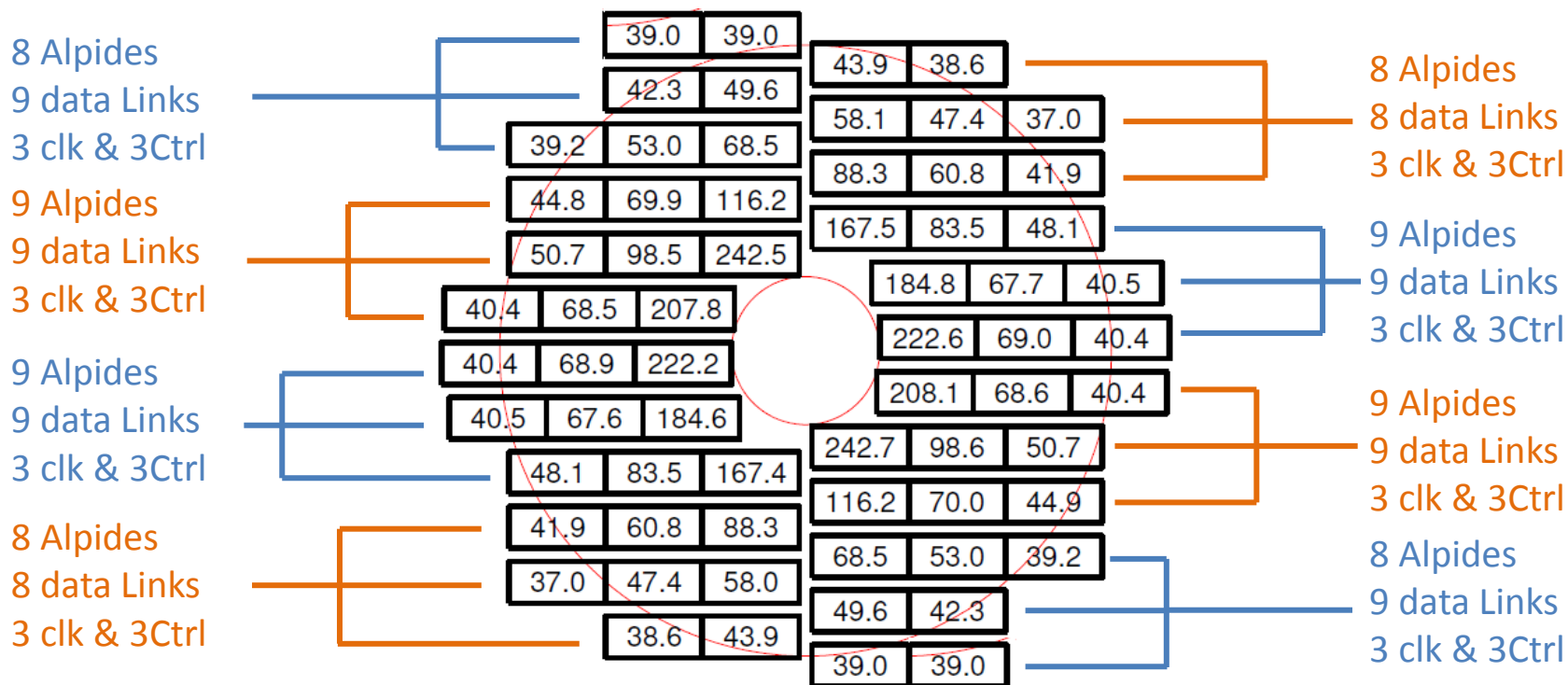
- 8 RU boards per side of disk 0 => 16 RU boards for Disk 0

IV. WG6 readout tasks
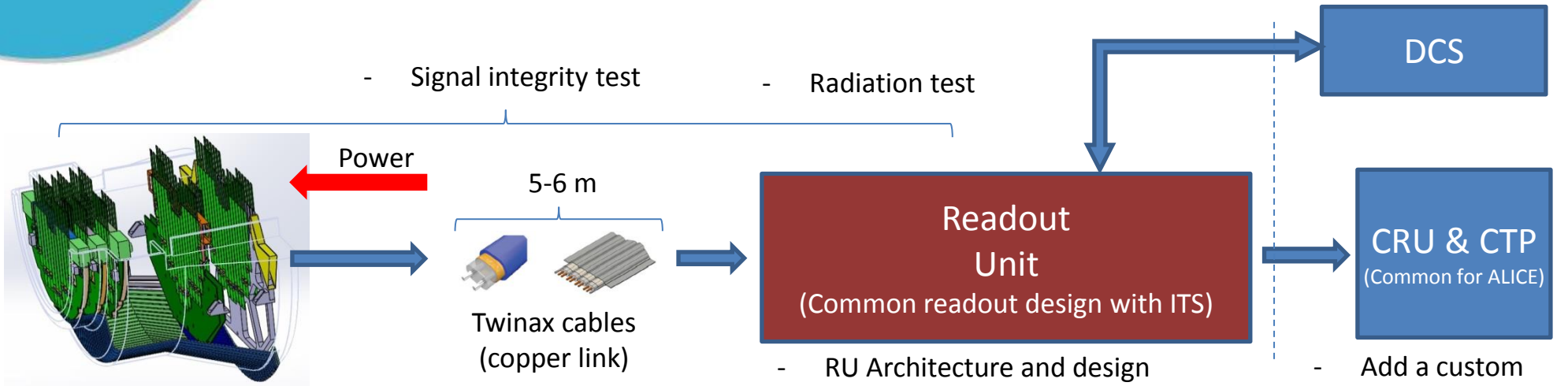
- Signal integrity test   - Radiation test

DCS

Power

5-6 m

Readout Unit
(Common readout design with ITS)

CRU & CTP
(Common for ALICE)

Twinax cables
(copper link)
1,2 Gb/s

- Links conections & integration inside MFT cone (Control, data, clock)
- Power distribution (FEAST DC/DC)
- Back bias regulation
- PCBs design & manufacturing
- Monitoring (power, temperature, …)
- Latchup detection
- Patch panel design
- …

- RU Architecture and design (hardware, FPGA, GBT, crate, …)
- Follow ITS readout development
- Interact with DCS team

FPGA features

⇒ Receive Data from sensor
⇒ Control to/from sensor
⇒ Power control
⇒ Busy managment
⇒ …

⇒ Trigger managment
⇒ Data building (concentrator?) & transmission through GBT link
⇒ Remote firmware deployment
⇒ …

- Add a custom functions in CRU firmware?
- Follow CRU development

IV. WG6 readout tasks

- Signal integrity test
- Radiation test

Power

5-6 m

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Cyrille Guérin (IPNL)

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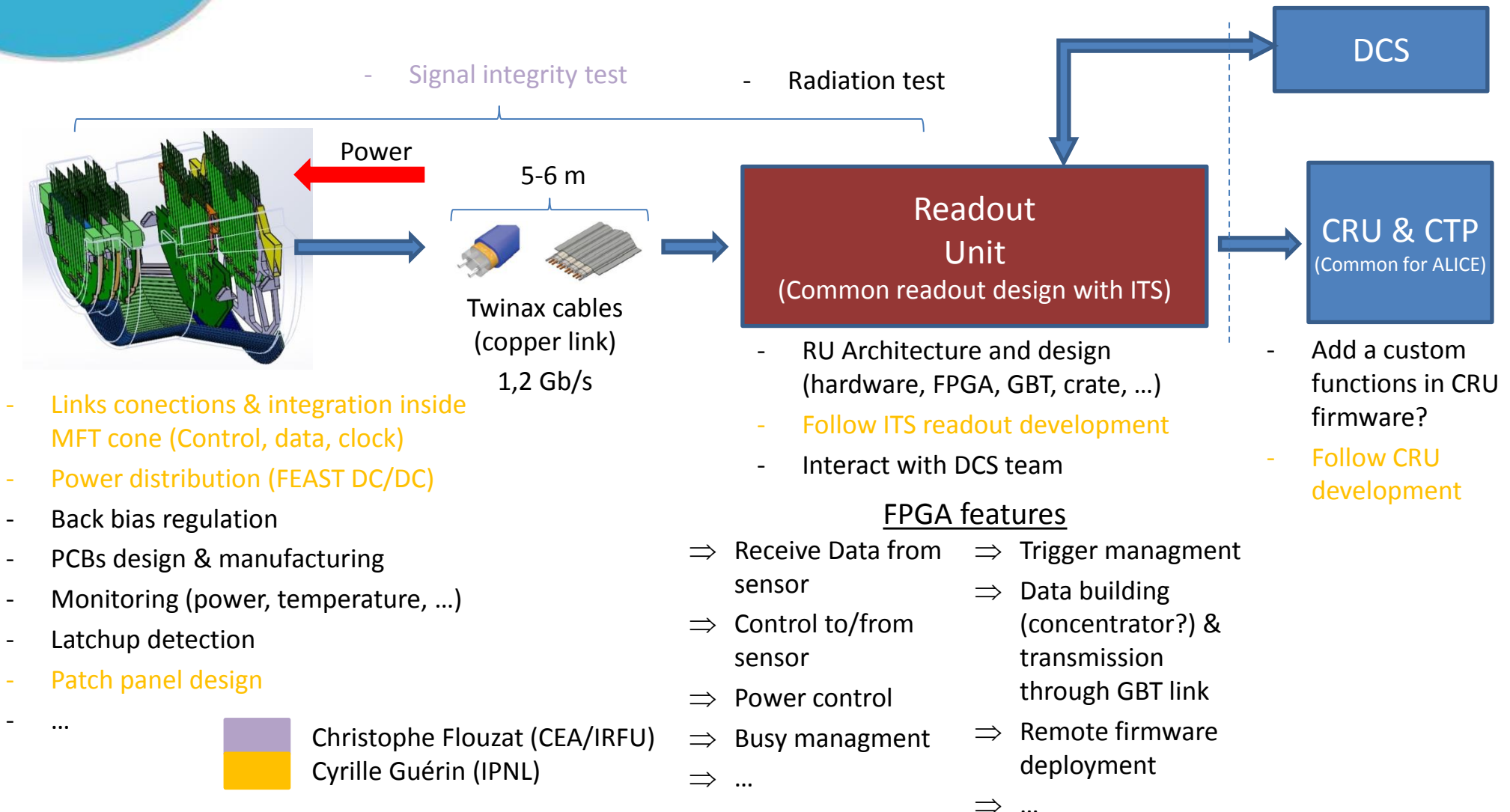- Add a custom functions in CRU firmware?
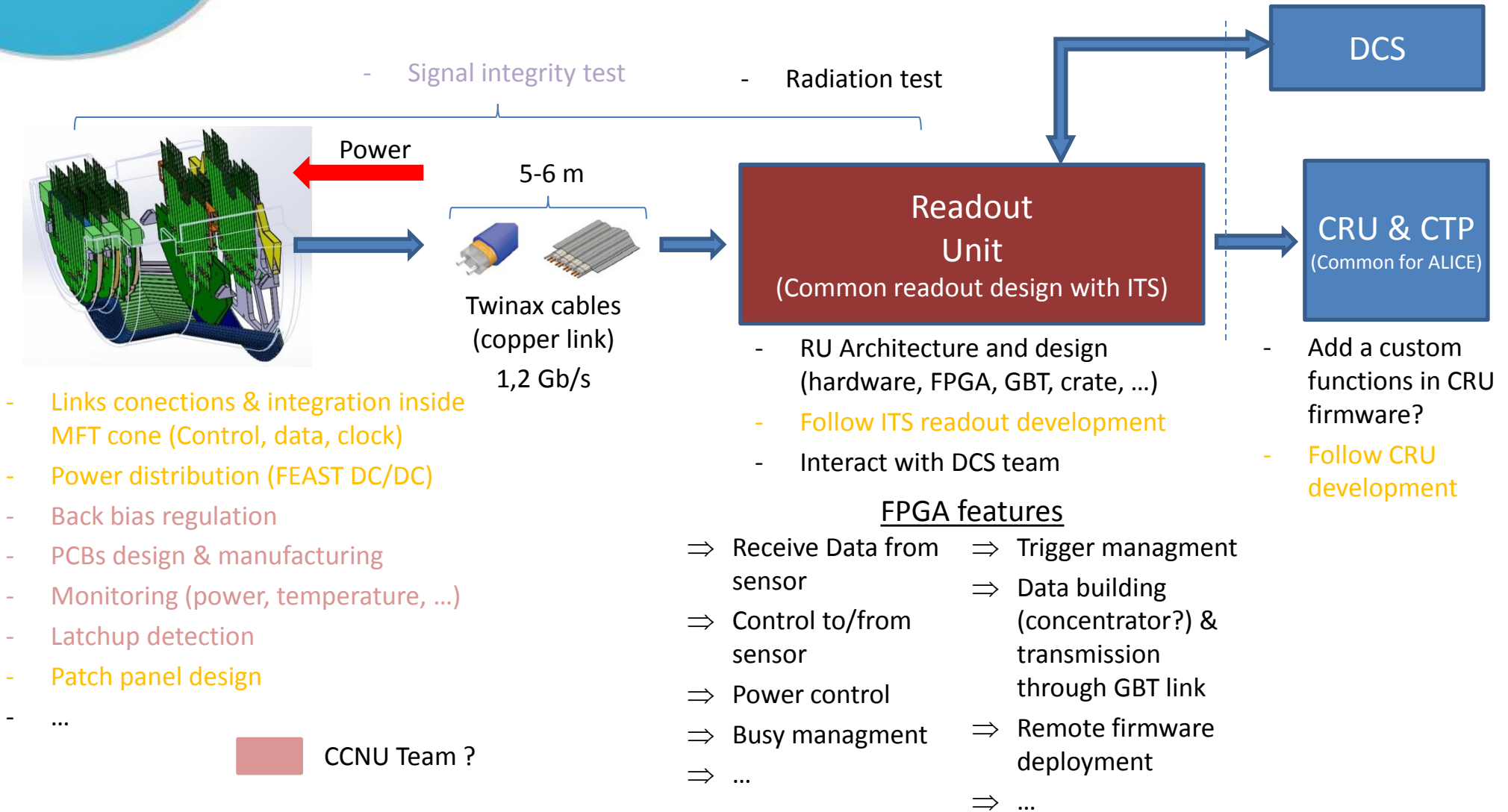- Follow CRU development

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⇒ …

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⇒ Remote firmware deployment
⇒ …

CCNU Team ?

V. Human resources and needs

Currently:

Christophe Flouzat (CEA-Saclay – 0,2 FTE2015 – 0,3FTE2016) Signal integrity tests on twinax link

Cyrille Guérin (IPNLyon - 0,8 FTE) convener of WG6, works on

- connection studies (inside cone & patchpanel)

- follow ITS readout meetings and just start study of MFT RU architecture to compare with ITS's one

Under discussions for designing ON-detector boards :

- Dr DAICUI Zhou, WANG Dong and their team (CCNU, Wuhan)

Discussions engaged with Indians for 0,6FTE

- Difficulties to identify the task on which they would like to participate

Needs reinforcement on the Readout Unit design (Off-detector):

- 1,5 FTE2015 and 0,75 FTE2016 in case of Indiens participation
- Otherwise 2,1 FTE2015 and 1,35 FTE2016

V. Human resources and needs

Reinforcement for

Two parts on the Readout Unit design

Hardware (RU board design)

- Continue to follow ITS design of the RU board
    - Interfaces (CRU, CTP, PowerUnit ...)
    - Hardware (FPGA, GBTX, VTx)
- Propose a dedicated architecture for MFT and discuss with ITS WP10 tem to design this common RU
- Interact with the group which design the firmware
- Interact with DCS team
- Provide a prototype of a RU board

Firmware (FPGA architecture and configuration)

- Follow firmware design of ITS
- Identify blocks in FPGA which require modification for MFT
- Involvement in the firmware design of the ALICE CRU
- Provide the firmware of the RU board

In both cases => strong interaction with ITS WP10 team

VI. Discussions

Thank you