Radiation-Tolerant SAR ADC Architecture and Digital Calibration Techniques

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PH-ESE Seminar, CERN

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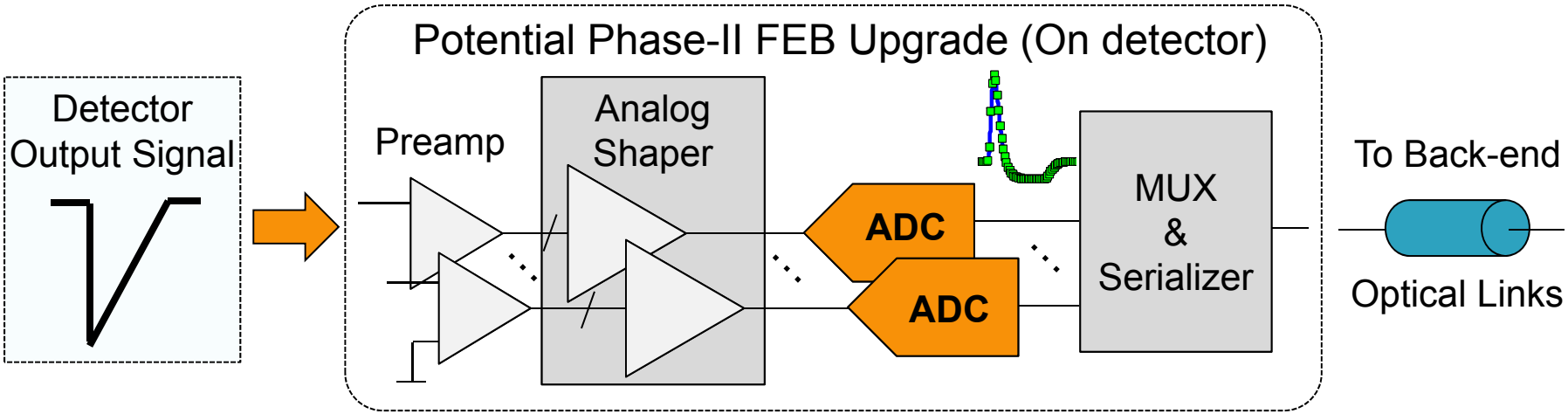
Phase-II LAr AFE Upgrade Needs



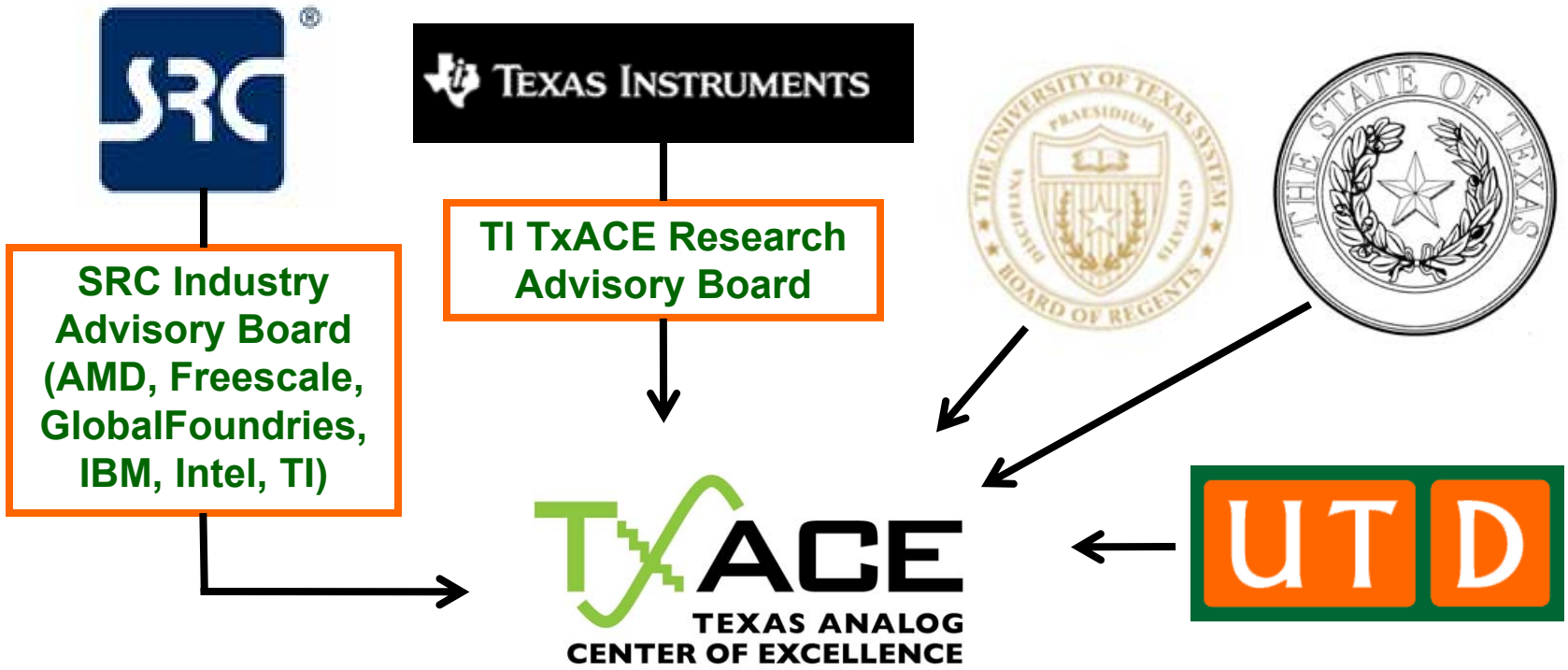
- Trigger-less, continuous signal digitization & data transmission
- Potential technical challenges:
  - ❑ **Minimum 12-bit, 40-MSPS ADC w/ low power**
  - ❑ Back-end signal processing w/ elevated pileup noise (80 MSPS can significantly aid the energy resolution…)

Potential ADC Specs for P2 Upgrade

	Plan I	Plan II
Gain Segmentation	4 scales	2 scales
ADC Resolution	**12 bits**	**14 bits**
Sample Rate	**40 / 80 MS/s**	**40 / 80 MS/s**
Technology	CMOS	SiGe & CMOS
Feature	SoC integrated	MCM integration

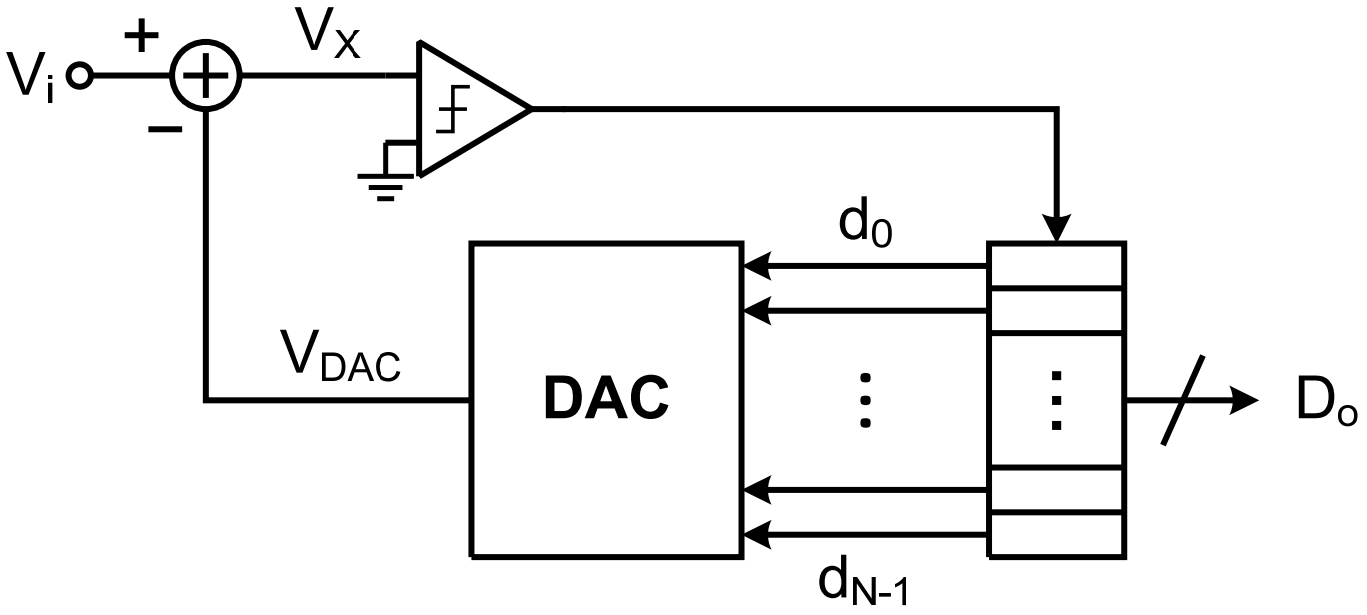
- Our (TxACE, UTD) goals and approaches:
  - ❑ 12/**14** bit, 40/**80** MS/s, 25 mW, 1.2 V, 65-nm CMOS
  - ❑ SAR architecture [1] and digital calibration [2, 3]
  - ❑ TID results presented at TWEPP'14, SEE/SEU will be addressed in the current design (R&D of FY15)

SRC Texas Analog Center



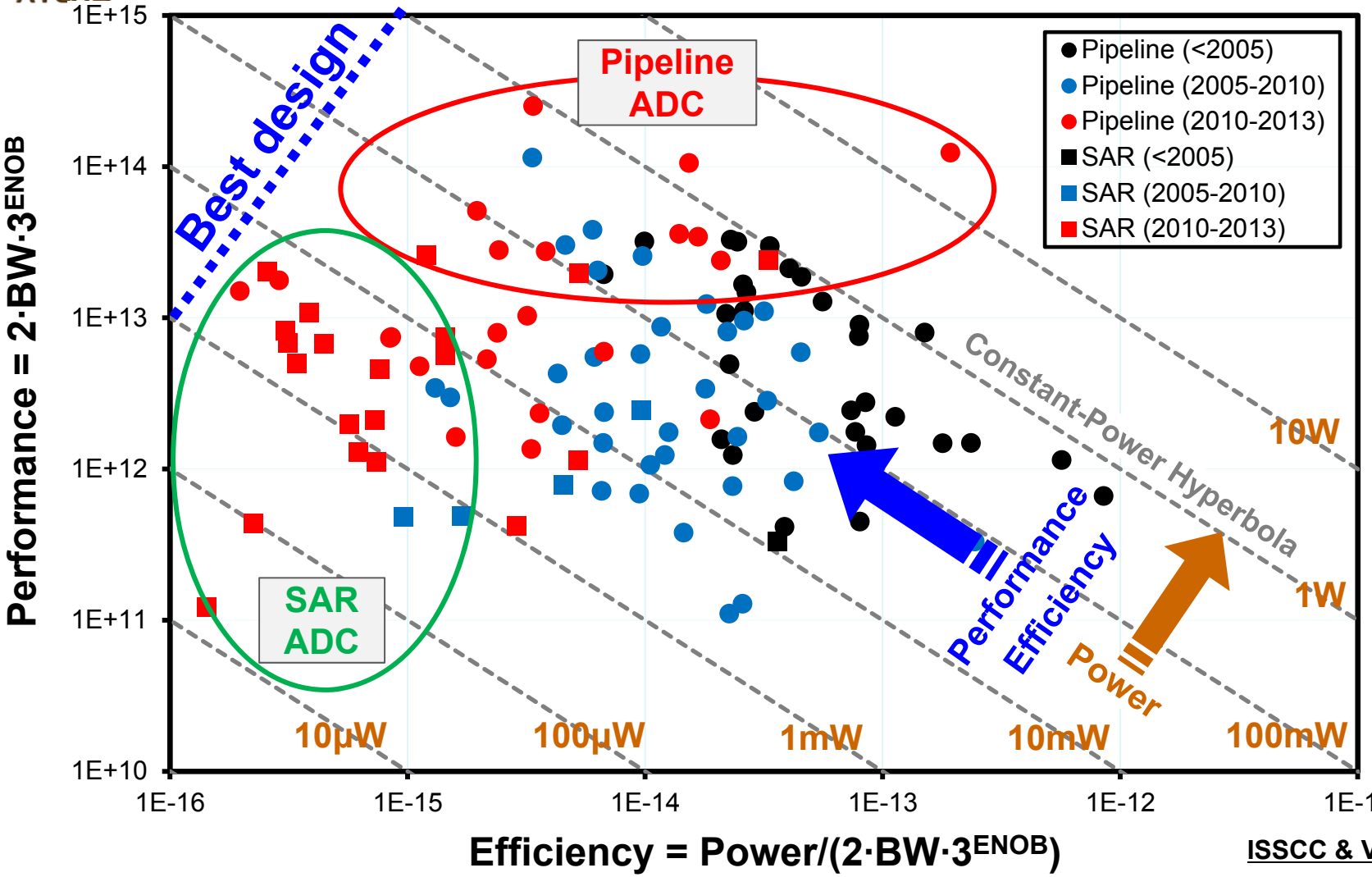
Our proposed ADC work for LAr Phase-II upgrade will be carried out in TxACE, an SOA A/MS/RF R&D facility

SAR ADC Architecture



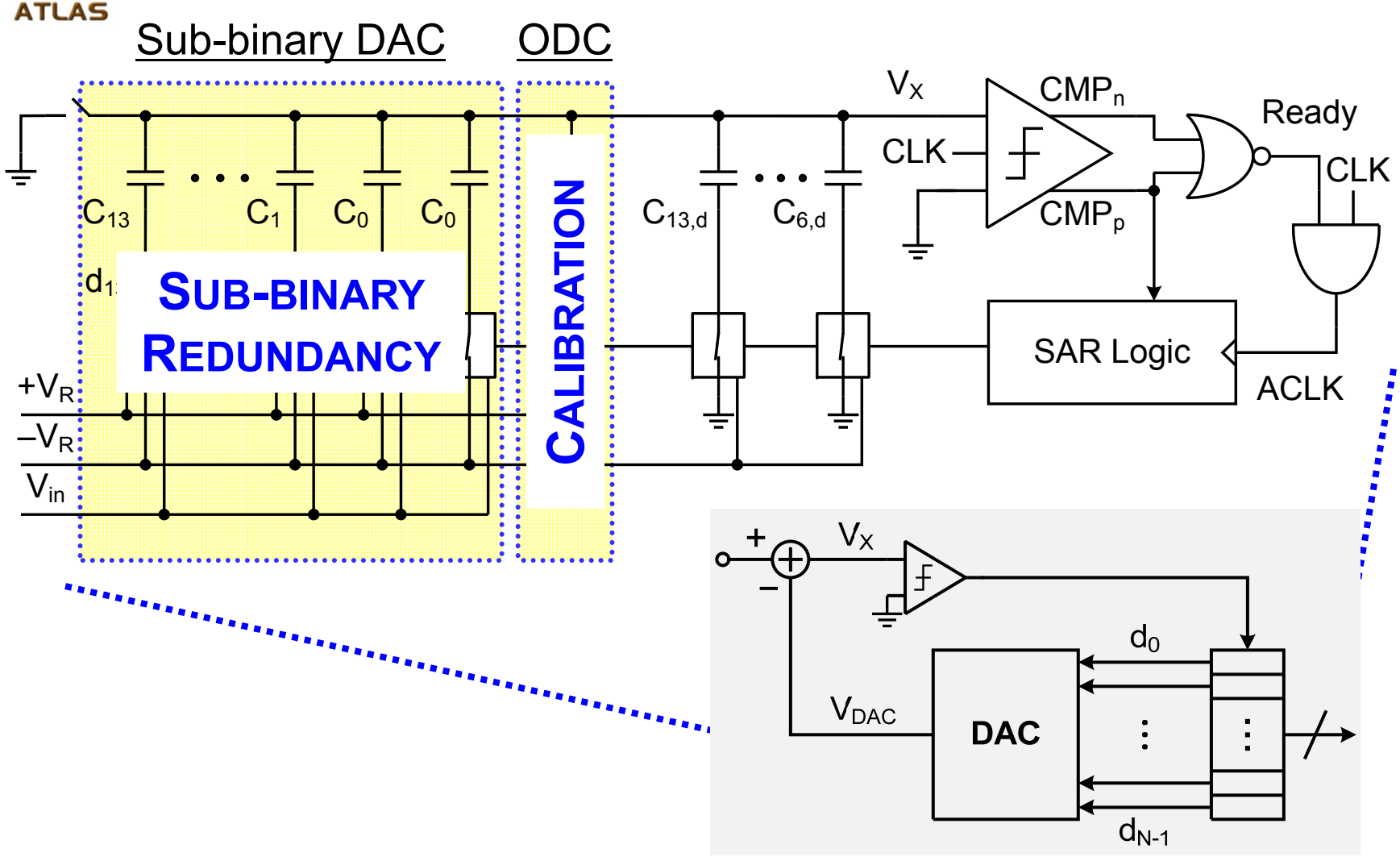
SAR = 1 comparator + 1 DAC + digital logic

Trend of SAR and Pipelined ADCs

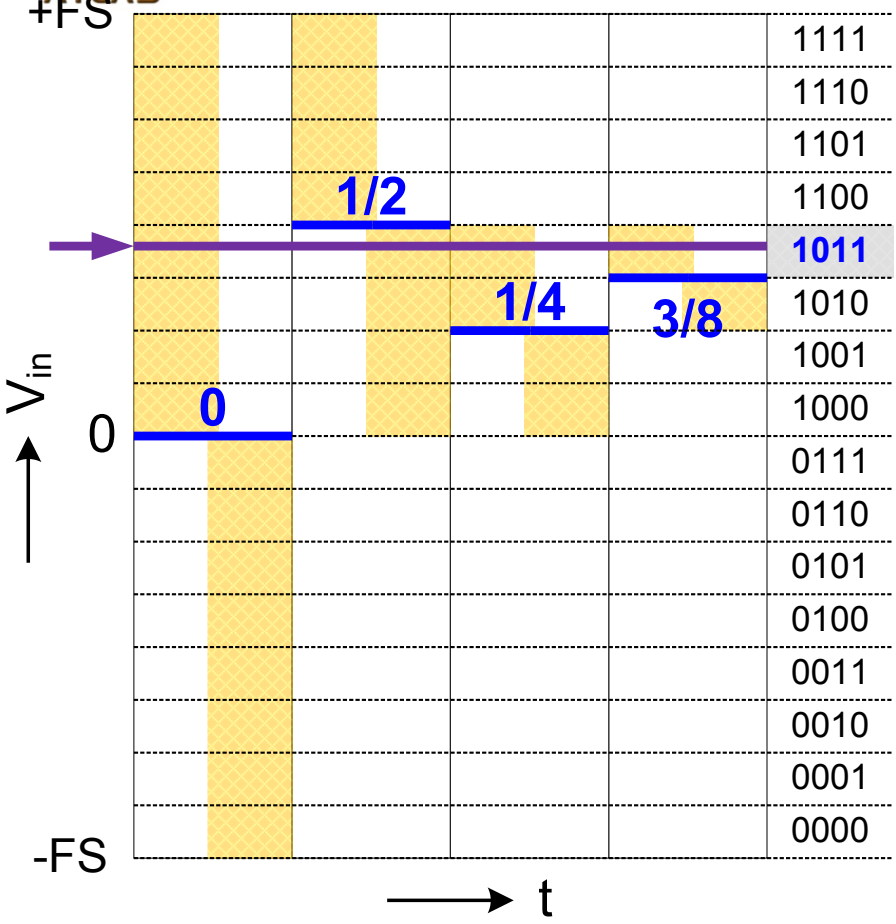


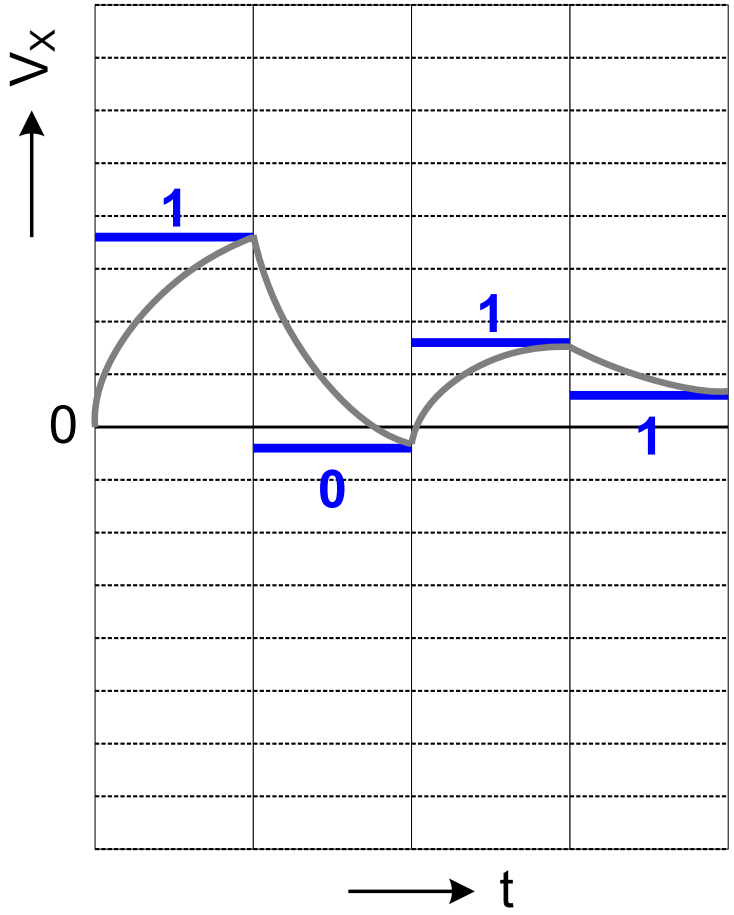
ISSCC & VLSI data

12-bit, 45-MS/s, 0.13-µm CMOS ADC



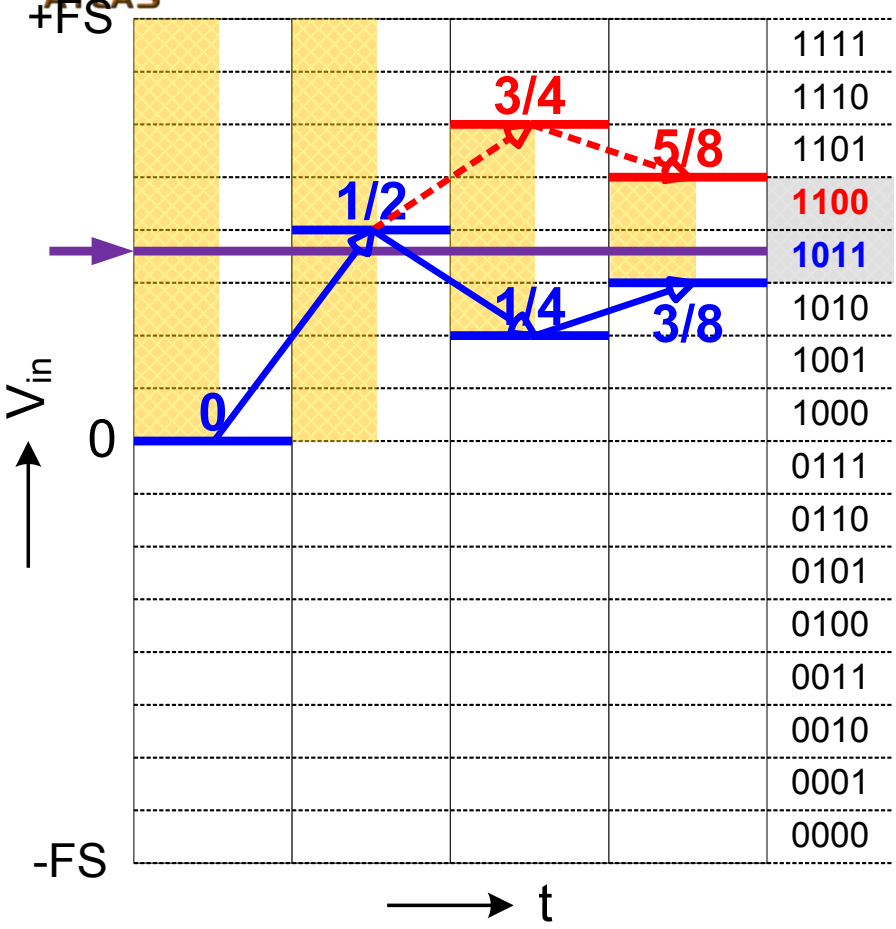
Binary Search

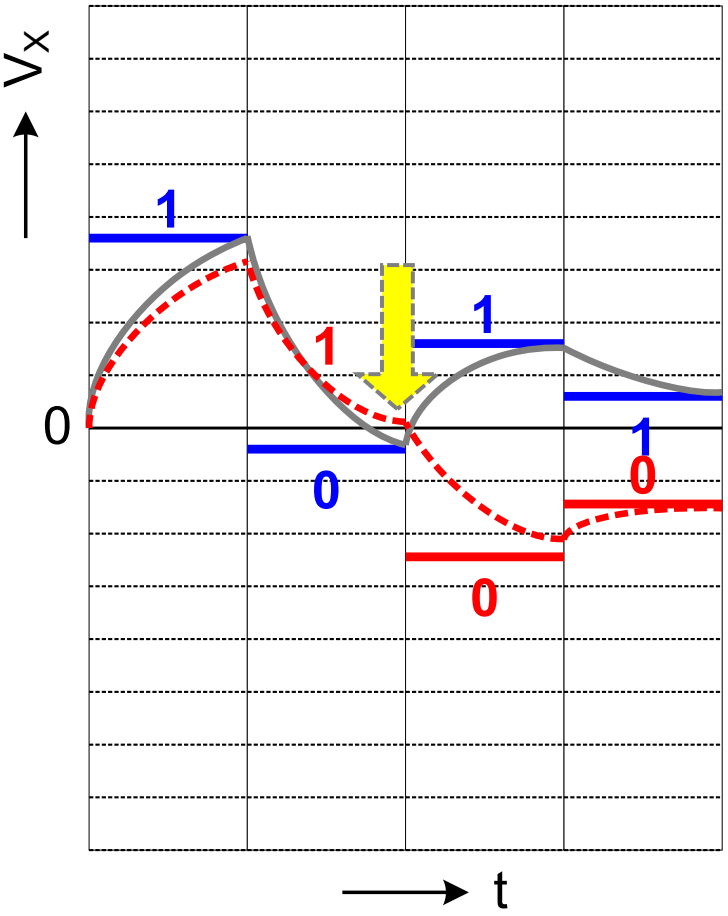




- When everything is ideal…

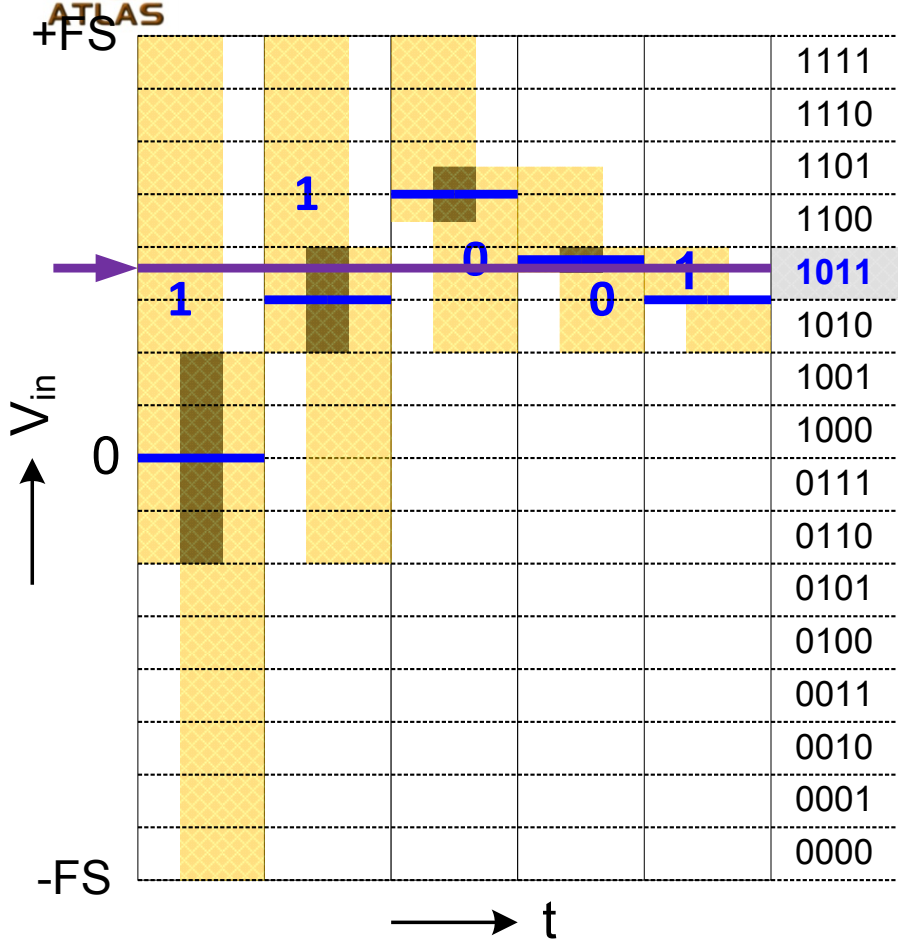
Binary Search w/ Dynamic Error

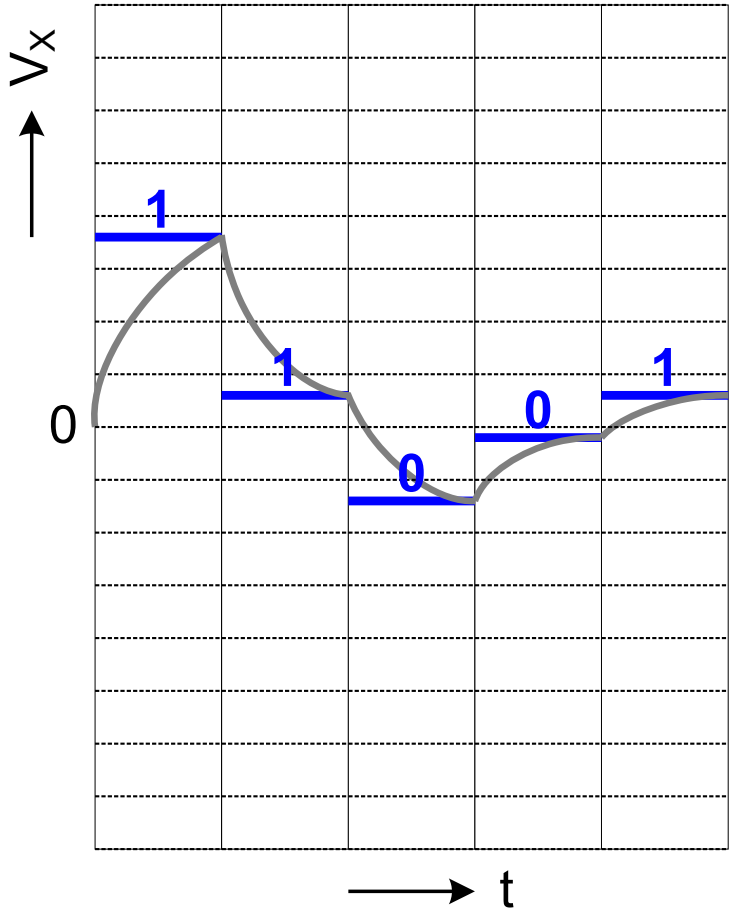




- Settling error, comparator hysteresis etc.

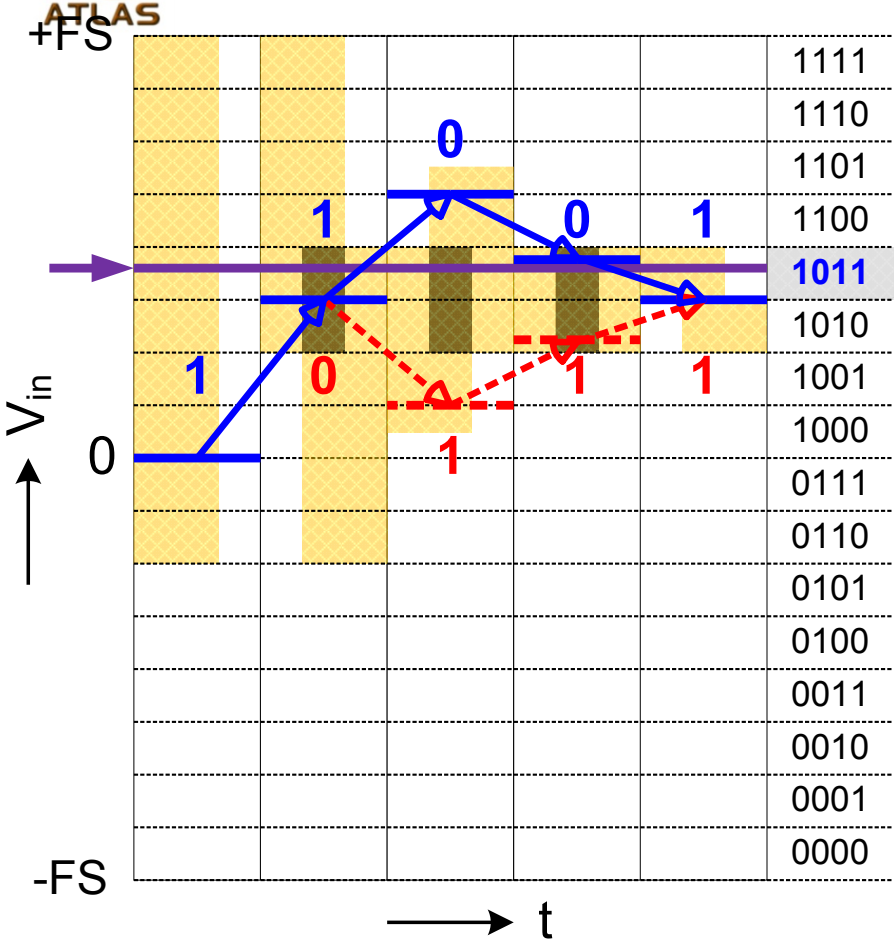
Overlapping Search Ranges

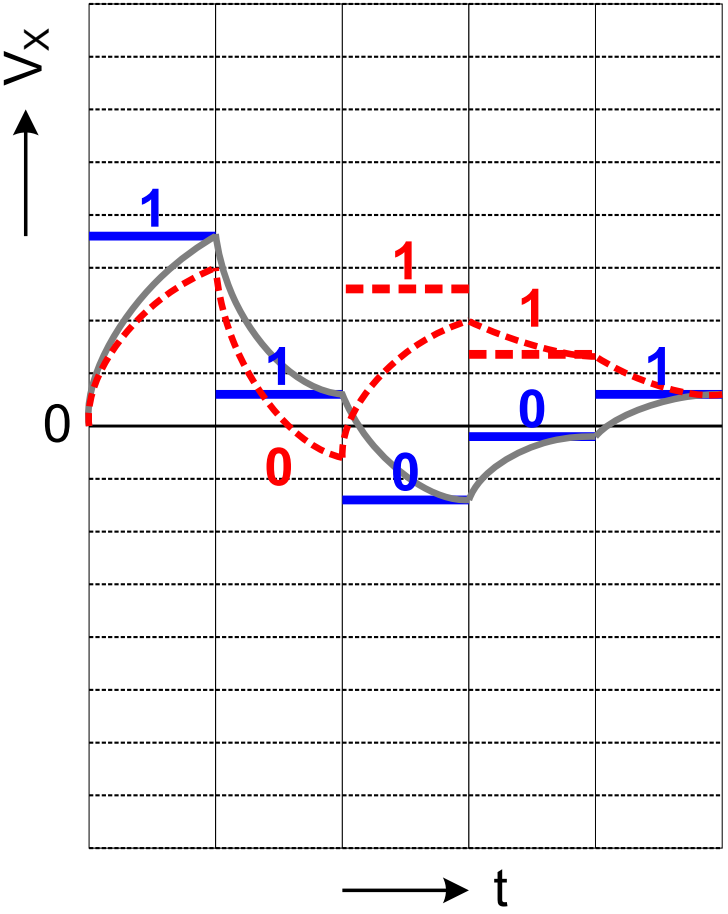




- Results indicate decision trajectory, no longer binary-coded

Redundancy of Sub-binary Search



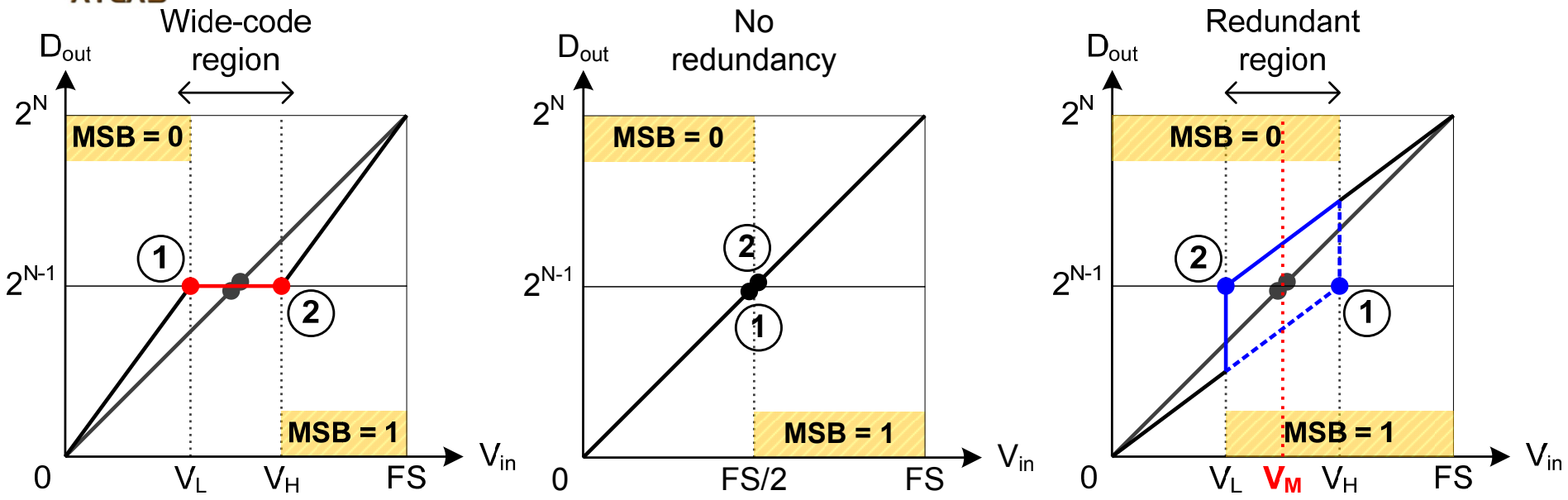


- Dynamic decision errors absorbed by redundancy

SAR ADC w/ Redundancy

- Redundant conversion consumes more bit cycles, but can recover intermediate decision errors.
- Redundancy can be exploited to expedite conversion progress or to save power.
- **Redundancy can also be exploited to reduce SEE.**
- **Redundancy can also be exploited to enable digital calibration.**

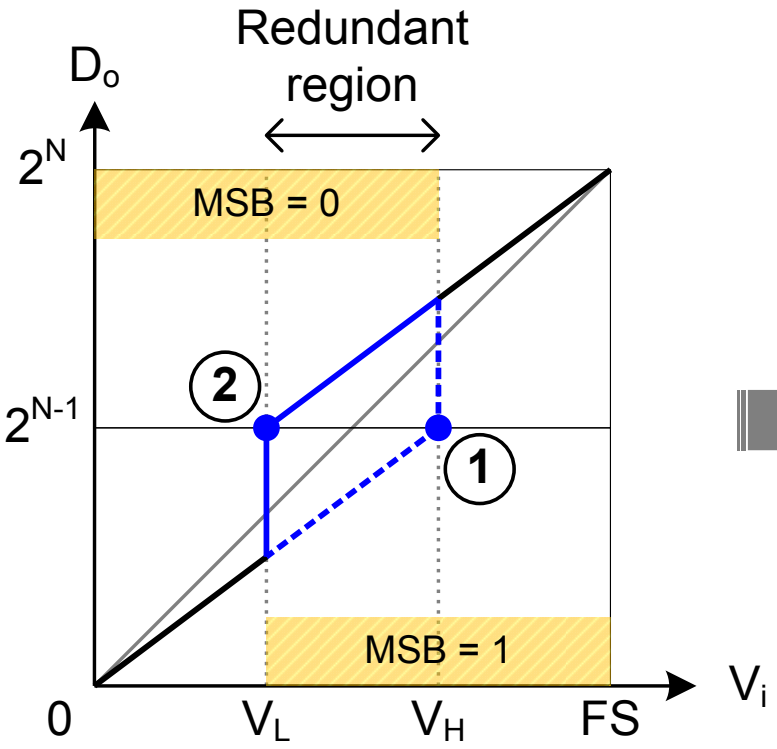
Sub-binary Redundancy (1)



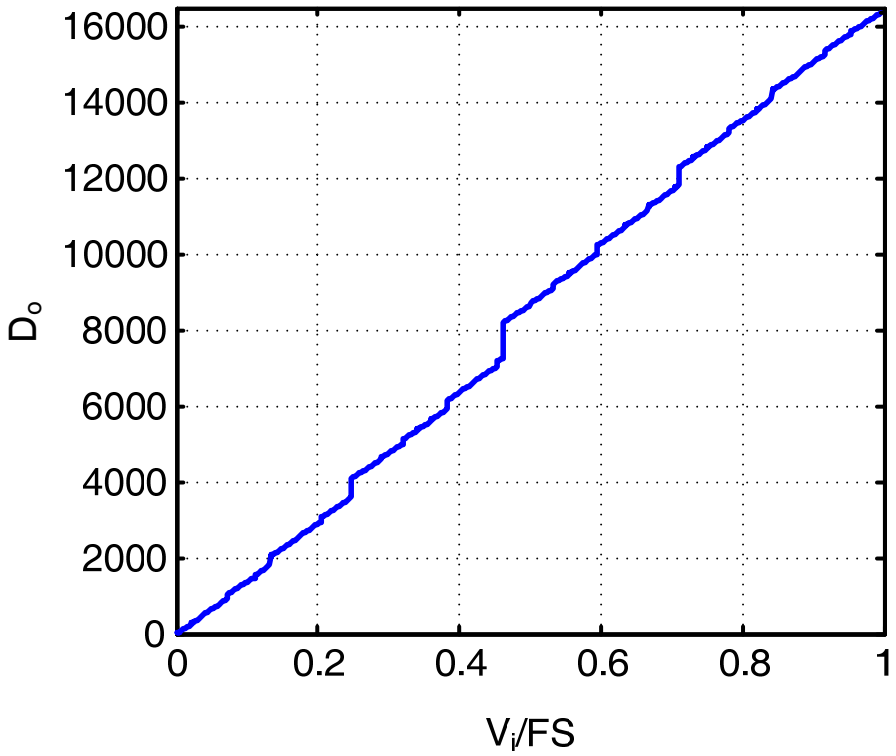
Super-binary | Binary | Sub-binary

- Sub-binary redundancy results in overlapped decision segments.
- Within the overlap, one analog input is mapped to two digital codes.

Sub-binary Redundancy (2)



N = 14



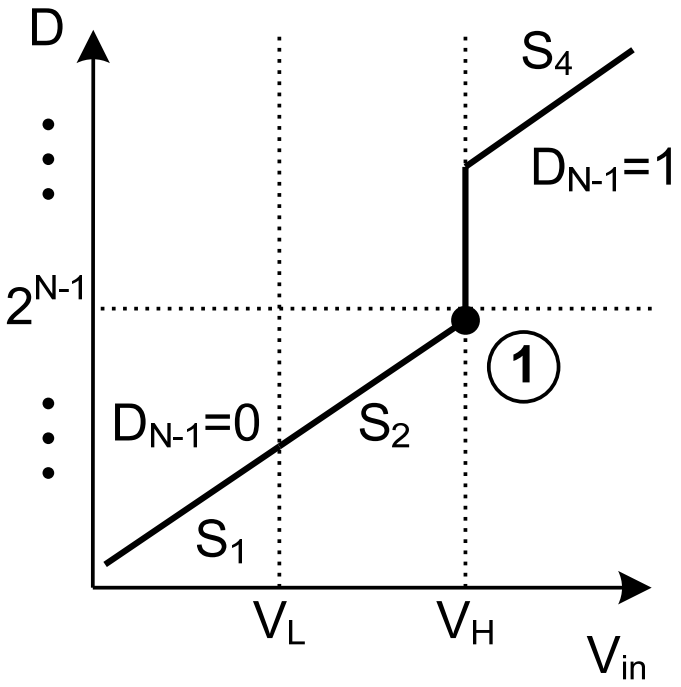
① = **011…1** → V_H

② = **100…0** → V_L

Note: only one transition edge shows up

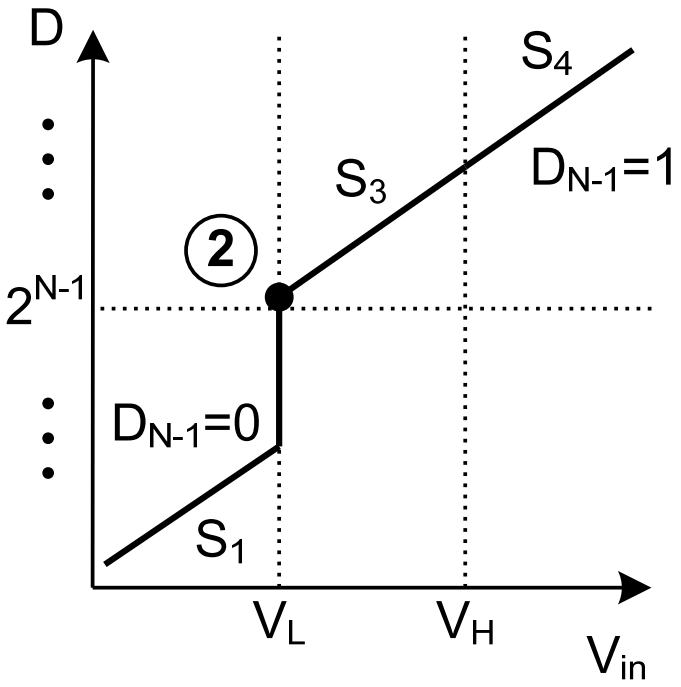
Exploiting Redundancy for Cal.

PN = 0

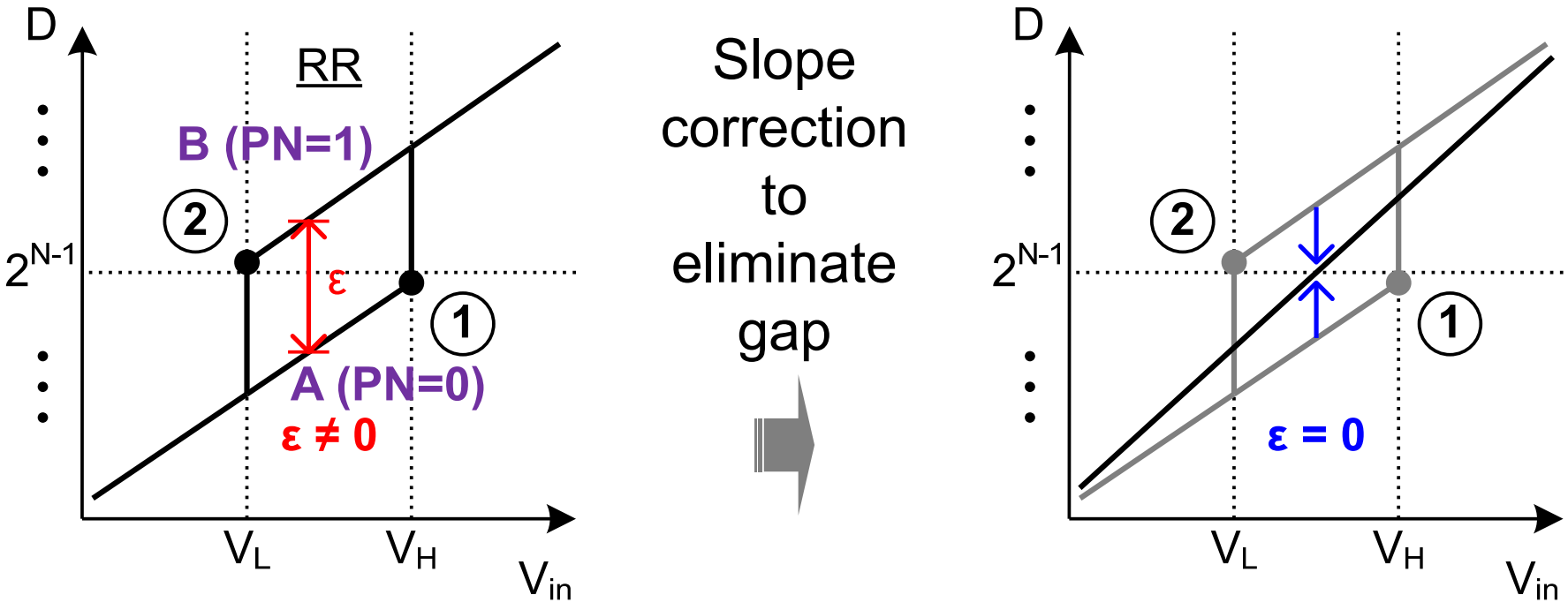


A B

PN = 1

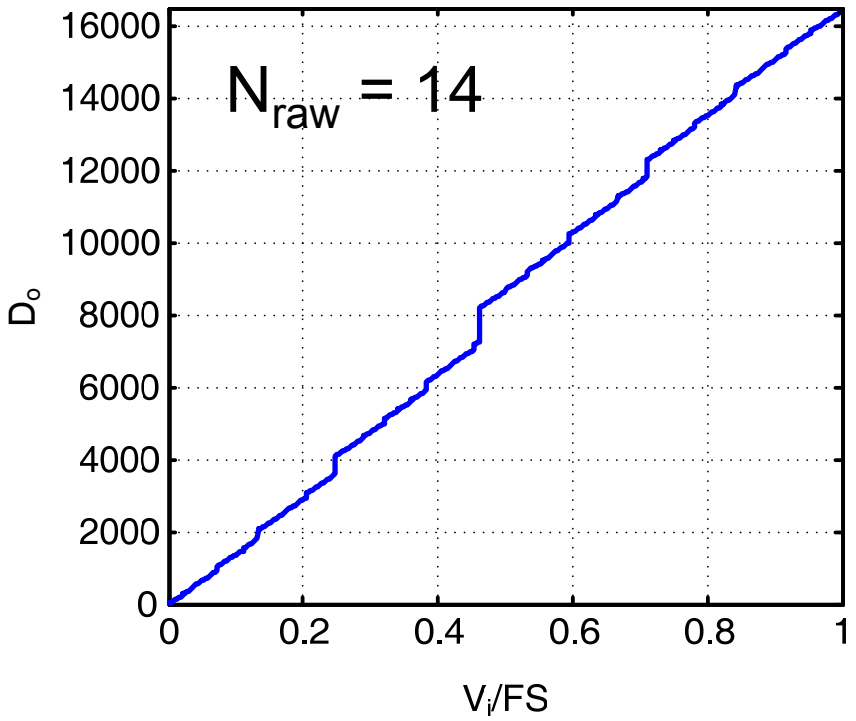


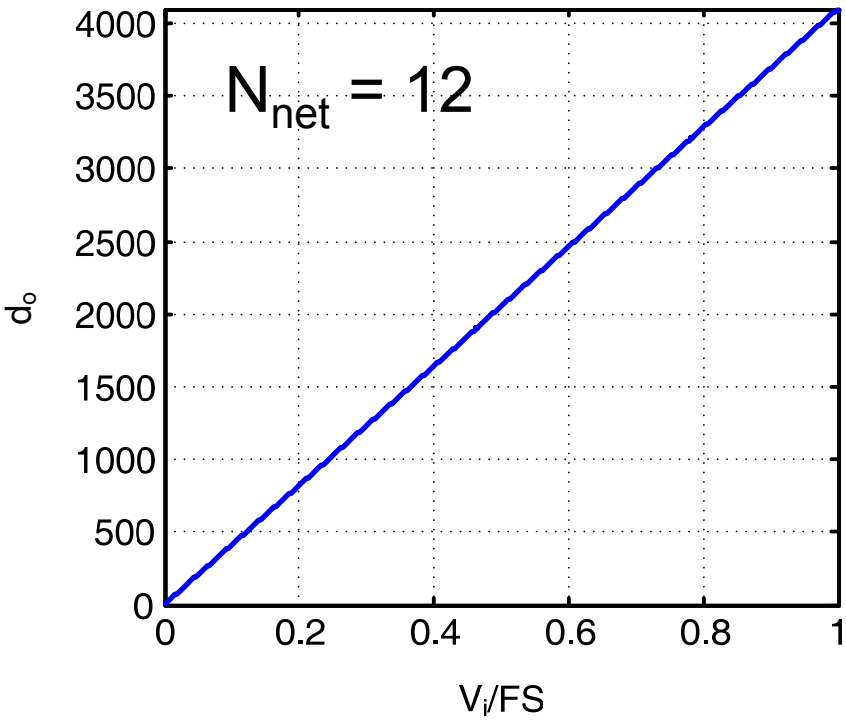
Exploiting Redundancy for Cal.



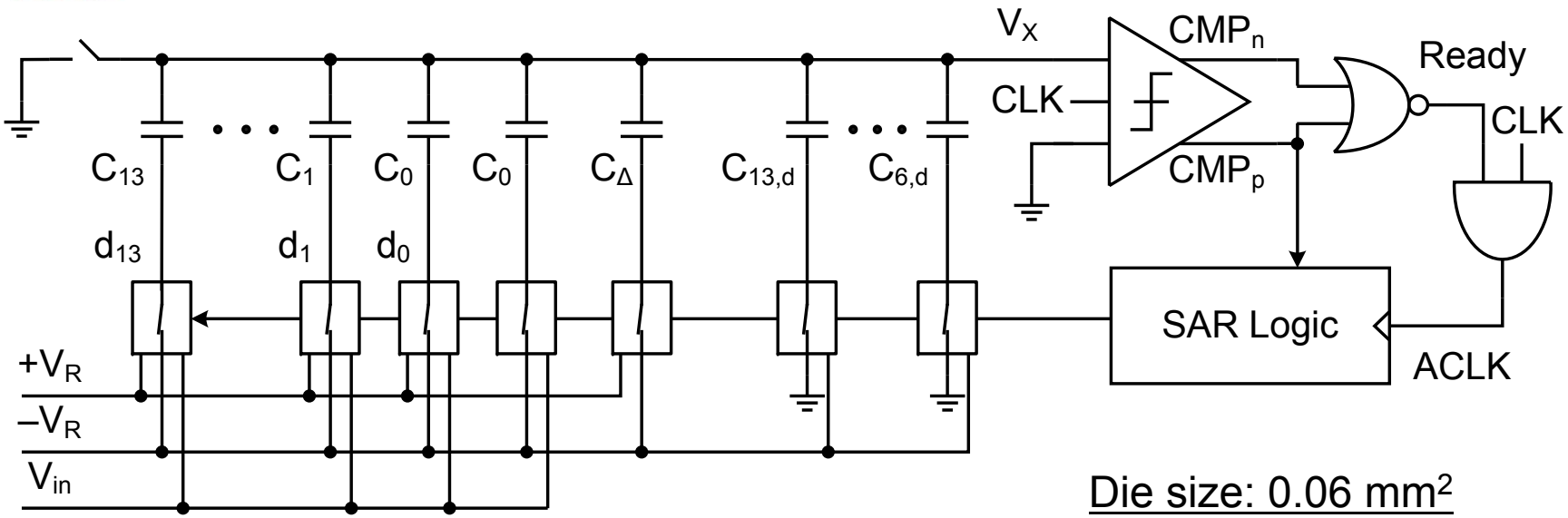
Digital Bit-Weight Calibration

$$d_o = \left\lfloor \frac{V_i}{V_{FS}} \right\rfloor = \sum_{j=0}^{N-1} w_j \cdot \left(2d_j - 1\right) \qquad \left\{w_j\right\} = \text{bit weights}$$

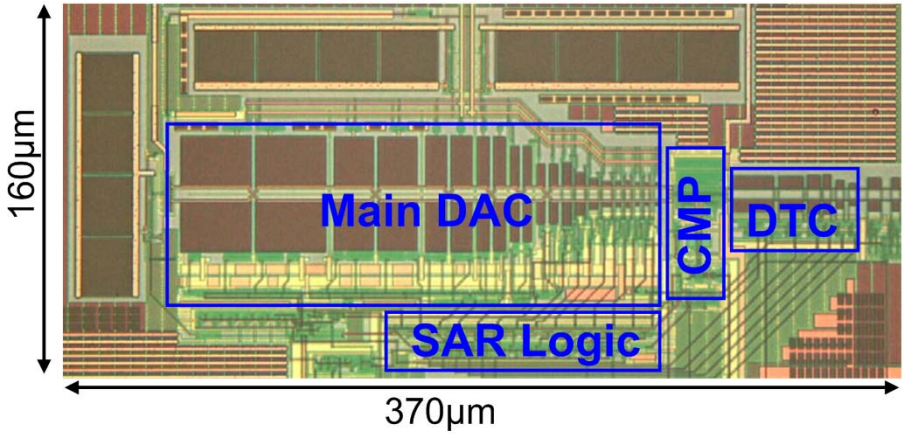




12-bit, 45-MS/s, 0.13-µm CMOS ADC

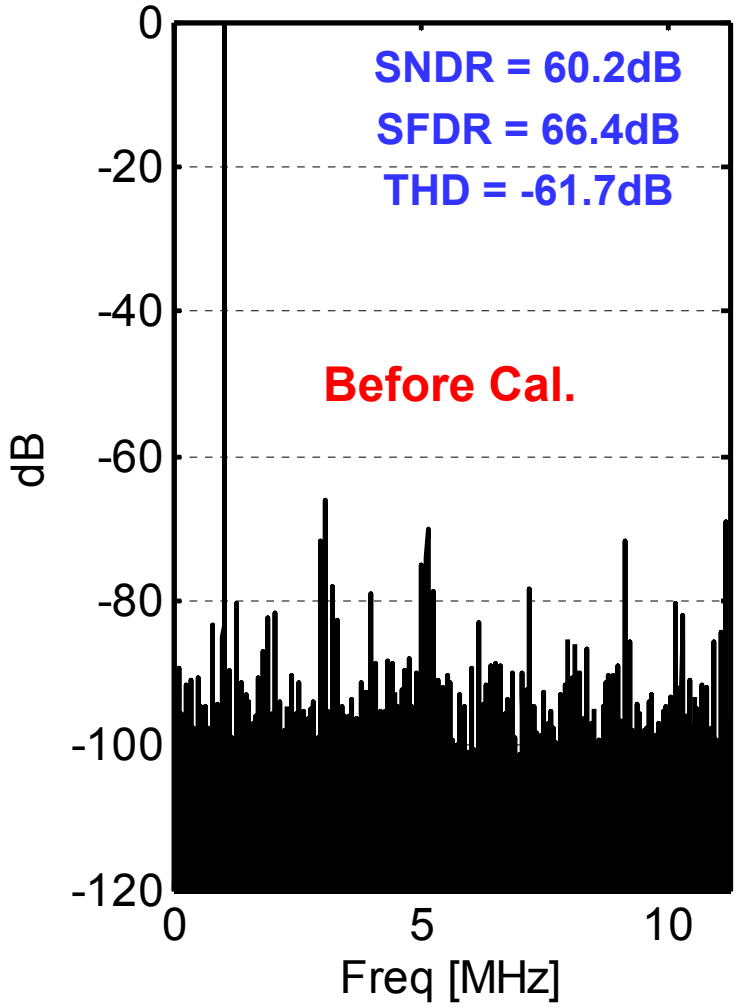


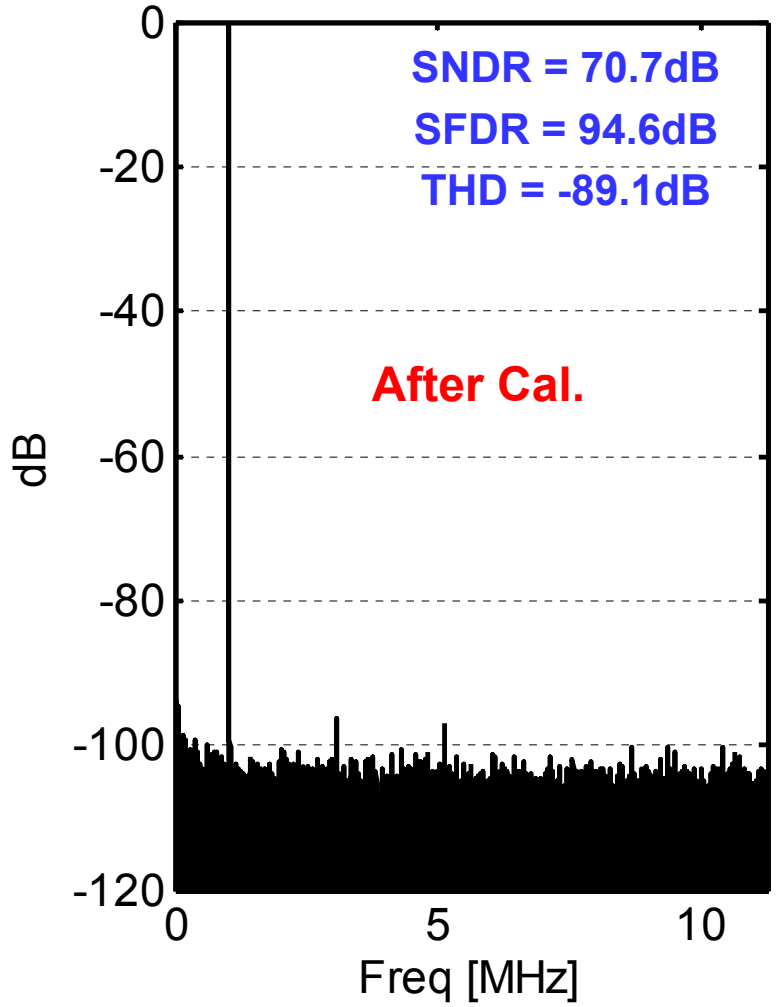
Die size: 0.06 mm²



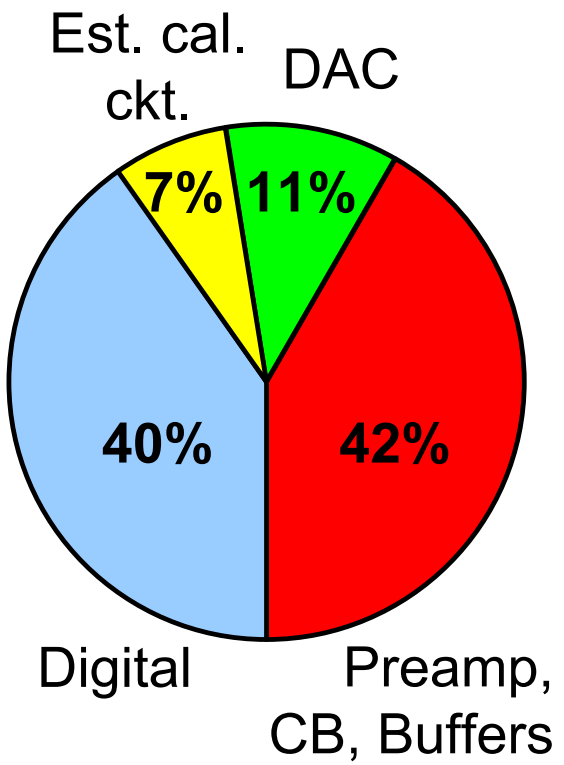
- 12 b, 45 MS/s in FG mode
- 3-mW power (36.3 fJ/step)
- **Most read JSSC article Nov. 2011**

Measured ADC Spectra (BG Mode)



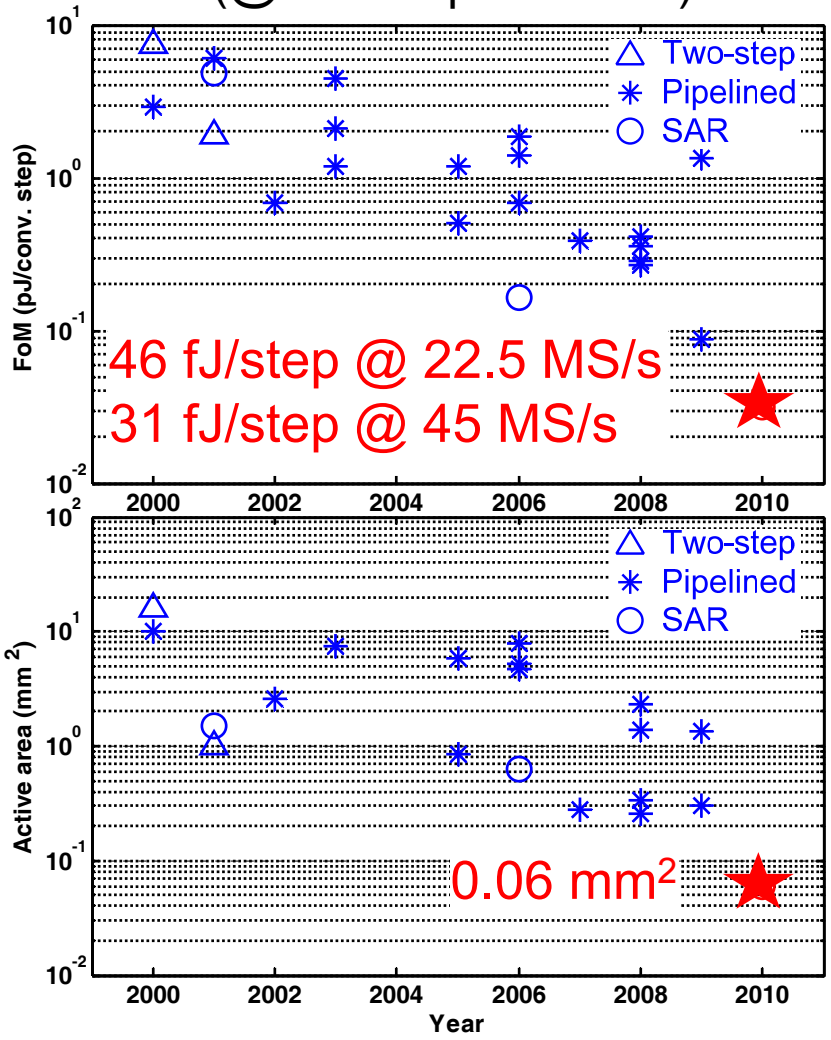


Comparison with 12-bit ADCs

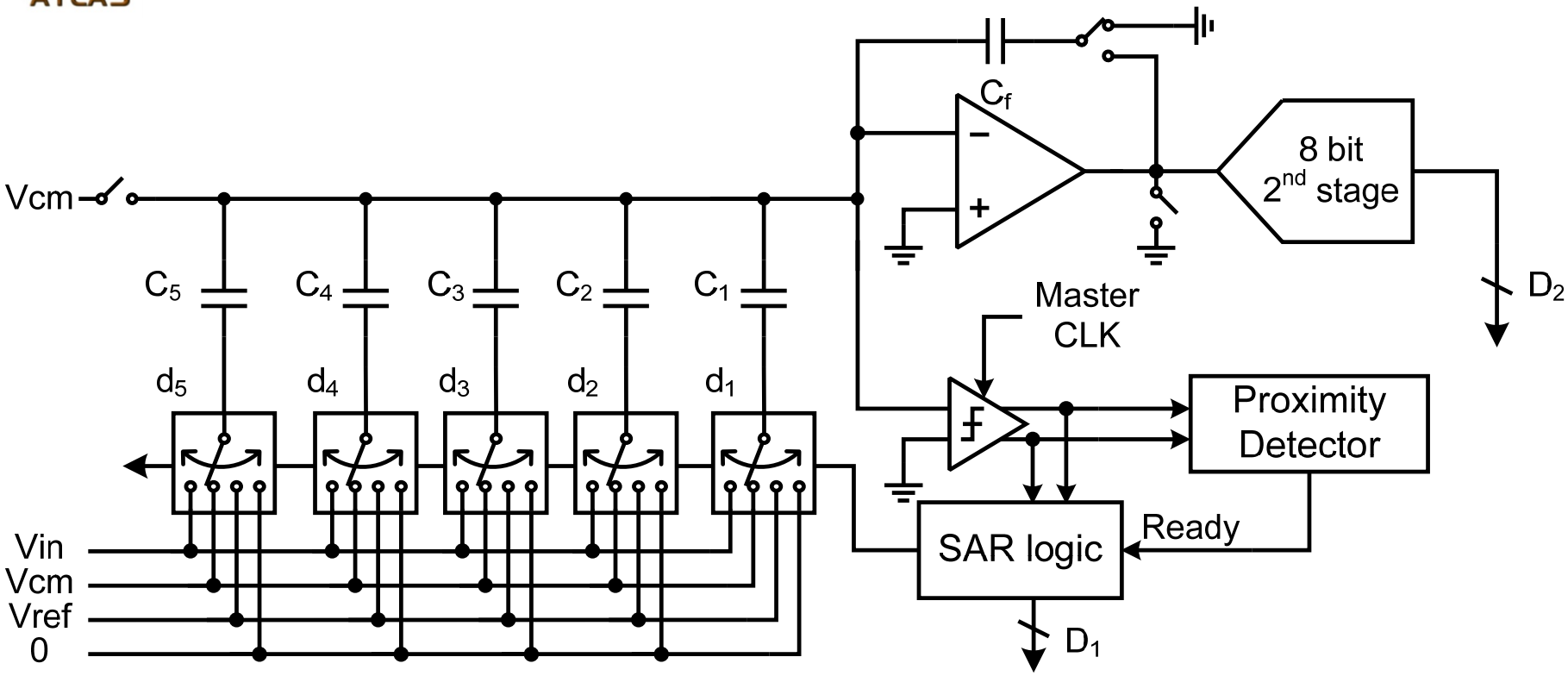


Total Power: 3.0 mW

(@ time of publication)

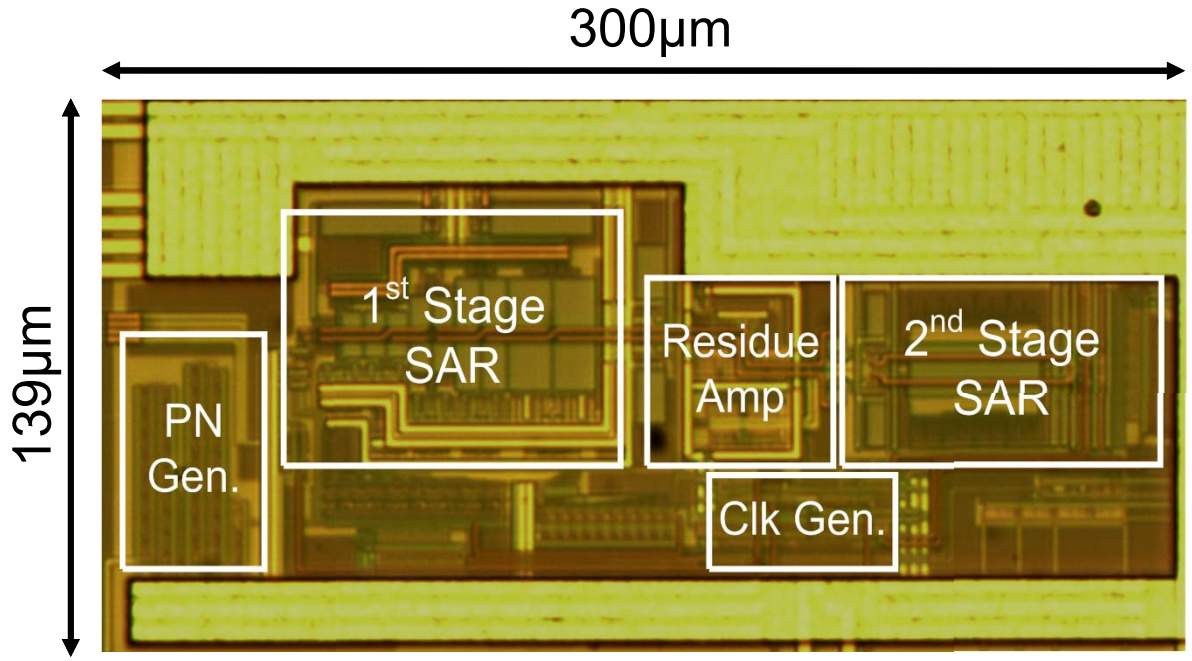


12-bit, 160-MS/s, 40-nm CMOS ADC



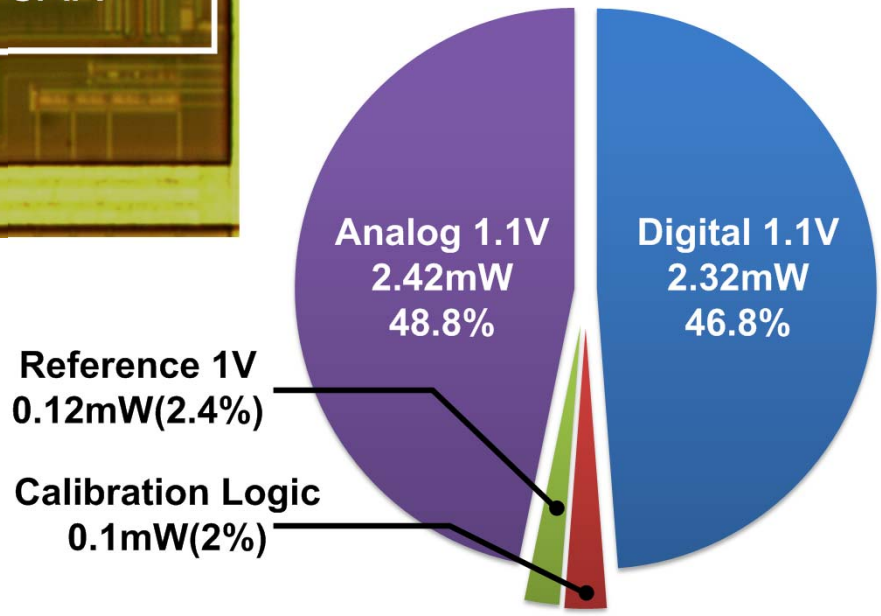
- (5b + 8b) synchronous two-step pipelined SAR architecture
- First-stage capacitor weights identified w/ opportunistic DAC dither

Die Photo and Power Breakdown



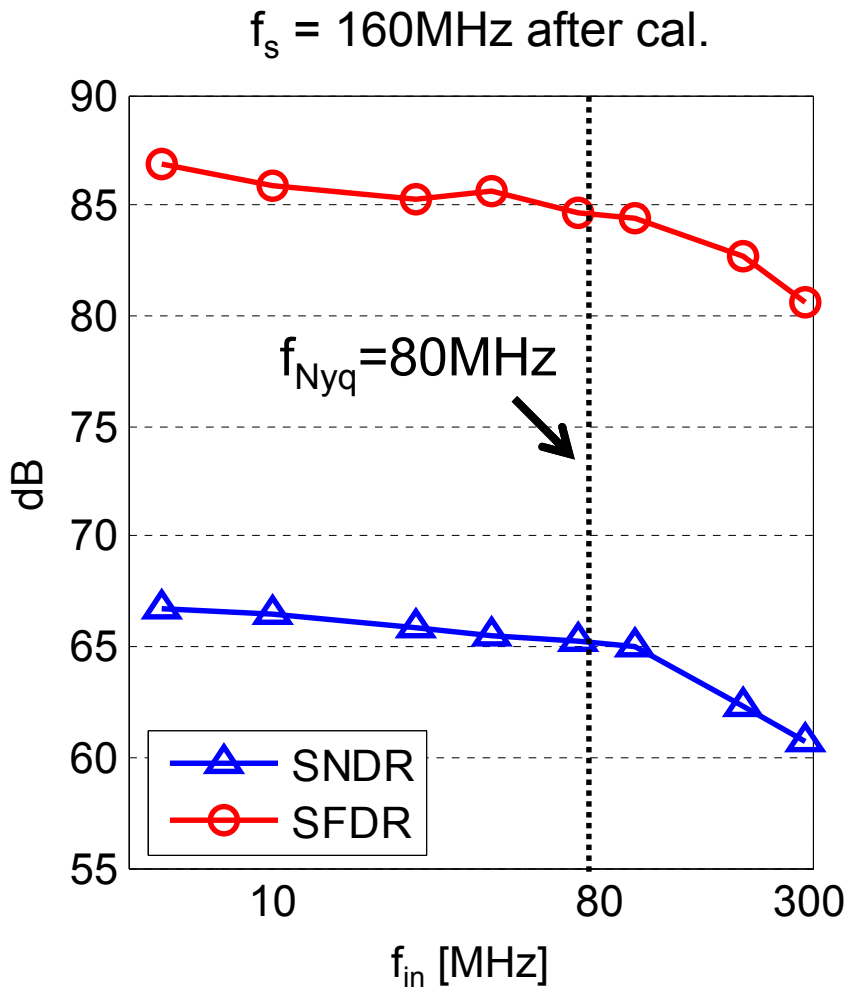
Die photo (0.042 mm²)

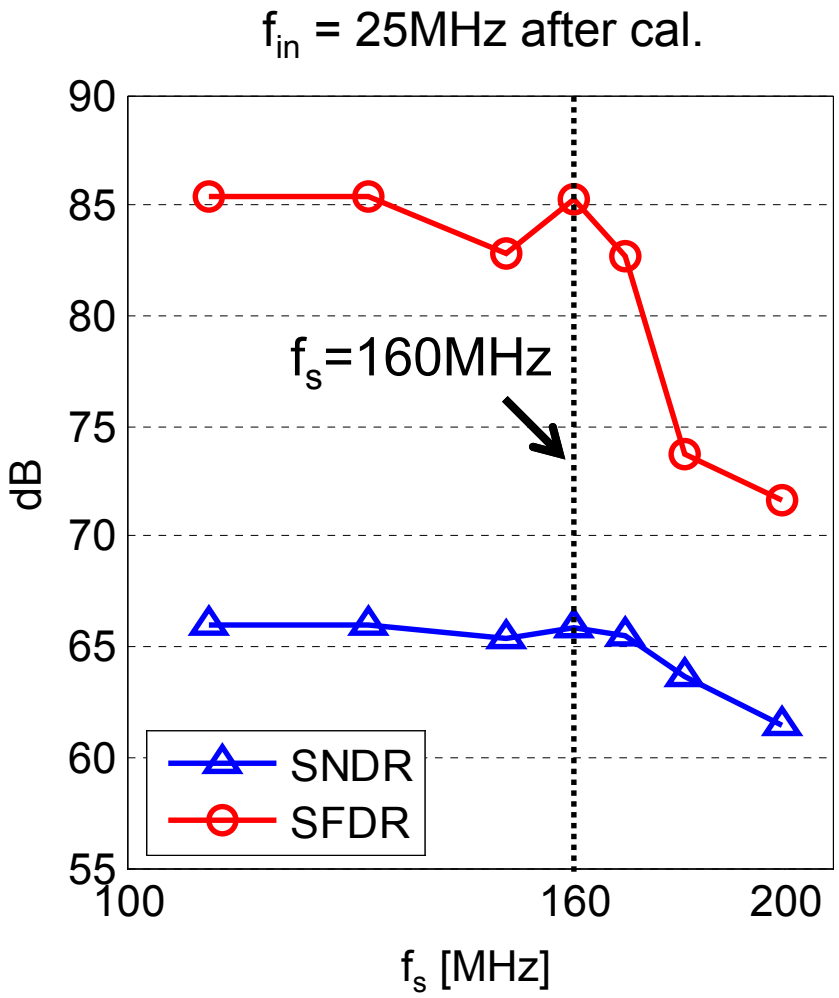
Power breakdown



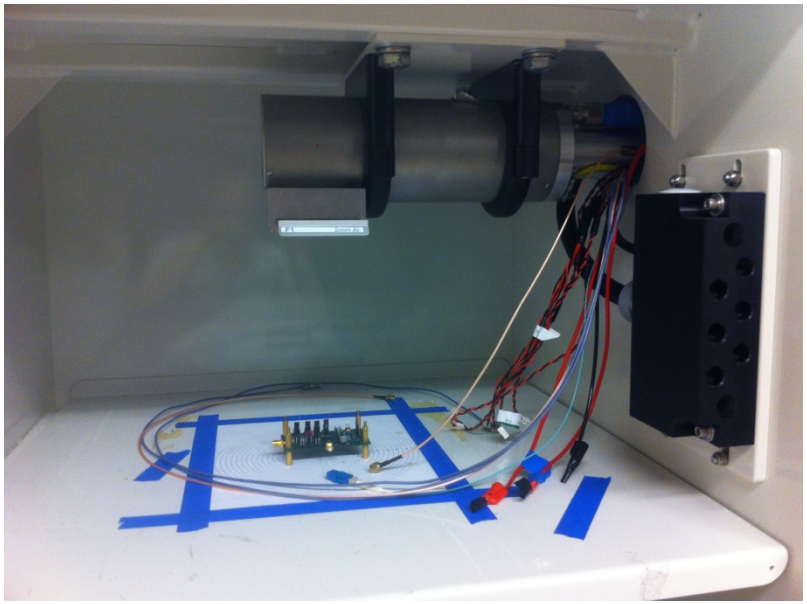
Total Power: 5.0 mW

Measured ADC Performance

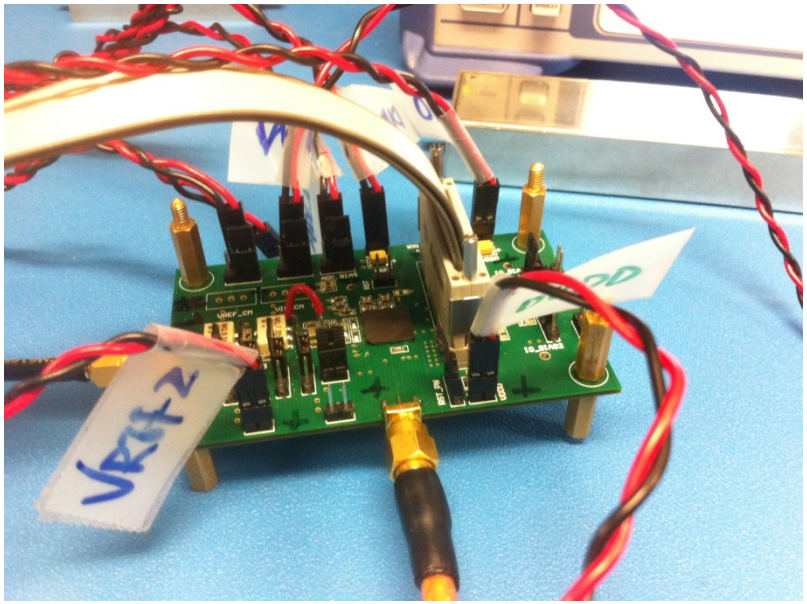




TID Test Setup



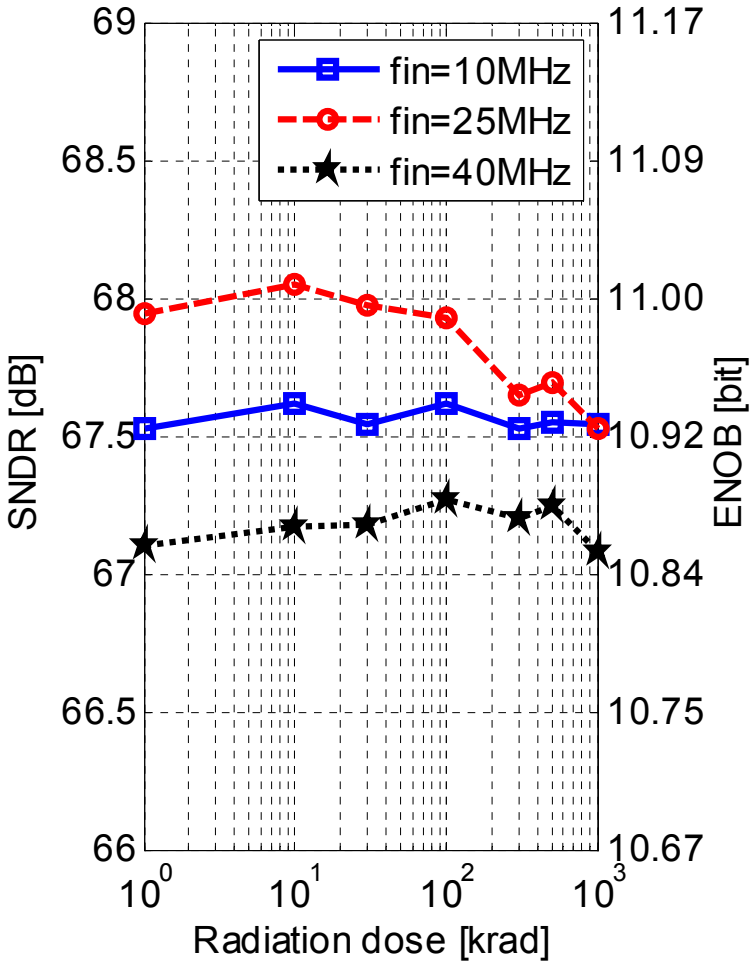
SMU TID setup

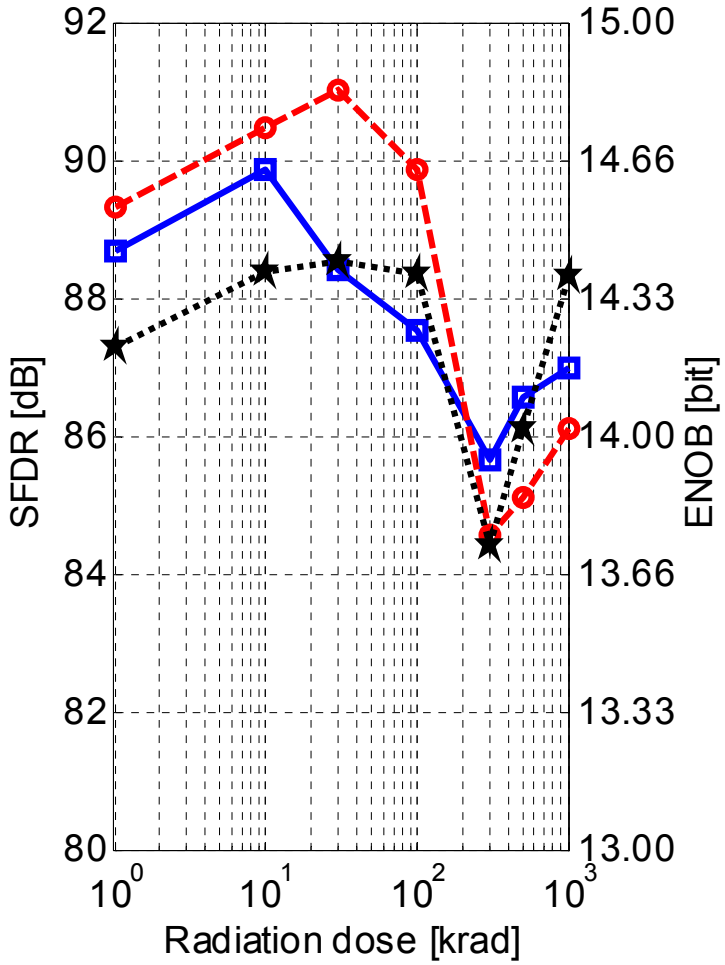


ADC test board

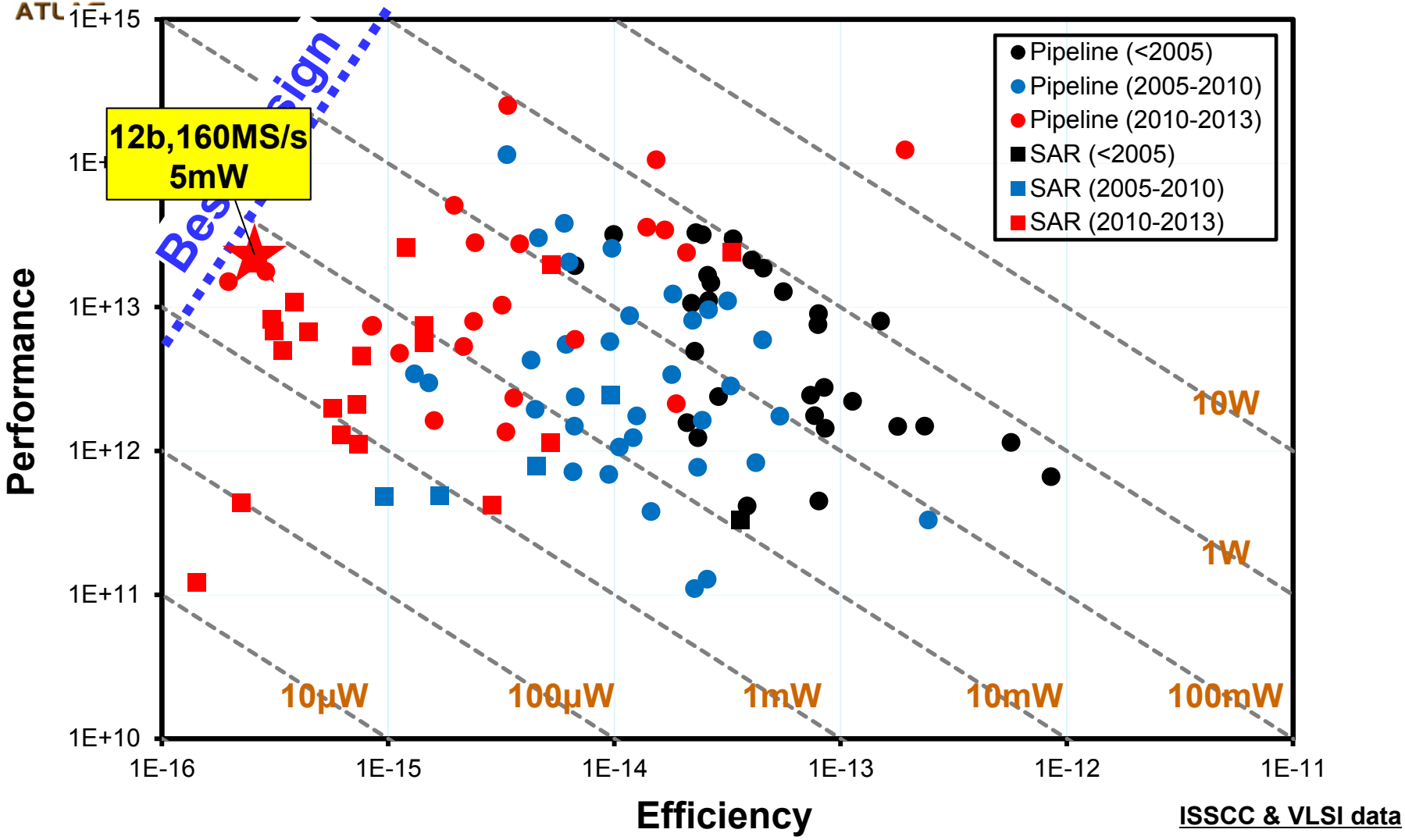
- DUT under X-ray radiation when powered up w/ clock input
- ADC performance (e.g., SNDR, SFDR, power, etc.) measured after irradiation

Measured SNDR/SFDR (80MS/s)





Performance Comparison

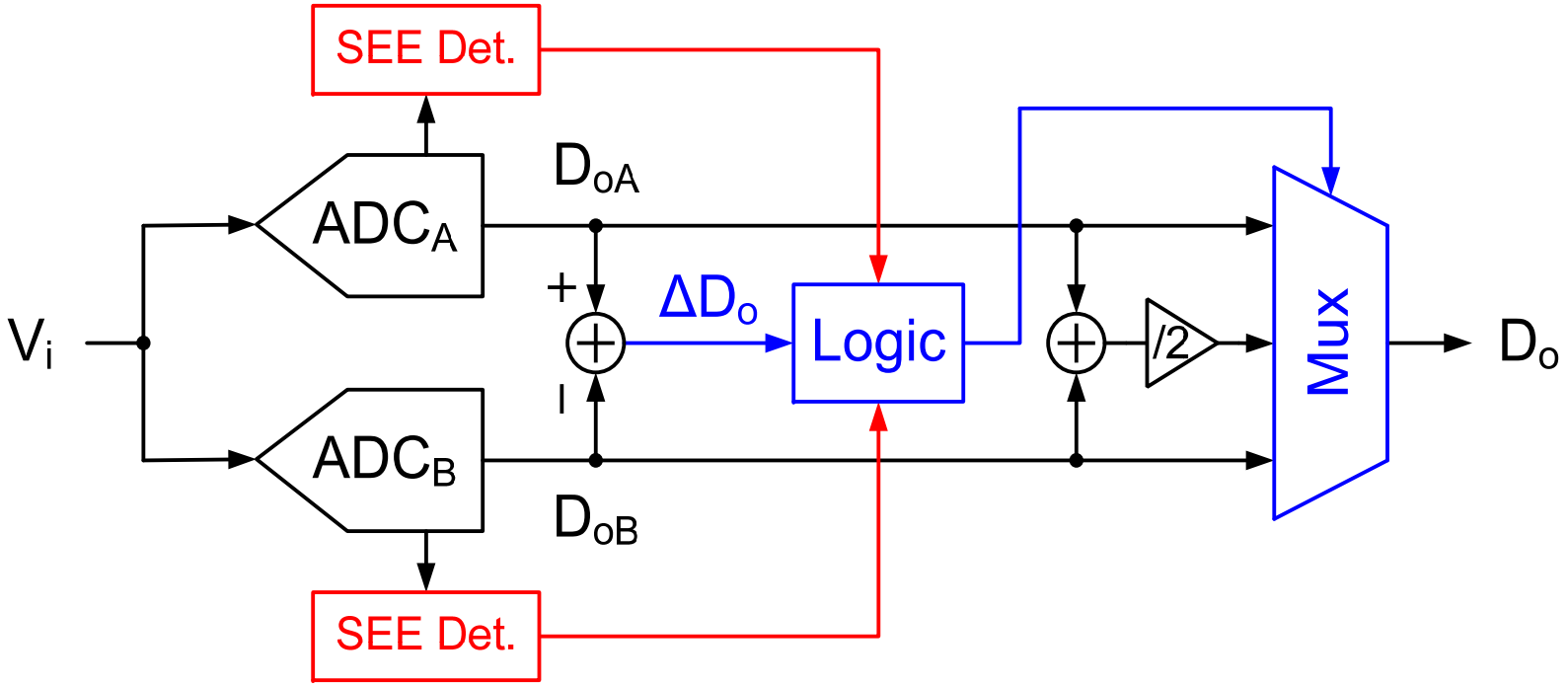


ISSCC & VLSI data

Current Design: 14b, 80MSPS

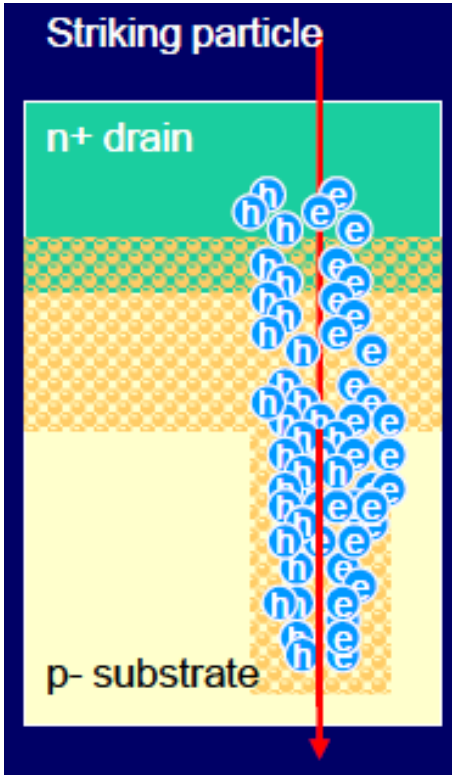
- Architecture: redundant 2-step SAR
- Digital circuits: protected with TMR
- Analog circuits (the focus of this work):
  - Sub-binary + inter-stage redundancy [1, 2]
  - Split-ADC (redundancy, calibration) [3]
  - Summing-node SEE detector (recently proposed → needs verification)

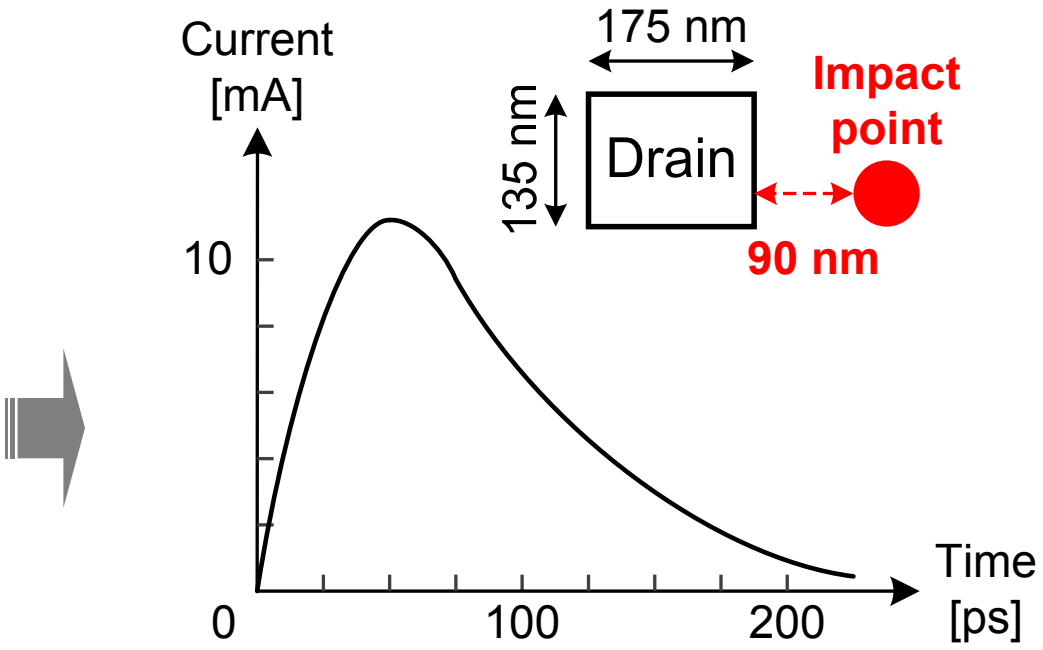
SEE – Split-ADC Redundancy



- If ΔD_o is large, chose the output of the ADC that is not hit.
- A 3-dB SNR gain with normal operation (i.e., no hit).
- Split-ADC also enables digital background calibration [3].

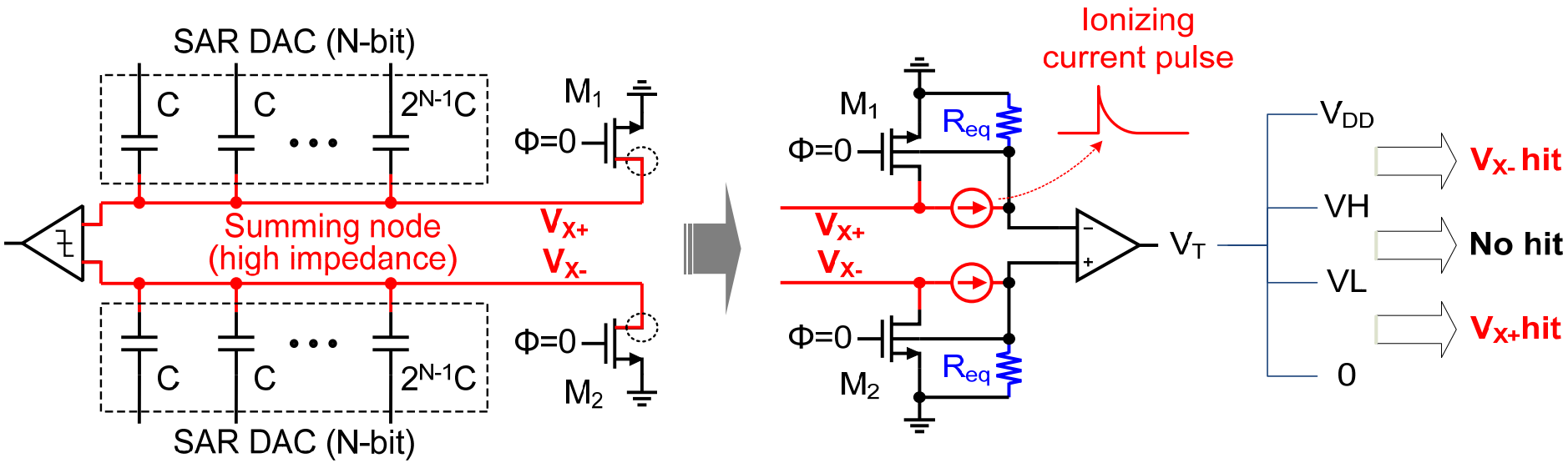
SEE – Modeling





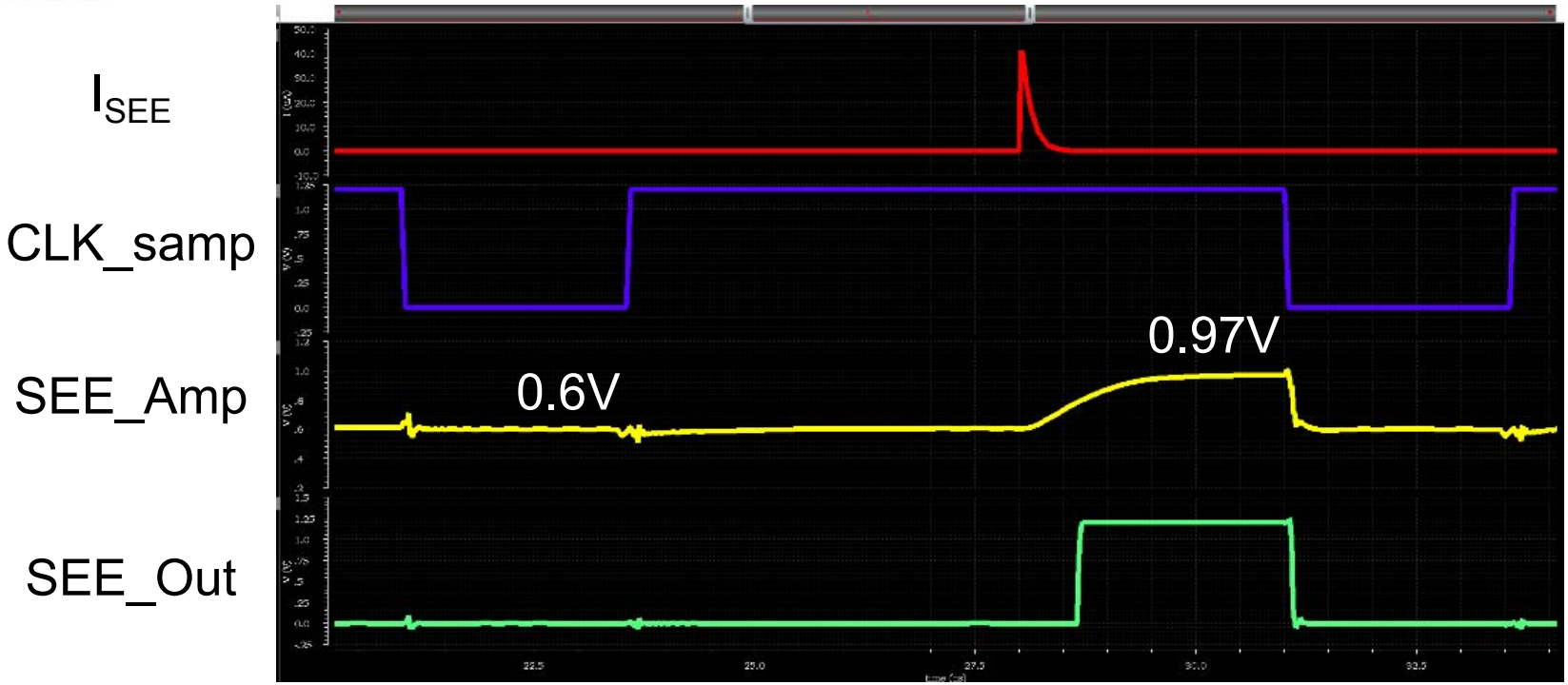
$$I(t) = \frac{Q_{tot}}{T_2 - T_1}\left(e^{-t/\tau_2} - e^{-t/\tau_1}\right) \quad [4]$$

SEE – Hit Detector



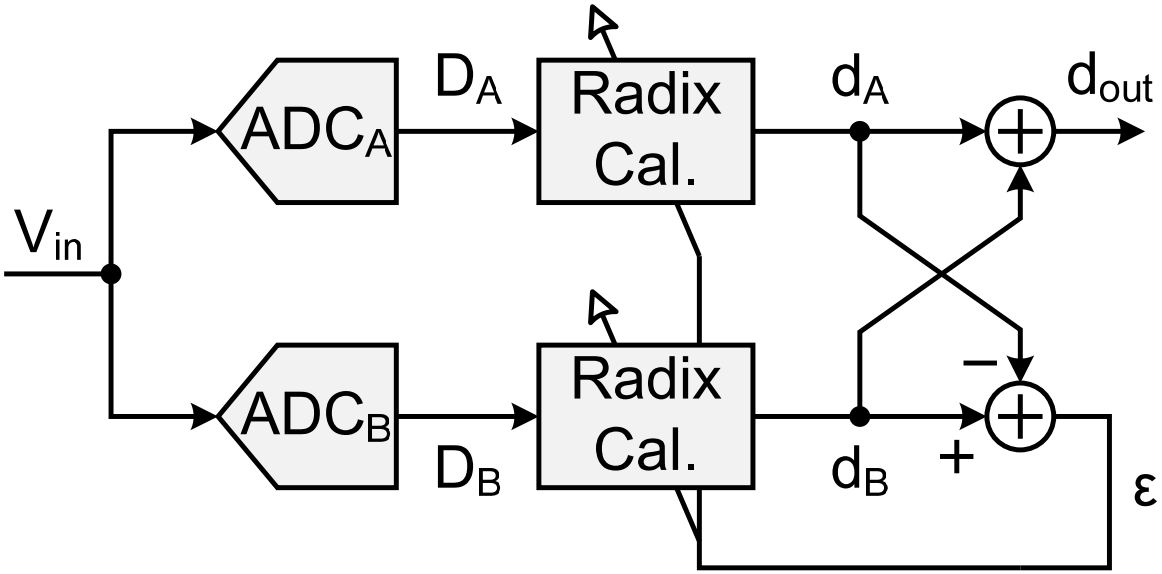
- For Q_{SEE} = 100fC and C_{TOT} = 2pF, V_{err} = 50mV ! [4]
- SEE detector is formed by a pair of resistors, a “substrate-current amplifier”, and some digital logic.

Preliminary Circuit Simulation



- The total charge collected due to SEE is set to 5.5fC, causing a 2.75mV voltage error on a 2pF DAC (~20 LSBs).
- The detector is reset during each sampling phase.

Split-ADC Calibration



$$d_A = \sum_i w_{A,i} \cdot D_{A,i}$$

$$d_B = \sum_i w_{B,i} \cdot D_{B,i}$$

LMS update:

$$w_{A,i}(n+1) = w_{A,i}(n) - \mu \cdot \varepsilon \cdot D_{A,i}$$

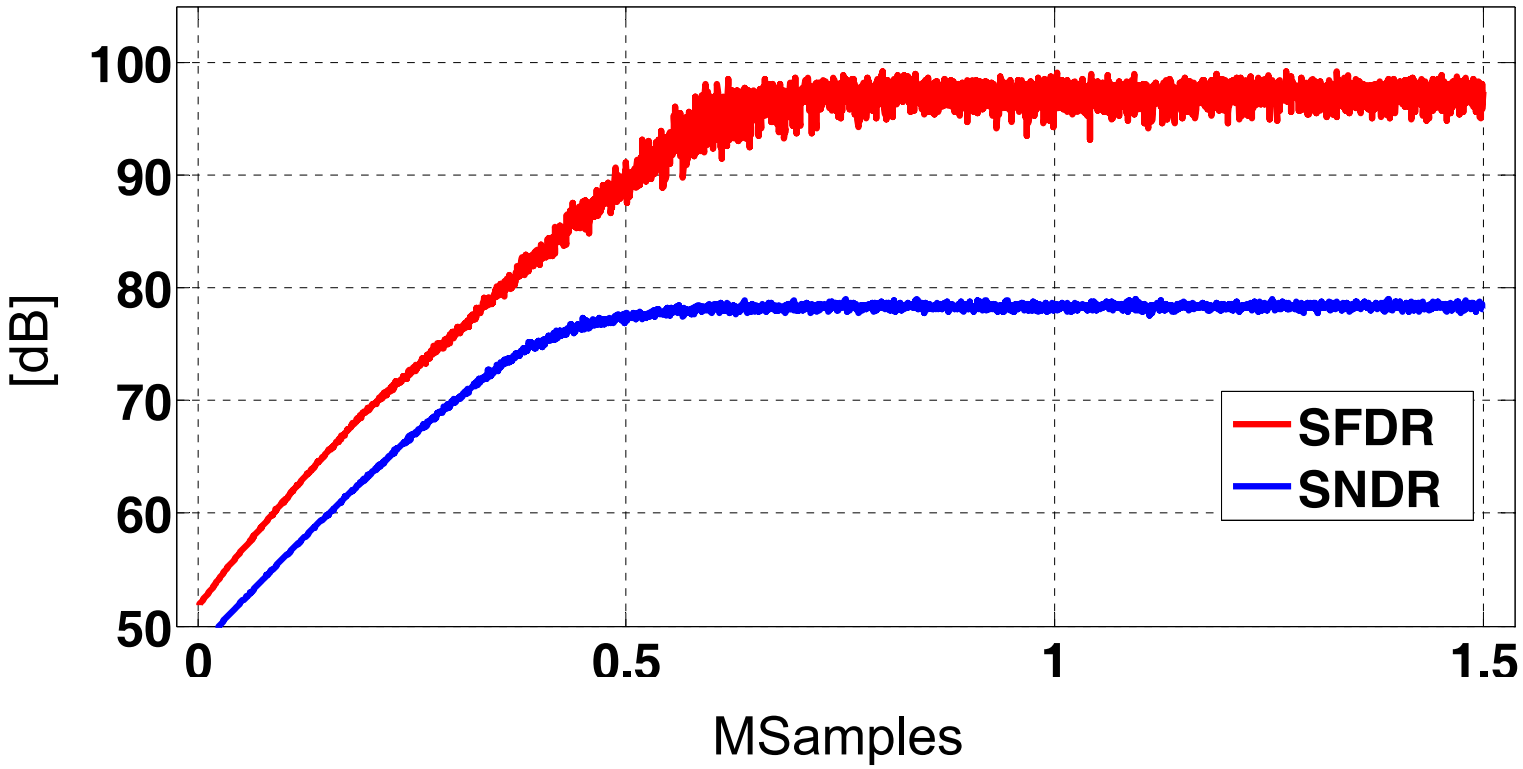
$$w_{B,i}(n+1) = w_{B,i}(n) + \mu \cdot \varepsilon \cdot D_{B,i}$$

[3]

Behavior Simulation Setup

Capacitor mismatch (1st stage, 2nd stage)	σ = 1%
1st stage Comparator offset (A)	16 mV
1st stage Comparator offset (B)	-18 mV
2nd stage Comparator offset (A)	7 mV
2nd stage Comparator offset (B)	-8 mV
1st stage Comparator noise (σ)	1 mV
2nd stage Comparator noise (σ)	0.5 mV
Amplifier output noise (σ)	1 mV
Sampling noise (C=2pF) (σ)	65 μV
Amplifier gain error	2%

Behavior Simulation Results



Calibration converges in < 1 million samples

Preliminary Circuit Sim. Results

Corner	SNDR (dB)	SFDR (dB)
TT	82.9	96.9
SS	83.2	95.2
FF	81.6	88.9
LV	82.5	97.6
HT	81.6	88.4
HVLT	84.3	99.8
TT w/ noise	76.4, single ADC 79.1, average	93.3, single ADC 95.3, average

LV/HV: power supply, reference, and common mode ×0.9/1.1

LT/HT: -40ºC/70ºC

Summary

- Features of low power and small die size make the SAR ADC a strong candidate for LAr readout Phase-II Upgrade of the ATLAS experiment.
- With preliminary TID results obtained, our future design will focus on SEE/SEU strategies for analog circuits.
- Architectural redundancy and digital calibration present a viable and efficient way to combat SEE and TID based on our studies.
- Expecting first prototype demonstration in Q2 of 2016.

Thank you for your attendance!

References

[1] Y. Zhou, B. Xu, and Y. Chiu, "A 12 bit 160 MS/s two-step SAR ADC with background bit-weight calibration using a time-domain proximity detector," *IEEE J. Solid-State Circuits*, vol. 50, pp. 920-931, Apr. 2015.

[2] W. Liu, P. Huang, and Y. Chiu, "A 12-bit, 45-MS/s, 3-mW redundant successive-approximation-register analog-to-digital converter with digital calibration," *IEEE J. Solid-State Circuits*, vol. 46, pp. 2661-2672, Nov. 2011.

[3] S. Sarkar, Y. Zhou, B. Elies, and Y. Chiu, "PN-assisted deterministic digital background calibration of multistage split-pipelined ADC," *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 62, pp. 654-661, Mar. 2015.

[4] D. G. Mavis and P. H. Eaton, "SEU and SET modeling and mitigation in deep submicron technologies," in *Proc. IEEE Int. Rel. Physics Symp.*, Apr. 2007, pp. 293-305.

