FRIB PLC Testing & Verification Process

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U.S. DEPARTMENT OF ENERGY | Office of Science

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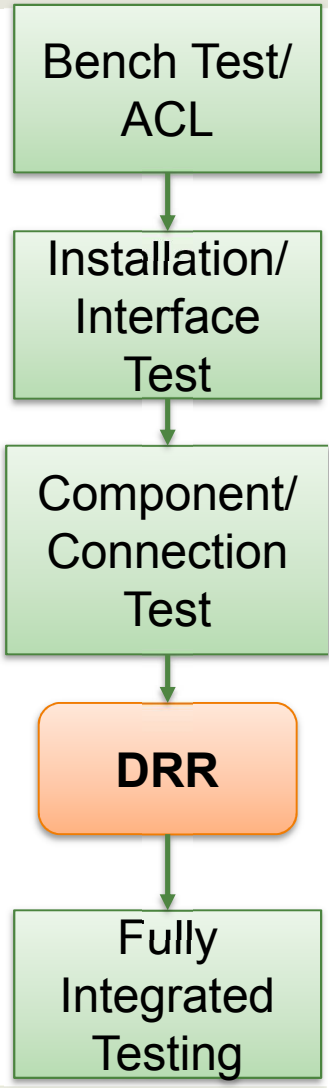
FRIB Controls Testing and Verification Process

- Hardware for major procurements tested with Bench Test Acceptance Criterial List (ACL) Testing
- Once PLC installation is complete, we perform several levels of testing
  - Installation tests
  - Interface tests
  - Component/Connection including Interlock Tests
  - Integration/Commissioning Tests include test with beam – Controls role is just support
  - Test records are filed with a number and title in our Document Control Center (DCC)
- Installation Test
  - Testing the PLC installation using traveler procedure/checklist system
- Interface Test
  - Test our outputs and inputs at the point of interface to hardware devices
  - Verify hardware devices have expected interface, i.e. Closed/open contact, 4-20 mA, etc
- Component/Connection Test
  - Connect to device hardware and verify I/O interface is working as expected, i.e. On/Off Control, readbacks, interlocks, limit status
  - Verify channels in control screens work as expected
  - Test Interlocks per Interlock and Alarm Document
- Device Readiness Review (DRR) reviews that testing and documentation completed, as well as safety and operational concerns before final integrated testing is performed

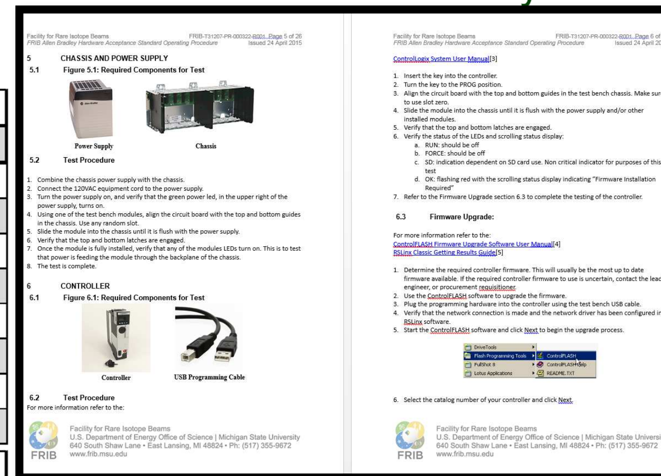


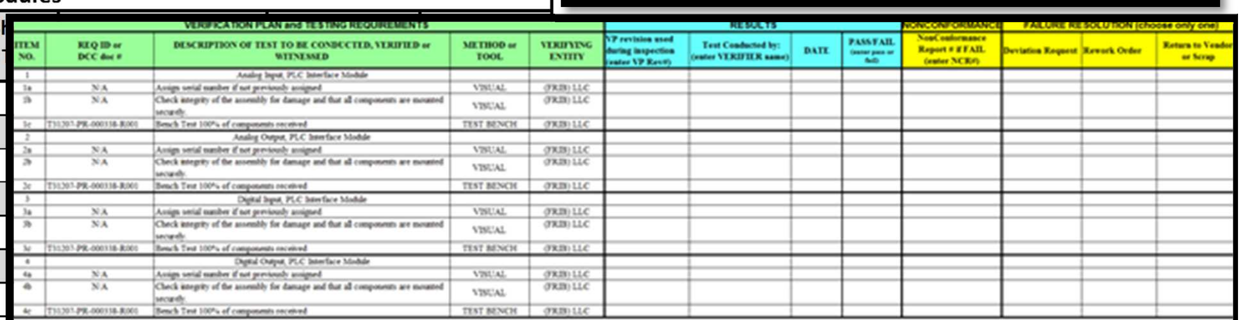
Acceptance Testing Plans Developed for PLC Hardware

- New hardware tested against ACL verification plan
- The Standard Operating Procedure is referenced by ACL plan and details how the ACL inspections are to be carried out
- The results of the tests are recorded in a separate tab of the ACL verification report document
- The results summary for the lot of modules is entered into the ACL Results section by the verifier and filed into our DCC system

Controllers						
Serial Number	RUN LED	FORCE LED	OK LED	Scrolling Status Display	Tested By	Date
	☐ Off	☐ Off	☐ Flashing red	☐ Firmware Installation Required		
	☐ Off	☐ Off	☐ Flashing red	☐ Firmware Installation Required		
	☐ Off	☐ Off	☐ Flashing red	☐ Firmware Installation Required		
	☐ Off	☐ Off	☐ Flashing red	☐ Firmware Installation Required		
	☐ Off	☐ Off	☐ Flashing red	☐ Firmware Installation Required		
	☐ Off	☐ Off	☐ Flashing red	☐ Firmware Installation Required		
	☐ Off	☐ Off	☐ Flashing red	☐ Firmware Installation Required		
	☐ Off	☐ Off	☐ Flashing red	☐ Firmware Installation Required		

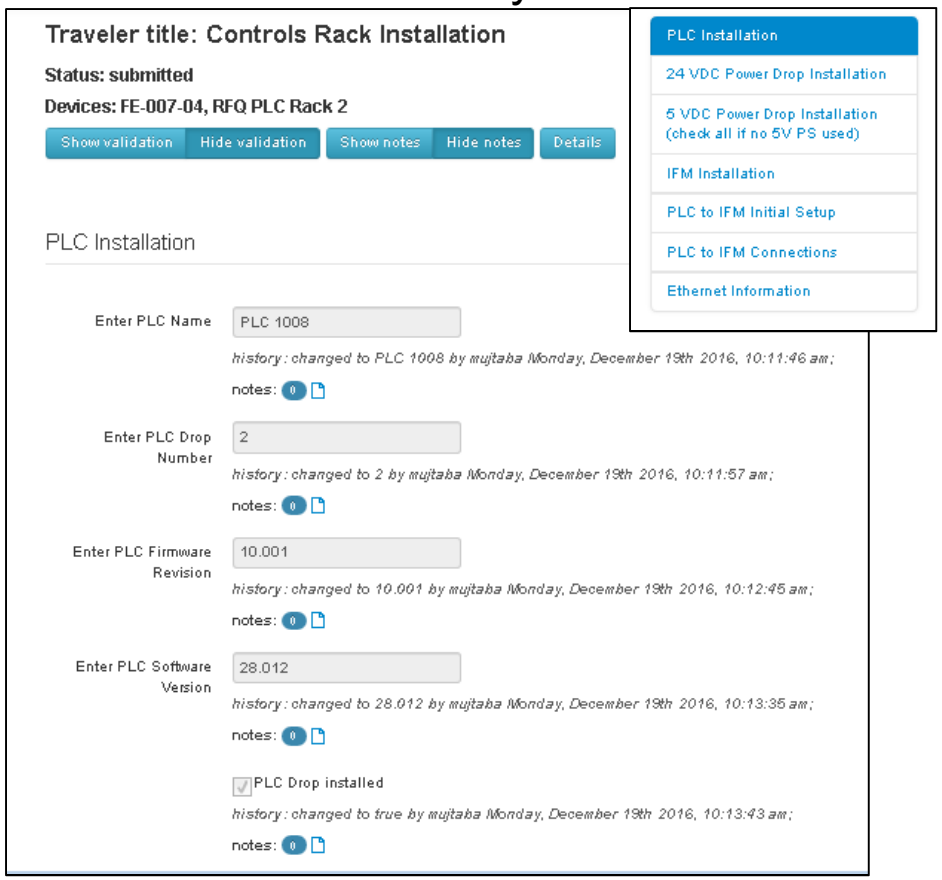
1756 Ethernet Modules				
Serial Number	LEDs			Alphanumeric Display Sh
	OK	LINK	NET	TEST, PASS, OK, REV x.x,
	☐ Flashing green	☐ Off	☐ Off	☐ OK, IP address
	☐ Flashing green	☐ Off	☐ Off	☐ OK, IP address
	☐ Flashing green	☐ Off	☐ Off	☐ OK, IP address
	☐ Flashing green	☐ Off	☐ Off	☐ OK, IP address
	☐ Flashing green	☐ Off	☐ Off	☐ OK, IP address
	☐ Flashing green	☐ Off	☐ Off	☐ OK, IP address
	☐ Flashing green	☐ Off	☐ Off	☐ OK, IP address

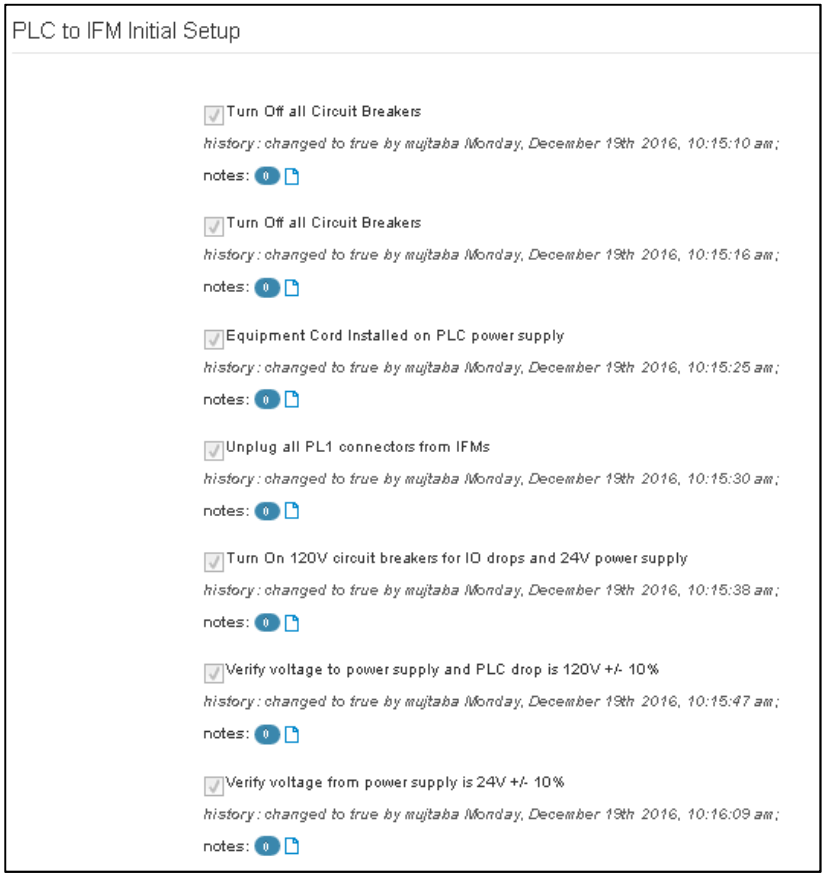




FRIB Controls Installation/Interface Tests

- Installation testing uses online traveler system or spreadsheet
  - Combination of procedure and checklist
  - Tracks user & history





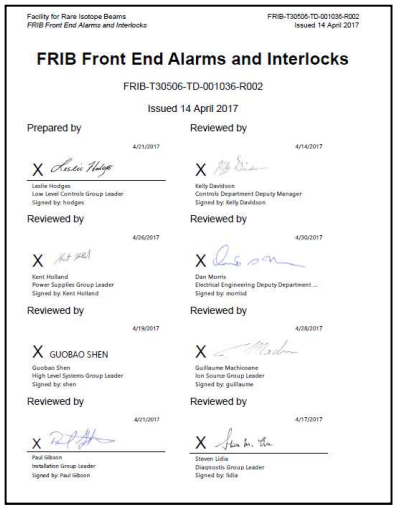
FRIB Controls Component/Connection Tests[1]

- Component/Connection testing is tracked in spreadsheet and filed in DCC
  - Testing verified installation/interface wiring and control connections through control screens
  - Tracked by each hardwired I/O point and filed in Document Control Center

				Controls Rack	Rack Termination Complete	Device Location	Device Termination Complete	Cable Number	Installation Test Result	Tested On	Tested By	Component Test Result	Tested On	Tested By	Representative	Notes
	Slot 1	4	FE_LEBT:IP_D0912:OK_RSTS	FE-001.03	YES	FE-001.02	YES		PASS	7/20/2017	LH	PASS	5/16/2017	LH	AW	
		5	FE_LEBT:IP_D0977:OK_RSTS	FE-001.03	YES	FE-001.02	YES		PASS	7/20/2017	LH	PASS	5/16/2017	LH	AW	
		6	FE_MEBT:IP_D1053:OK_RSTS	FE-001.03	YES	FE-001.01	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		7	FE_MEBT:IP_D1066:OK_RSTS	FE-001.03	YES	FE-001.01	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		8	FE_MEBT:IP_D1070:OK_RSTS	FE-001.03	YES	FE-001.01	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		9	FE_MEBT:IP_D1092:OK_RSTS	FE-001.03	YES	FE-001.01	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		10	FE_MEBT:IP_D1102:OK_RSTS	FE-001.03	YES	FE-001.01	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		11	FE_MEBT:IP_D1109:OK_RSTS	FE-001.03	YES	FE-001.01	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		12	FE_MEBT:IP_D1121:OK_RSTS	FE-001.03	YES	FE-001.01	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		13	FE_BTS:IP_D1098:OK_RSTS	FE-001.03	YES	FE-001.01	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		14	RFQ VAC STATUS TO FE	FE-001.03	YES	FE-007.04	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		15		FE-001.03												
	Slot 2		DIGITAL OUTPUT	FE-001.03												
	Slot 2	0	FE_LEBT:NEGP_D0955:ON_RCMD	FE-001.03	YES	FE-001.02	YES		PASS			PASS				
		1	FE_LEBT:NEGP_D0987:ON_RCMD	FE-001.03	YES	FE-001.02	YES		PASS			PASS				
		2	FE_LEBT:TMP_D0833:ON_RCMD	FE-001.03	YES	FE-001.02	YES		PASS	8/24/2017	LH	PASS	5/16/2017	LH	AW	
		3	FE_LEBT:TMP_D0833:SFTS_RCMD	FE-001.03	YES	FE-001.02	YES	84F000053	PASS	8/24/2017	LH	PASS	5/16/2017	LH	AW	
		4	FE_LEBT:IP_D0912:ON_RCMD	FE-001.03	YES	FE-001.02	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		5	FE_LEBT:IP_D0977:ON_RCMD	FE-001.03	YES	FE-001.02	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		6	FE_MEBT:IP_D1053:ON_RCMD	FE-001.03	YES	FE-001.01	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		7	FE_MEBT:IP_D1066:ON_RCMD	FE-001.03	YES	FE-001.01	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		8	FE_MEBT:IP_D1070:ON_RCMD	FE-001.03	YES	FE-001.01	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		9	FE_MEBT:IP_D1092:ON_RCMD	FE-001.03	YES	FE-001.01	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		10	FE_MEBT:IP_D1102:ON_RCMD	FE-001.03	YES	FE-001.01	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		11	FE_MEBT:IP_D1109:ON_RCMD	FE-001.03	YES	FE-001.01	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		12	FE_MEBT:IP_D1121:ON_RCMD	FE-001.03	YES	FE-001.01	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		13	FE_BTS:IP_D1098:ON_RCMD	FE-001.03	YES	FE-001.01	YES		PASS	7/20/2017	LH	PASS	7/24/2017	LH	AW	
		14	FE VAC STATUS TO RFQ	FE-001.03												
		15		FE-001.03												
	Slot 3		DIGITAL INPUT	FE-001.03												
	Slot 3	0	FE_SC51:PG_D0707:OK_RSTS_VP	FE-001.03	YES	FE-001.02	YES		PASS	3/9/2017	LH	PASS	3/20/2017	LH	PG	
		1	FE_SC51:RPG_D0707:OK_RSTS_VP	FE-001.03	YES	FE-001.02	YES		PASS	3/9/2017	LH	PASS	3/20/2017	LH	PG	
		2	FE_SC51:CCG_D0707:OK_RSTS_VP	FE-001.03	YES	FE-001.02	YES		PASS	3/9/2017	LH	PASS	3/17/2017	LH	PG	
		3	FE_LEBT:CCG_D0795:OK_RSTS_VP	FE-001.03	YES	FE-001.02	YES	84F000002	PASS	3/9/2017	LH					
		4	FE_SC51:RPG_D0717:OK_RSTS_VP	FE-001.03	YES	FE-001.02	YES		PASS	3/9/2017	LH	PASS	3/20/2017	LH	PG	
		5	FE_SC52:RPG_D0701:OK_RSTS_VP	FE-001.03	YES	FE-001.02	YES		PASS	3/9/2017	LH					
		6	FE_SC51:CCG_D0717:OK_RSTS_VP	FE-001.03	YES	FE-001.02	YES		PASS	3/9/2017	LH					
		7	FE_SC52:CCG_D0701:OK_RSTS_VP	FE-001.03	YES	FE-001.02	YES	84F000003	PASS	3/9/2017	LH					
		8	FE_SC51:PG_D0739:OK_RSTS_VP	FE-001.03	YES	FE-001.02	YES		PASS	3/9/2017	LH	PASS	3/20/2017	LH	PG	
		9	FE_SC51:RPG_D0739:OK_RSTS_VP	FE-001.03	YES	FE-001.02	YES		PASS	3/9/2017	LH	PASS	3/20/2017	LH	PG	
		10	FE_SC51:CCG_D0739:OK_RSTS_VP	FE-001.03	YES	FE-001.02	YES		PASS	3/9/2017	LH	PASS	3/17/2017	LH	PG	
		11	FE_LEBT:CCG_D0814:OK_RSTS_VP	FE-001.03	YES	FE-001.02	YES	84F000004	PASS	3/9/2017	LH					

FRIB Controls Component/Connection Tests[2]

- Checklists for component/connection test filed in DCC
  - Alarms and Interlocks documented and signed off in DCC
  - Interlocks tested per area's Alarm and Interlocks document and results filed in Document Control Center



Facility for Rare Isotope Beams
FRIB Front End Alarms and Interlocks
FRIB-T30506-TD-001036-R002
Issued 14 April 2017

FRIB Front End Alarms and Interlocks

FRIB-T30506-TD-001036-R002

Issued 14 April 2017

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Reviewed by — Dan Morris, Electrical Engineering Deputy Department, 4/30/2017
Reviewed by — GUOBAO SHEN, High Level Systems Group Leader, 4/19/2017
Reviewed by — Guillaume Machicoane, Ion Source Group Leader, 4/28/2017
Reviewed by — Paul Gibson, Installation Group Leader, 4/21/2017
Reviewed by — Steven Lidia, Diagnostic Group Leader, 4/17/2017

Facility for Rare Isotope Beams
FRIB Front End Alarms and Interlocks
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Table 4: High Voltage Power Supply Interlocks

Interlocked Device Channel	Interlocked Device	Interlocked State	Interlocked By	Device Description	Signal/Limit	Delay	Notes
FE_ISRC1:PSEL_D0698:EN_RCMD	Acceleration Column Electrode Enable	0 – "OFF"	FE_PS:LT_N0001:ON_RCMD	Power Supply Warning Light	0 - "Not On"	None	
			FE_SCS1:VAC_D0739:BYP_RCMD	Charge Selection Vacuump Pumpdown Bypass	1 - "Bypass ON"	None	
			FE_SCS1:CCG_D0707:OK_RSTS_VP	Cold Cathode Gauge Digital Setpoint	0 - "Not Okay" (>2x10^{-5} Torr)	1 s	See Note 1
			FE_SCS1:CCG_D0739:OK_RSTS_VP	Cold Cathode Gauge Digital Setpoint	0 - "Not Okay" (>2x10^{-5} Torr)	1 s	
			FE_ISRC1:IG_D0679:OK_RSTS_VP1	Cold Cathode Gauge Digital Setpoint	0 - "Not Okay" (>2x10^{-5} Torr)	1 s	See Note 1
			FE_ISRC1:IG_D0687:OK_RSTS_VP1	Cold Cathode Gauge Digital Setpoint	0 - "Not Okay" (>2x10^{-5} Torr)	1 s	
FE_PSC01:PSMC_N0101:EN_RCMD	Diagnostic Device Bias Power Supply Enable	0 – "OFF"	FE_SCS1:CCG_D0707:OK_RSTS_VP	Cold Cathode Gauge Digital Setpoint	0 – "Not Okay" (>10-5 Torr)	1 s	See Note 1
			FE_SCS1:CCG_D0739:OK_RSTS_VP	Cold Cathode Gauge Digital Setpoint	0 – "Not Okay" (>10-5 Torr)	1 s	
FE_PSC01:PSMC_N0102:EN_RCMD			FE_LEBT:CCG_D0783:OK_RSTS_VP	Cold Cathode Gauge Digital Setpoint	0 - "Not Okay" (>2x10^{-5} Torr)	1 s	See Note 1
			FE_LEBT:CCG_D0808:OK_RSTS_VP	Cold Cathode Gauge Digital Setpoint	0 - "Not Okay" (>2x10^{-5} Torr)	1 s	
FE_SCS1:QET_D0730	E-Quad Triplet Power Supplies Enable	0 – "OFF"	FE_PS:LT_N0001:ON_RCMD	Power Supply Warning Light	0 - "Not On"	None	
FE_SCS1:PSQ1_D0726:EN_RCMD			FE_SCS1:VAC_D0739:BYP_RCMD	Charge Selection Vacuump Pumpdown Bypass	1 - "Bypass ON"	None	
FE_SCS1:PSQ2_D0726:EN_RCMD			FE_SCS1:CCG_D0707:OK_RSTS_VP	Cold Cathode Gauge Digital Setpoint	0 - "Not Okay" (>2x10-5 Torr)	1 s	See Note 1
FE_SCS1:PSQ1_D0730:EN_RCMD							
FE_SCS1:PSC							
FE_SCS1:PSC							
FE_SCS1:PSC							
FE_SCS1:QET							
FE_SCS1:PSC							
FE_SCS1:PSC							
FE_SCS1:PSC							
FE_SCS1:PSC							
FE_SCS1:PSC							

Facility for Rare Isotope Beams
Front End Controls Installation and Interlock Test Records
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Issued Draft 26 July 2017

Interlocked Device Channel	Interlocked Device	Interlocked State	Interlocked By	Device Description	Signal/Limit	Delay	Notes	Test Results	Tested By	Date Tested
FE_ISRC1:PSEL_D0698:EN_RCMD	Acceleration Column Electrode Enable	0 – "OFF"	FE_PS:LT_N0001:ON_RCMD	Upper FE Power Supply Warning Light	0 - "Not On"	None		PASS	LH	
			FE_SCS1:VAC_D0739:BYP_RCMD	Charge Selection Vacuump Pumpdown Bypass	1 - "Bypass ON"	None		PASS	LH	
			FE_SCS1:CCG_D0707:OK_RSTS_VP	Cold Cathode Gauge Digital Setpoint	0 - "Not Okay" (>2x10^{-5} Torr)	1 S	See Note 1	PASS	LH	
			FE_SCS1:CCG_D0739:OK_RSTS_VP	Cold Cathode Gauge Digital Setpoint	0 - "Not Okay" (>2x10^{-5} Torr)	1 S		PASS	LH	
			FE_ISRC1:IG_D0679:OK_RSTS_VP1	Cold Cathode Gauge Digital Setpoint	0 - "Not Okay" (>2x10^{-5} Torr)	1 S	See Note 1	PASS	LH	
			FE_ISRC1:IG_D0687:OK_RSTS_VP1	Cold Cathode Gauge Digital Setpoint	0 - "Not Okay" (>2x10^{-5} Torr)	1 S		PASS	LH	
FE_PSC01:PSMC_N0101:EN_RCMD	Diagnostic Device Bias Power Supply Enable	0 – "OFF"	FE_SCS1:CCG_D0707:OK_RSTS_VP	Cold Cathode Gauge Digital Setpoint	0 – "Not Okay" (>10-5 Torr)	1 S	See Note 1	PASS	LH	
			FE_SCS1:CCG_D0739:OK_RSTS_VP	Cold Cathode Gauge Digital Setpoint	0 – "Not Okay" (>10-5 Torr)	1 S		PASS	LH	
FE_PSC01:PSMC_N0102:EN_RCMD			FE_LEBT:CCG_D0783:OK_RSTS_VP	Cold Cathode Gauge Digital Setpoint	0 - "Not Okay" (>2x10^{-5} Torr)	1 S	See Note 1	PASS	LH	
			FE_LEBT:CCG_D0808:OK_RSTS_VP	Cold Cathode Gauge Digital Setpoint	0 - "Not Okay" (>2x10^{-5} Torr)	1 S		PASS	LH	
FE_SCS1:QET_D0730	E-Quad Triplet Power Supplies Enable	0 – "OFF"	FE_PS:LT_N0001:ON_RCMD	Upper FE Power Supply Warning Light	0 - "Not On"	None		PASS	LH	
FE_SCS1:PSQ1_D0726:EN_RCMD			FE_SCS1:VAC_D0739:BYP_RCMD	Charge Selection Vacuump Pumpdown Bypass	1 - "Bypass ON"	None		PASS	LH	
FE_SCS1:PSQ2_D0726:EN_RCMD			FE_SCS1:CCG_D0707:OK_RSTS_VP	Cold Cathode Gauge Digital Setpoint	0 - "Not Okay" (>2x10-5 Torr)	1 S	See Note 1	PASS	LH	
FE_SCS1:PSQ1_D0730:EN_RCMD								PASS	LH	
FE_SCS1:PSQ2_D0730:EN_RCMD								PASS	LH	
FE_SCS1:PSQ1_D0733:EN_RCMD			FE_SCS1:CCG_D0739:OK_RSTS_VP	Cold Cathode Gauge Digital Setpoint	0 - "Not Okay" (>2x10-5 Torr)	1 S		PASS	LH	

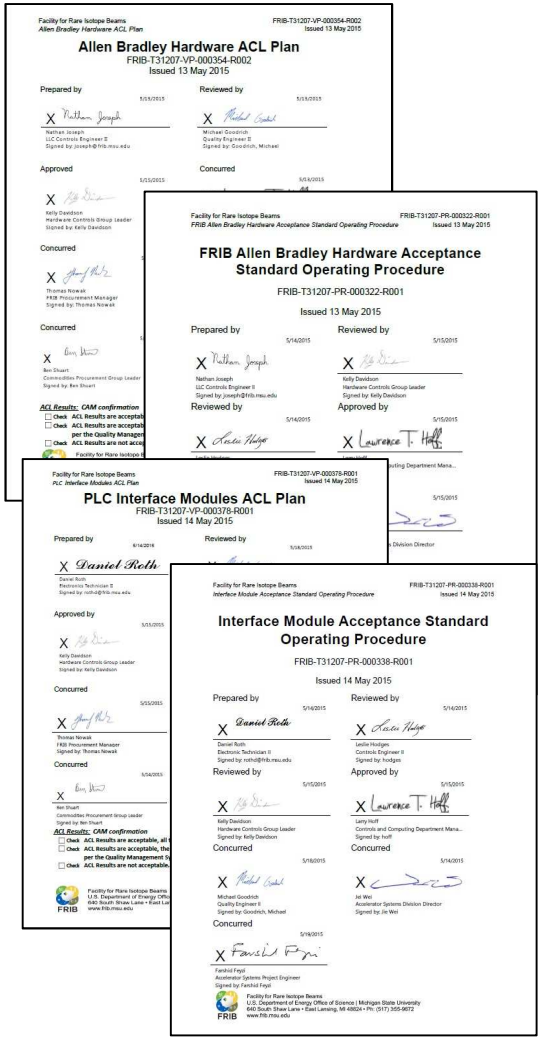
Summary

- Testing completed at each level ensures quality installation and reduces engineers time troubleshooting at the final level
- Beamline performs as intended on first commissioning/integration tests – reducing calls for support

Backup Slides

Quality Assurance - Acceptance Testing Plans Developed for PLC Hardware

- Acceptance and SOP Test documents developed for PLC components and Interface Modules (IFMs),
  - Allen Bradley Hardware ACL Plan (T31207-VP-000354)
  - FRIB Allen Bradley Hardware Acceptance Standard Operating Procedure (T31207-PR-000322)
  - Programmable Logic Controller (PLC) Interface Modules Acceptance Criteria Listing (ACL) Plan (T313207-VP-000378)
  - Interface Module Acceptance Standard Operating Procedure (T3107-PR-000338)
- Acceptance testing is performed once parts are received and documented in a verification report (VR)



VERIFICATION PLAN and TESTING REQUIREMENTS				
ITEM NO.	**REQ ID or DCC doc #**	**DESCRIPTION OF TEST TO BE CONDUCTED, VERIFIED or WITNESSED**	**METHOD or TOOL**	**VERIFYING ENTITY**
1	[1] frib-ctrl_5.4-1	CHASSIS(BACKPLANE): Verify quantity for applicable P/Ns; 1756-A10, 1756-A7	VISUAL	(FRIB) LLC
1a	N/A	Visual inspection for shipping damage	VISUAL	(FRIB) LLC
1b	T31207-PR-000322-R001	Bench test 5% of components received	TEST BENCH	(FRIB) LLC
2	[1] frib-ctrl_5.4-1	POWER SUPPLIES: Verify quantity for applicable P/Ns; 1756-PA72, 1734-EP24DC, 1606-XLE240EN	VISUAL	(FRIB) LLC
2a	N/A	Visual inspection for shipping damage	VISUAL	(FRIB) LLC

VERIFICATION PLAN and TESTING REQUIREMENTS				
ITEM NO.	**REQ ID or DCC doc #**	**DESCRIPTION OF TEST TO BE CONDUCTED, VERIFIED or WITNESSED**	**METHOD or TOOL**	**VERIFYING ENTITY**
1		Analog Input, PLC Interface Module		
1a	N/A	Assign serial number if not previously assigned	VISUAL	(FRIB) LLC
1b	N/A	Check integrity of the assembly for damage and that all components are mounted securely.	VISUAL	(FRIB) LLC
1c	T31207-PR-000338-R001	Bench Test 100% of components received	TEST BENCH	(FRIB) LLC
2		Analog Output, PLC Interface Module		
2a	N/A	Assign serial number if not previously assigned	VISUAL	(FRIB) LLC
2b	N/A	Check integrity of the assembly for damage and that all components are mounted securely.	VISUAL	(FRIB) LLC
2c	T31207-PR-000338-R001	Bench Test 100% of components received	TEST BENCH	(FRIB) LLC