RE22- PANDA MVD

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on behalf of the PANDA MVD group

H2/H4 meeting, April 15th 2015, CERN

Overview

Request: test of silicon device prototypes for the Micro Vertex Detector of PANDA (RE22) experiment.

- Available Prototypes
- Setup: reduction of the space request
- Beam time: scheduled too early in July

The Micro Vertex Detector

It must combine good space resolution with accurate time-tagging

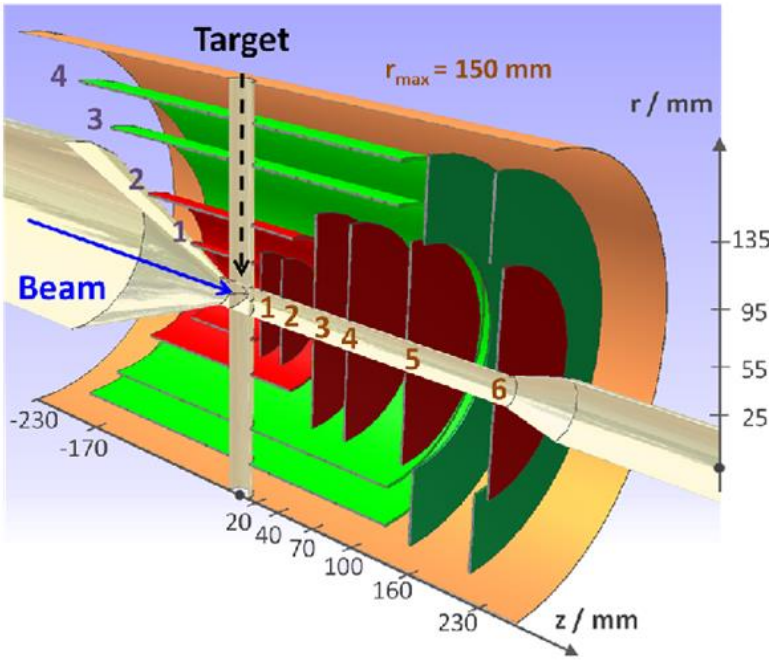
Main functions

- Primary vertex reconstruction
- Identification of the secondary vertices

($c\tau$ of some hundreds of μm)

- Improvement in momentum resolution
- Support PID of low momentum particles

by energy loss measurement



- Good spatial resolution (some tens of μm in $\rho\phi$, better than 100 μm along z)
- Time resolution < 10 ns
- Continuous readout at ~ 10^7 interactions /s (clock signal @160 MHz)
- Limited material budget X/Xo ≤ 1 % / layer
- Radiation tolerance < 10^{14} n $_{1\ MeV\ eq}$ cm^{-2}
- Provide at least four hits per track
- Energy loss measurement
- Room temperature operation
- Routing and services only in the backward region

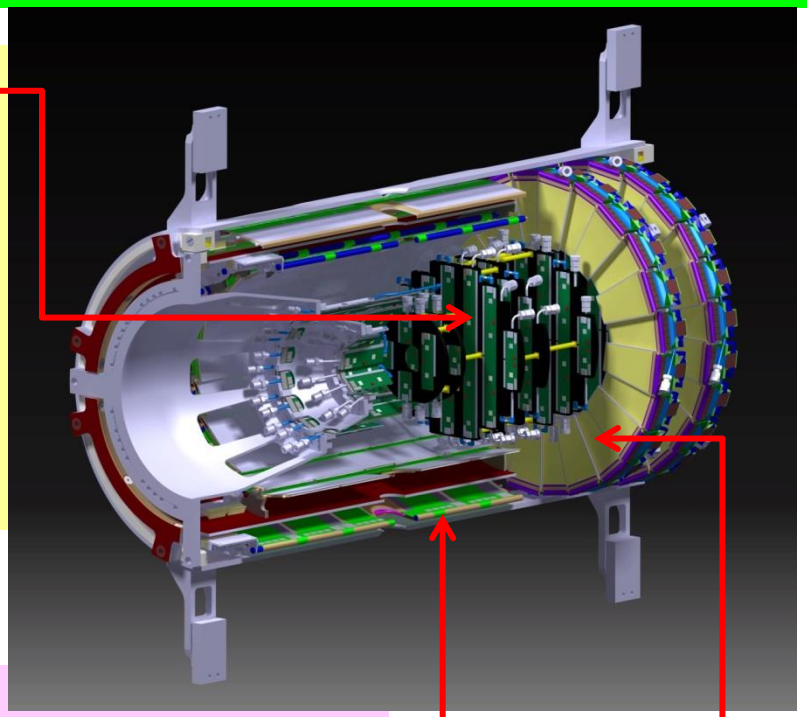
10.3 M (pixel channels) – active area: 0.106 m^2

162 k (strip channels) – active area: 0.494 m^2

Silicon devices

Hybrid epitaxial silicon pixel:

- ✓ **Sensor** made of Epitaxial Silicon material
  - ρ_{epi} ~ kΩ·cm
  - ρ_{Cz} ~ 20-50 mΩ·cm
- ✓ **Pixel cell size**: 100μm x 100μm x 100μm
- ✓ **ASIC** developed in 130 nm CMOS technology (ToPix)
  - Triggerless
  - dE/dx using Time over Threshold technique

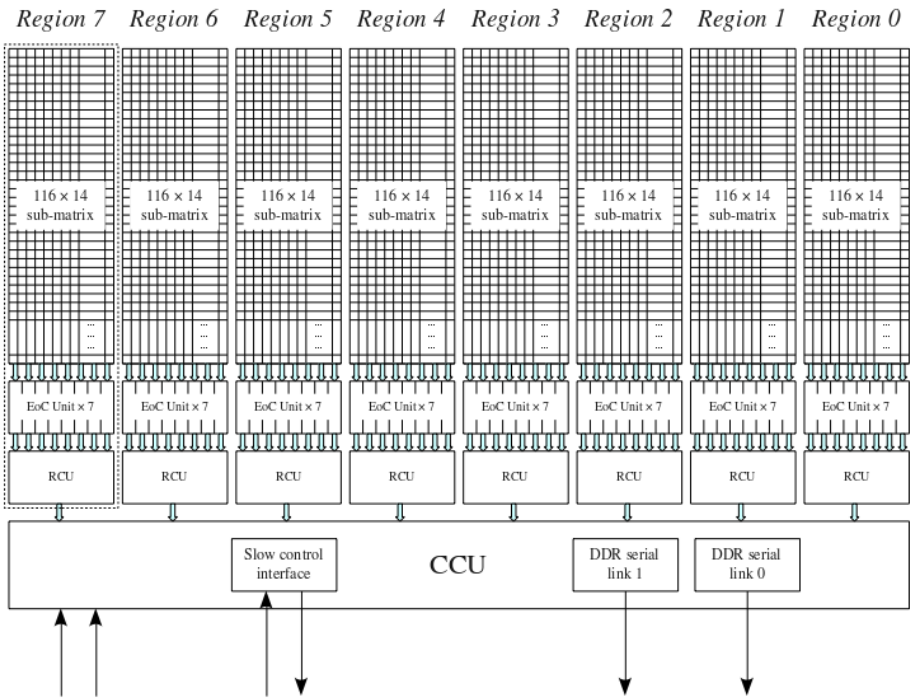


Double sided silicon micro strips:

- ✓ Rectangular (512 x 896 strips) and squared (512 x 512 strips) **sensors**;
  stereo angle: 90°, strip pitch: 67.5 μm, 285 μm thickness
- ✓ Trapezoidal (768 x 768 strips) **sensors**;
  stereo angle: 15°, pitch: 45 μm, 285 μm thickness

- ✓ **ASIC** developed in 110 nm CMOS technology (PASTA)
  - Triggerless
  - ToT technique for dE/dx measurement

ToPix



- Columns divided in 8 regions with 7 double columns each
- FIFO in the end of column and region control
- Output bandwidth: 2 x 320 Mb/s
- Supply voltage: 1.2 V

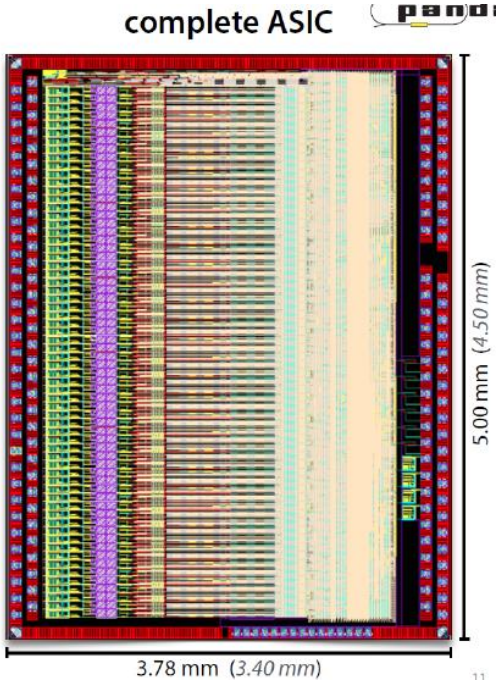
- Pixel matrix: 110 x 116
- Size (to be optimized):
  11.2 mm x 14.8 mm
- dE/dx measurement: ToT,
  12 bits dynamic range
- Maximum input charge: 50 fC
- Detector type: *n* and *p*
- Noise floor: < 200 electrons
- Input clock frequency: 160 MHz
- Time resolution: ~ 6 ns
- Power consumption: ≤ 0.8 W/cm^2
- Maximum event rate/cm^2: ~ 6.1 x 10^6
- Data rate per chip: up to ~ 450 Mb/s

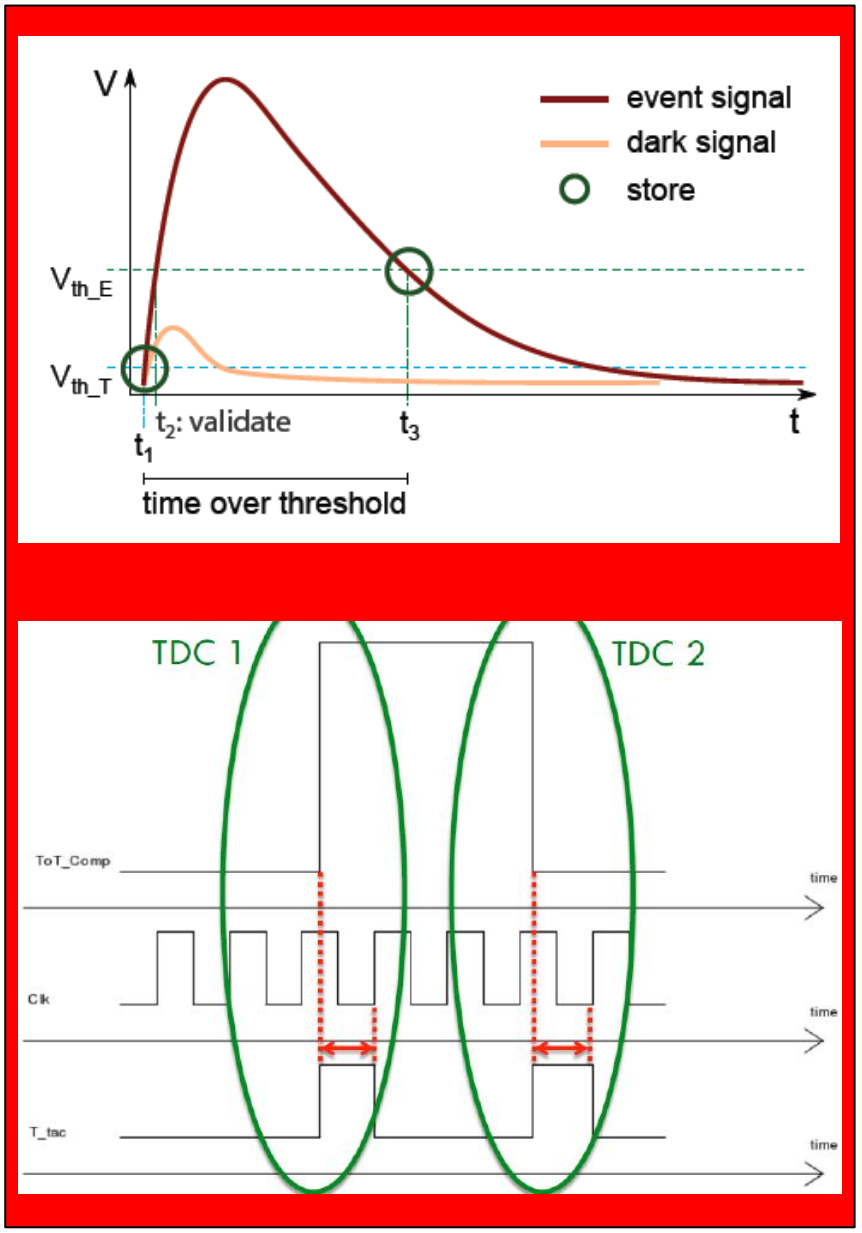
PASTA

First prototype under submission:

- 64 channel (full size), 3.8 mm x 4.5 mm
- Input capacitance/charge: → 25 fF / 40 fC
- Dynamic range: 8 bit
- Power consumption: < 4 mW/ch
- Noise < 1500 e-
- Time bin width ~ 100 ps
- Channel pitch: 60 μm

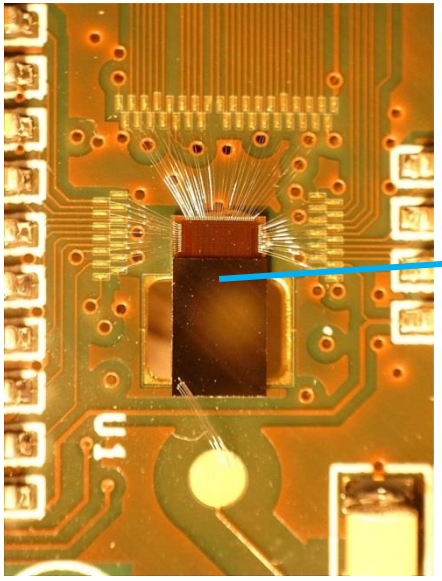
Development of TofPet Project



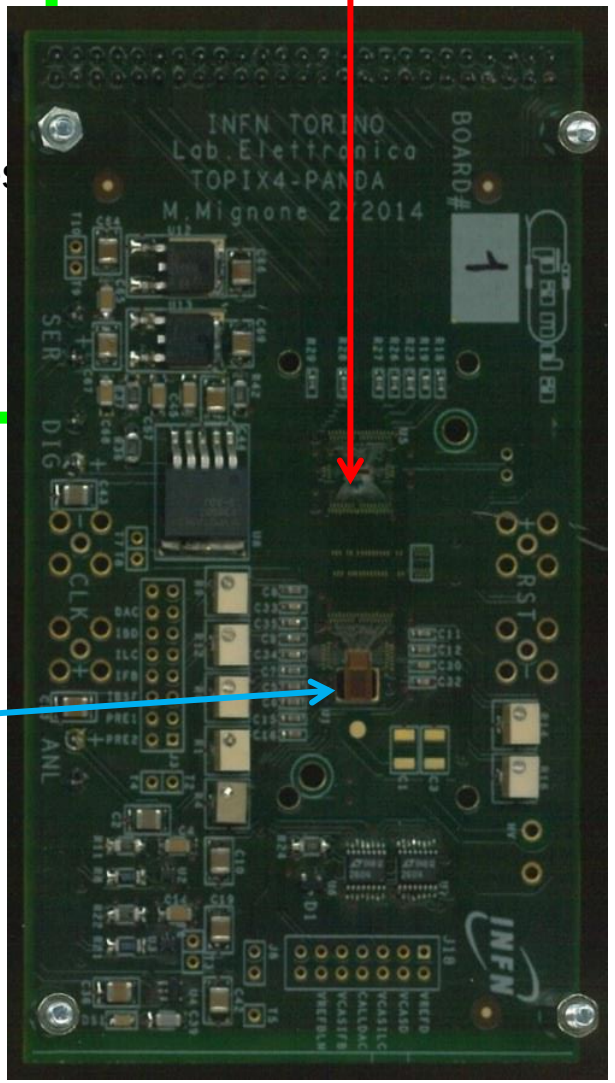


Single chip assembly based on ToPix_v4

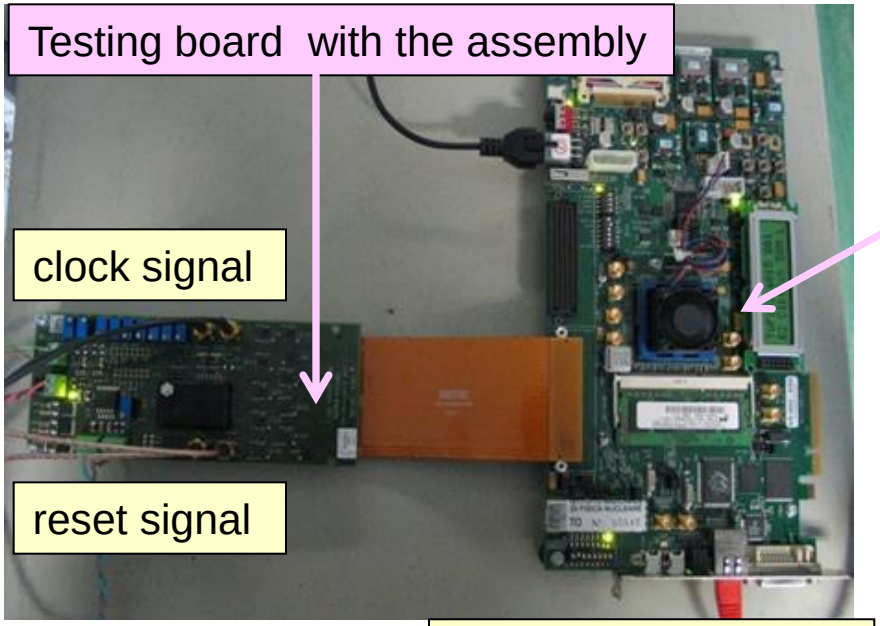
- ASIC size: 3 mm x 6 mm
- 130 nm CMOS technology
- Input clock frequency: 160 MHz
- Pixel matrix: 640 cells (100μmx100μmx100μm), 2x2x128 and 2x2x32 columns
- Epitaxial silicon sensor (100 μm thick): 3.2 mm x 2 mm
- Hamming encoding and TMR pixel logic protection
- Leading and trailing edge registers with DICE -protected latches
- SEU protected EoC
- Serial data output (SDR and DDR)
- Frame based transmission
- GBT compatible SLVS I/O



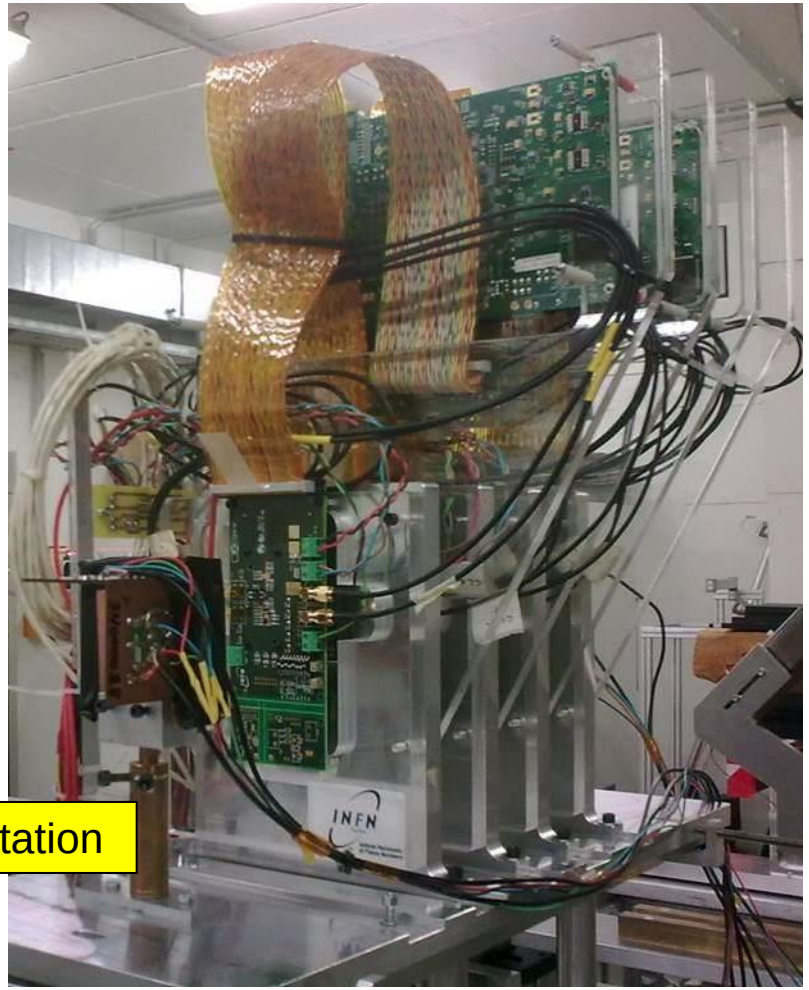
SLVS-LVDS translator



Setup

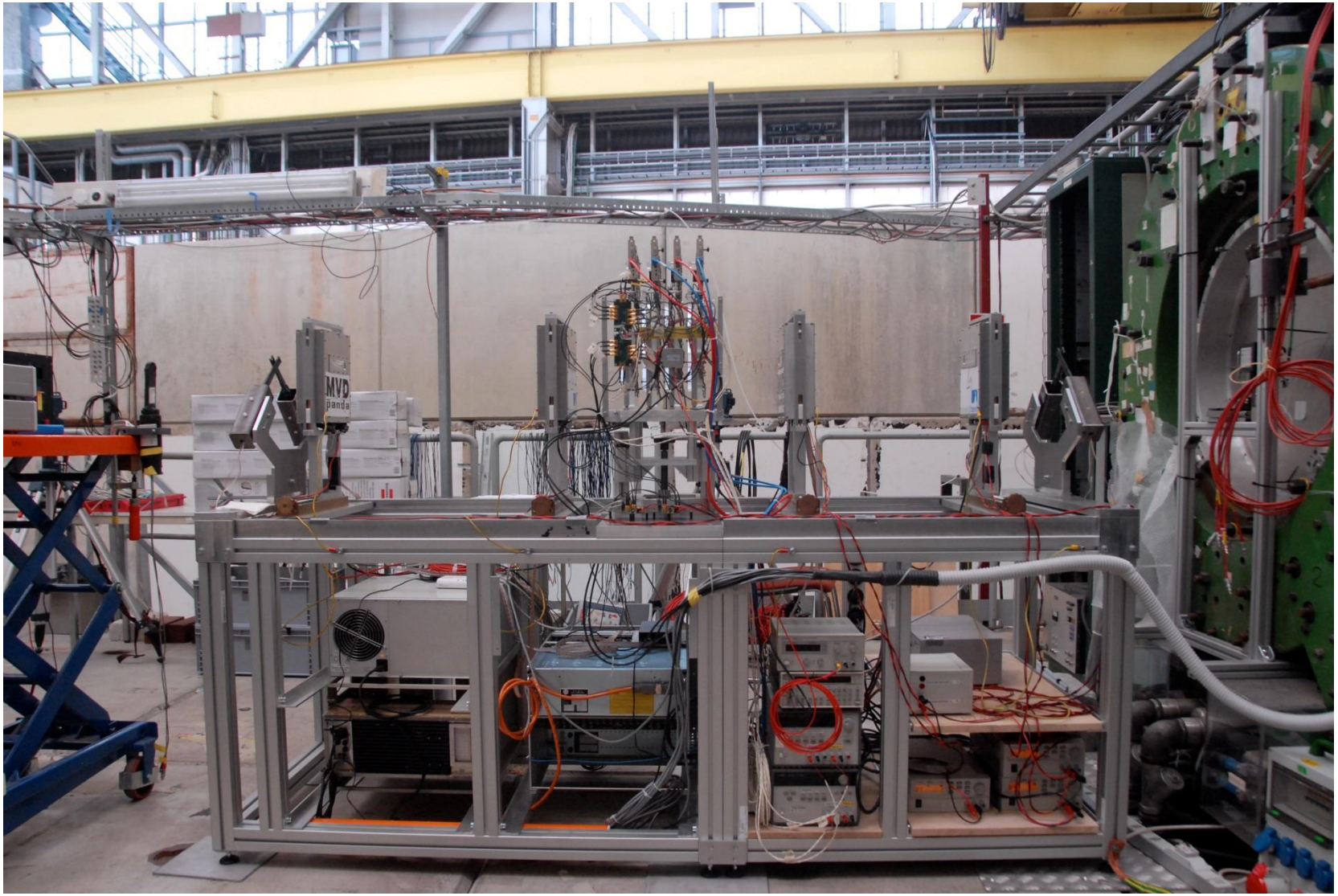


Xilinx Evaluation Board equipped with a Virtex 6 FPGA

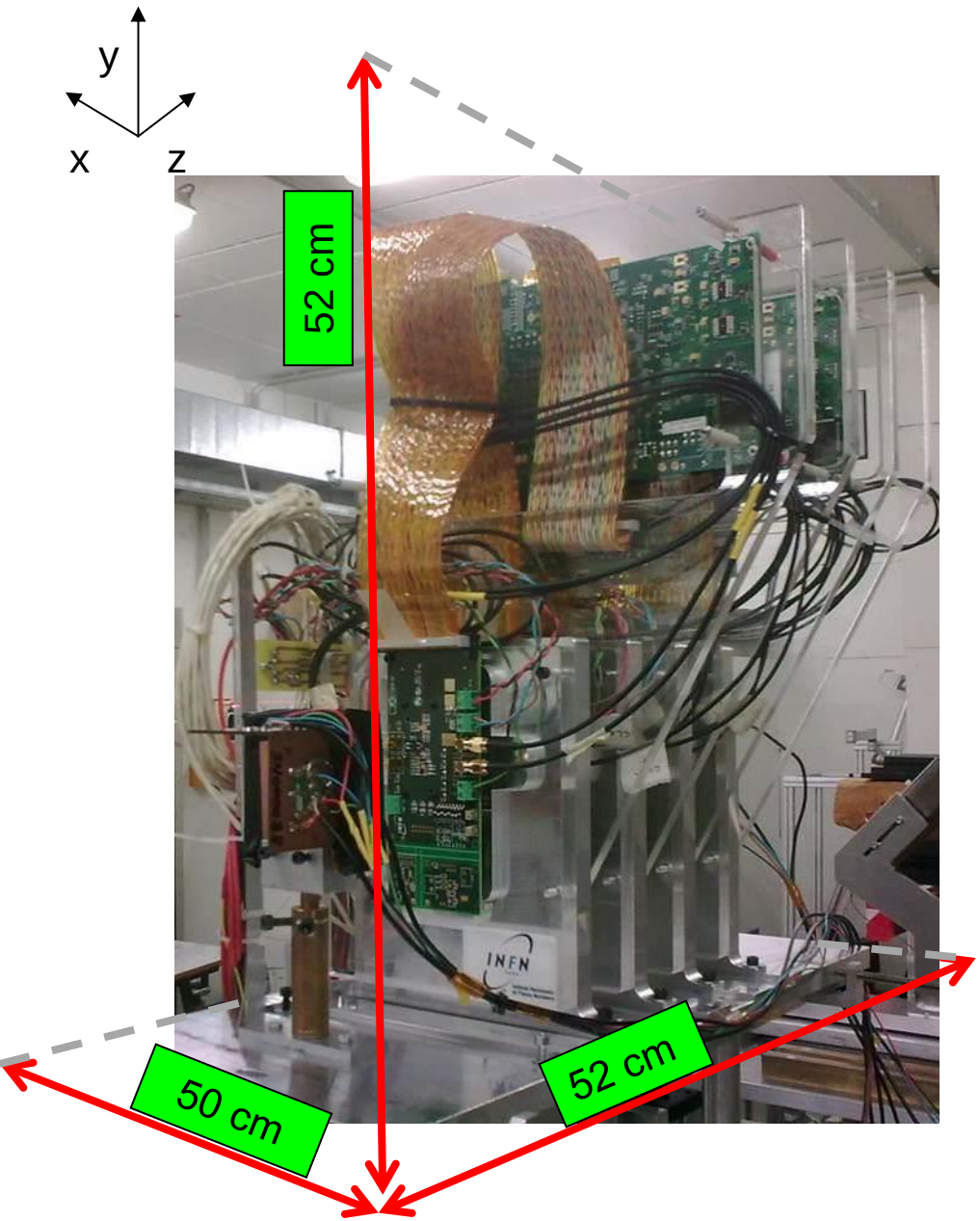


Pixel tracking station

Long table for pixel and strips



Pixel tracking station



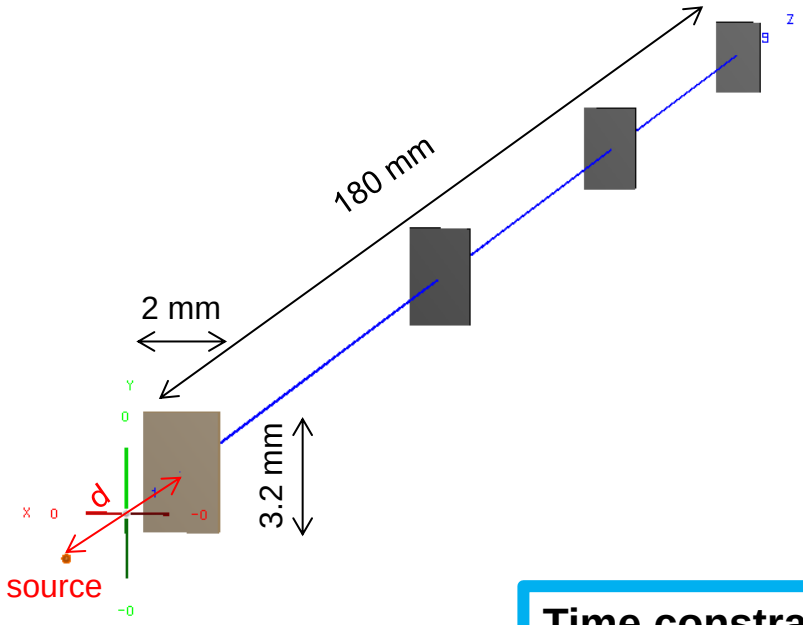
Requests to Cern:

- x-y table
- alignment support along the beam line
- Equipment to check alignment during the data taking.

- Power requirements: 220 V- 20 A
- Point to point Ethernet cables (min. 2 lines, max. length less than 30 m) between the setup and the counting room
- Space to allocate 4 power supplies and 1 crate NIM close the setup

- in the counting room , 2 workstations for daq and analysis

Beam parameter request



Requests to Cern:

- Pion beam momenta: 10 GeV/c and 100-150 GeV/c (polarity does not matter)
- (Proton beam momentum: 20 GeV/c and 100 GeV/c)
- Beam size: 3 mm x 3 mm
- @ different intensities: 10^4, 10^5, 10^6, 10^7 /spill
- Spill length of ~ 10 s, interspill time of ~ 50 s
- Beam divergence:
  Point-like source @ d=30 cm: ~ 0.19°
  @ d=60 cm: ~ 0.12°
  @ d=100 cm: ~ 0.08°

Time constraints:

- Not before of the last week of July (I mean not before July 27th)
- The present schedule foresees beam already Wednesday 22nd

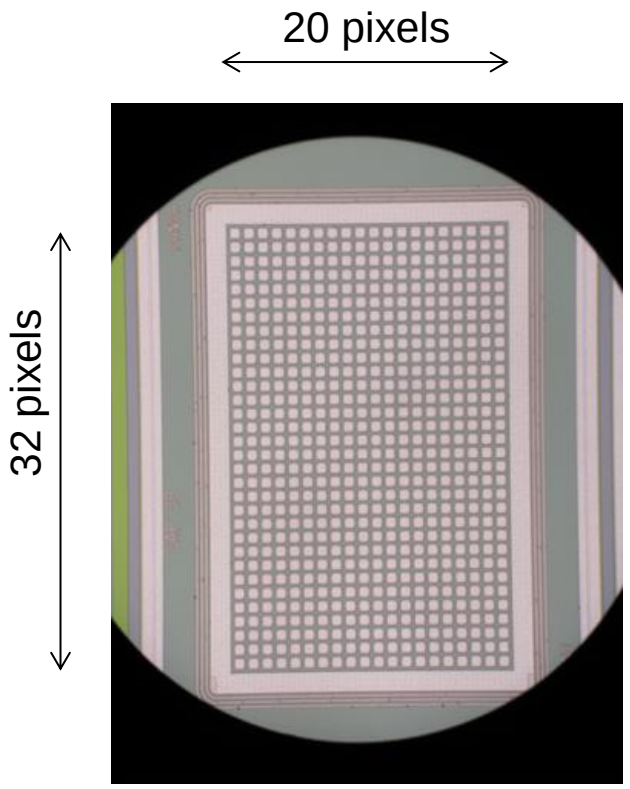
SPARES

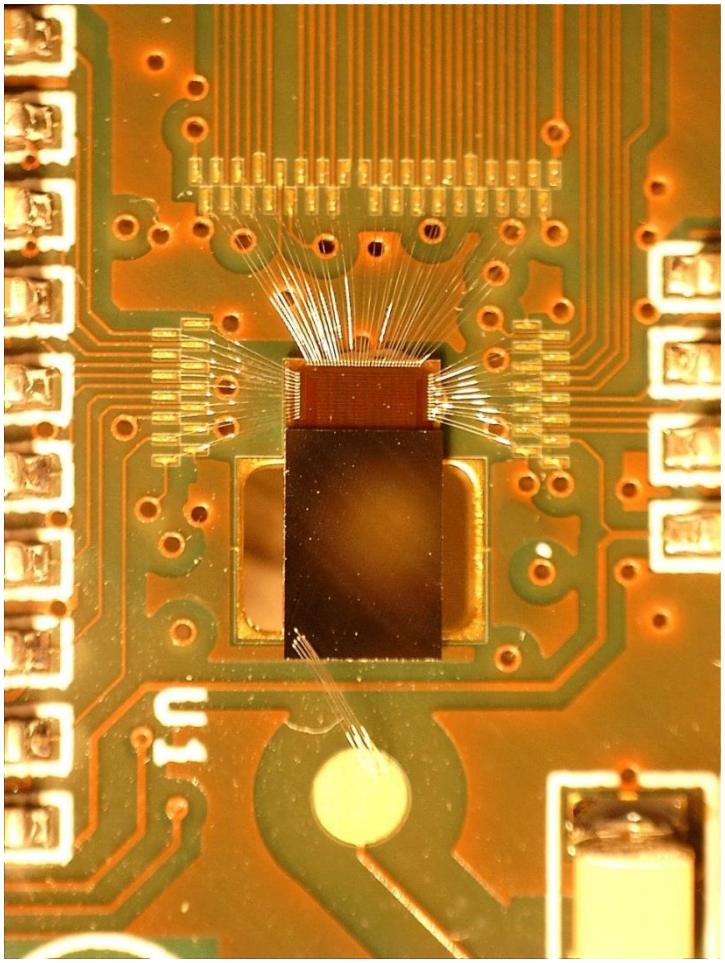
Single chip assembly

- Epitaxial silicon wafer by ITME (Varsaw)
  ρ_{epi} ~ 1500 Ω·cm
- Pixels @ FBK (Trento)
  100μm x 100μm
- Cz thinning + Bump bonding @ IZM (Berlin)
  Sn-Pb bumps

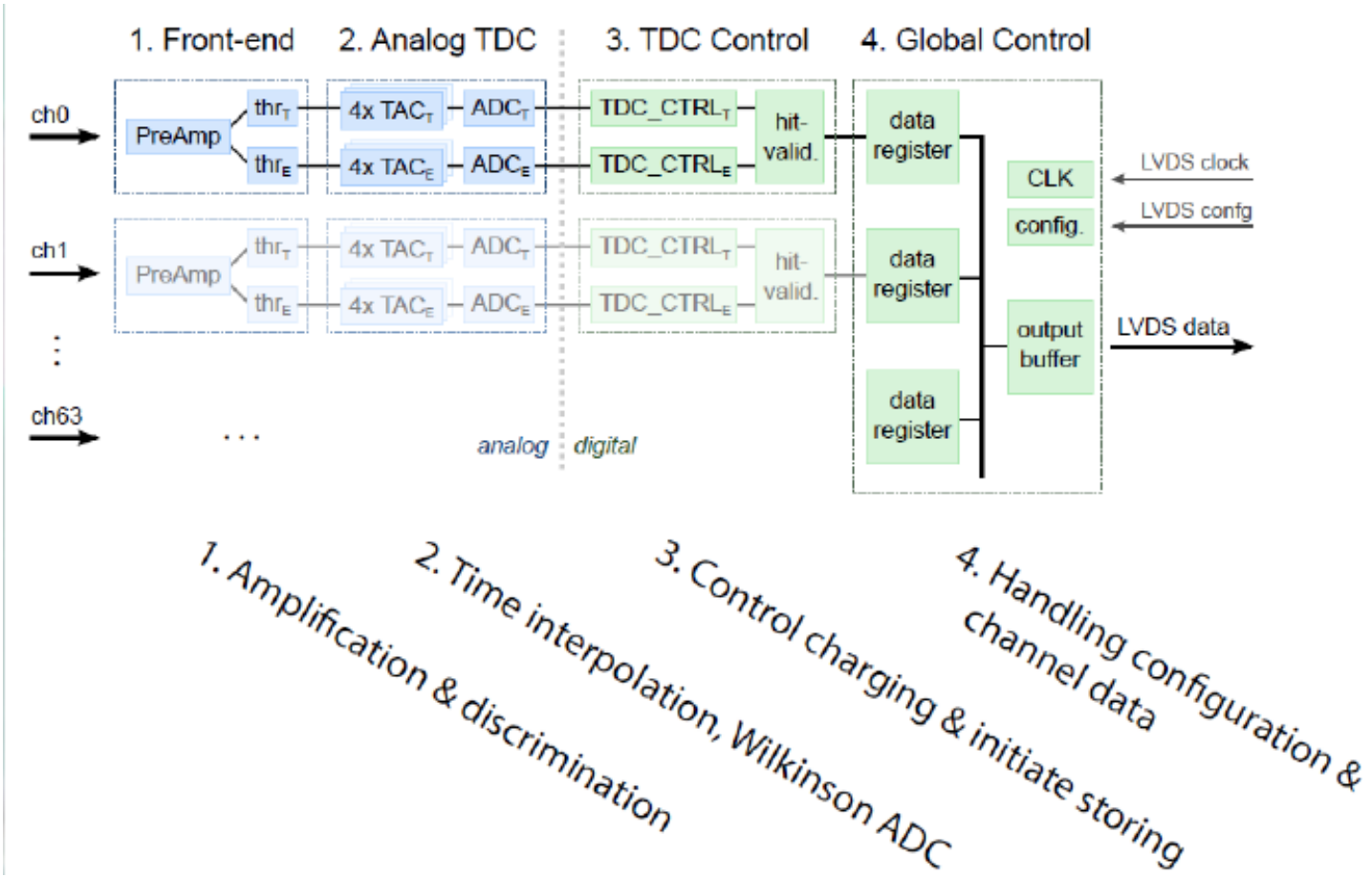
  Bump bonding yield of the tested assemblies: ~ 99.5 %

Thin Cz layer is the ohmic contact for the sensor biasing





PASTA architecture



ToPix4 data format

2	12	8	12	6
01	Chip address	FC	Not used	ECC

Frame header packet

2	14	12	12
11	Pixel address	Leading edge time	Trailing edge time

Data packet

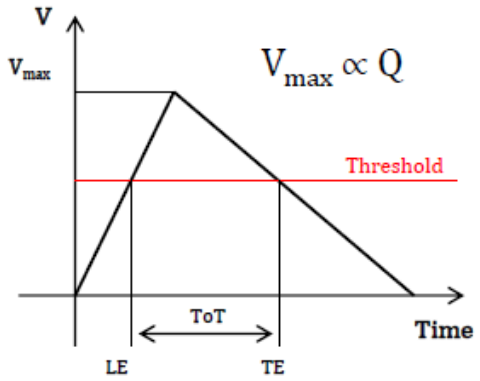
2	16	16	6
10	# of events	CRC	ECC

Frame trailer packet

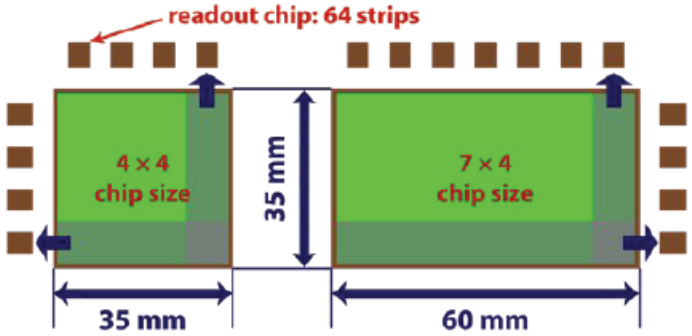
2	38
00	idle code (Hex 3A55AA55AA)

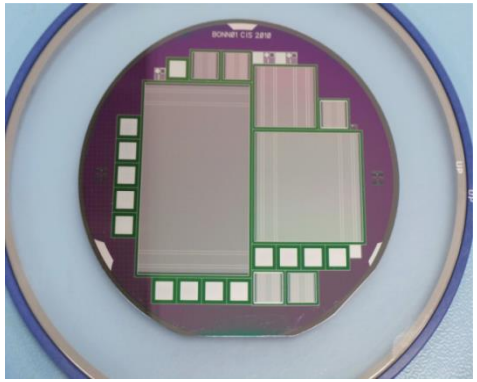
Idle packet

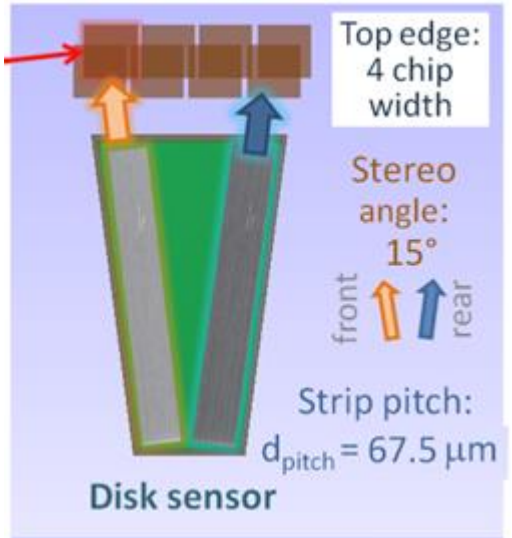
Output frequency	160, 320 Mb/s
Time stamp counter frequency	160, 80 MHz
Time stamp mode	Binary, Gray
Idle packet	off, on
Analog timeout	off, on
Detector type	n-type, p-type
SLVS current control	0000 (max), 1111(off)
Driver pre-emphasis	off, on

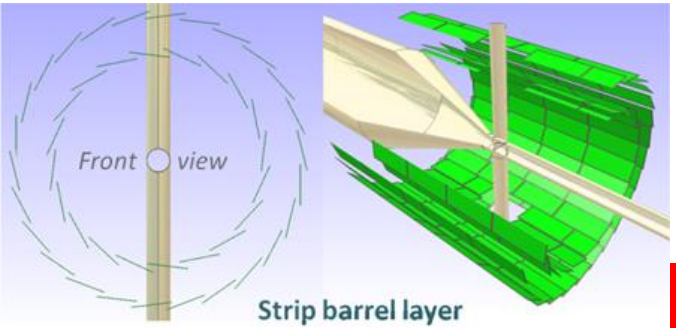


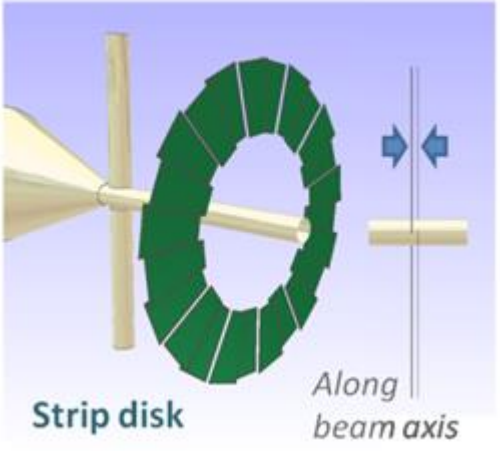
Double-sided silicon strips











3112 readout chips / 296 sensors

Rectangular (512 x 896 strips) and squared (512 x 512 strips) **sensors**;

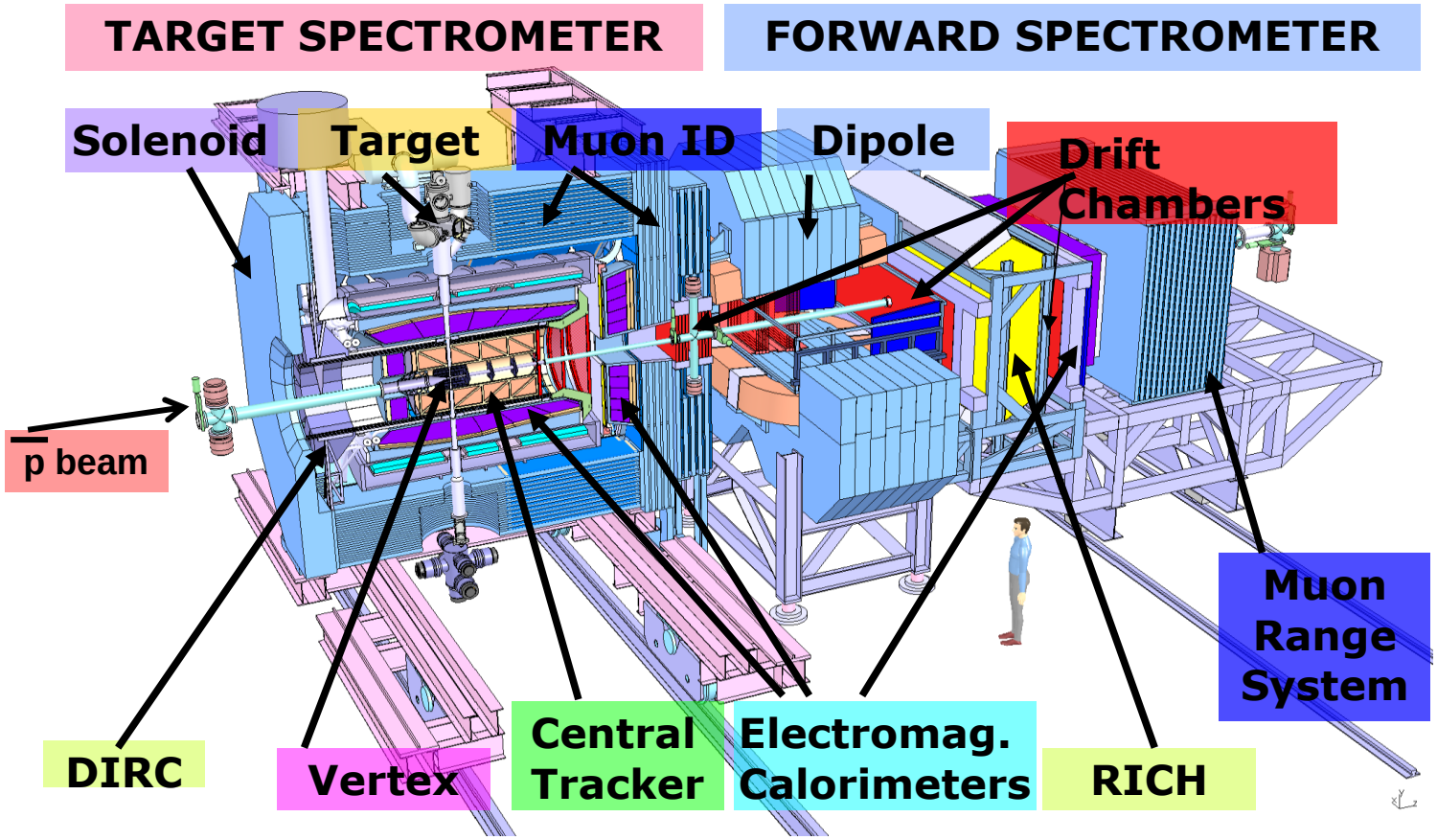
stereo angle: 90°, pitch: 67.5 μm

Trapezoidal (768 x 768 strips) sensors; stereo angle: 15°, pitch: 45 μm

285 μm thickness

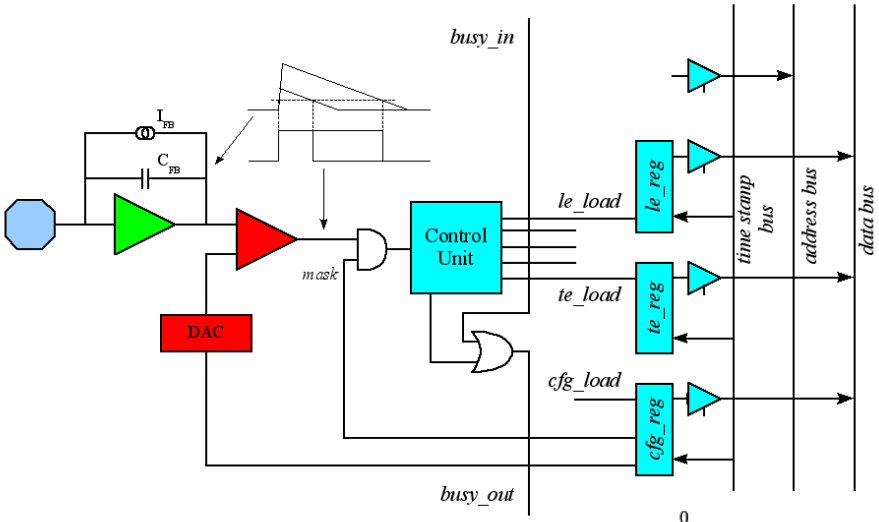
Readout every second strip with self trigger ASIC and ToT technique for dE/dx

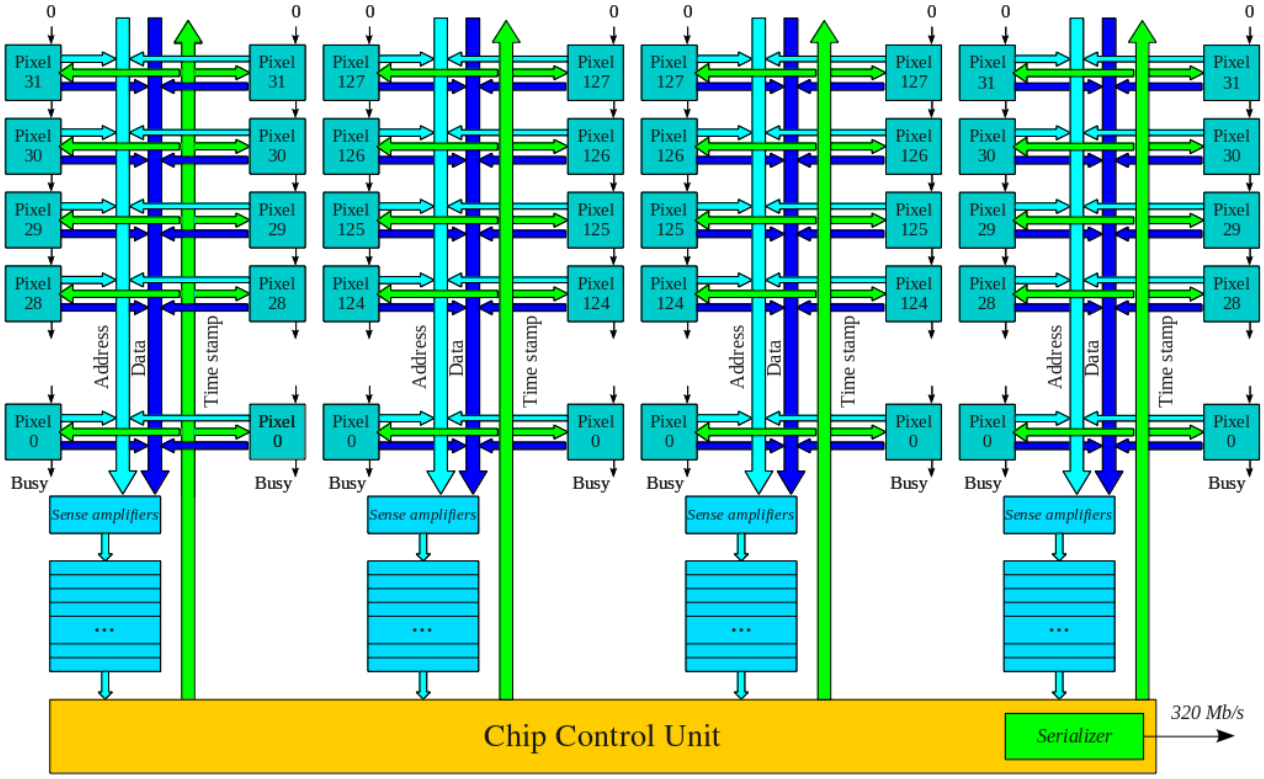
The PANDA experiment



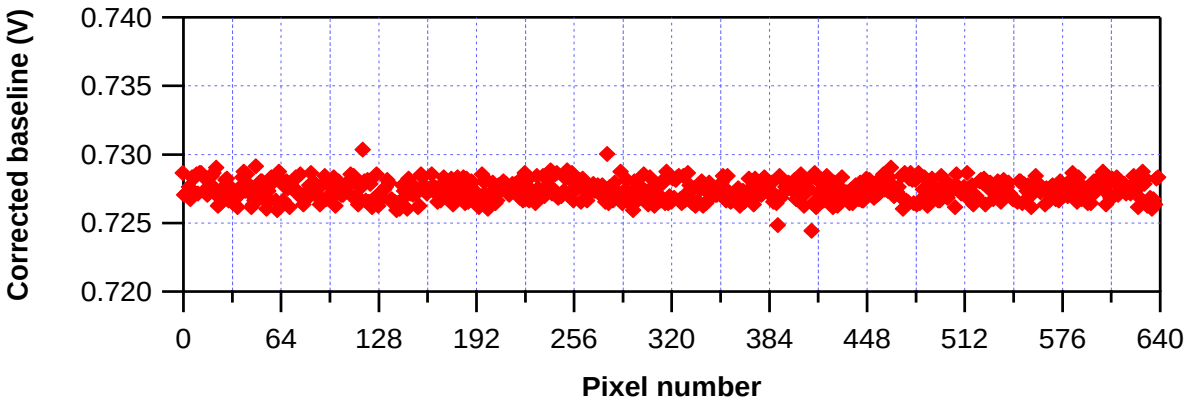
PANDA is a fixed target experiment with frozen hydrogen pellet and heavier nuclear targets (N, Ne, Ar…)

ToPix

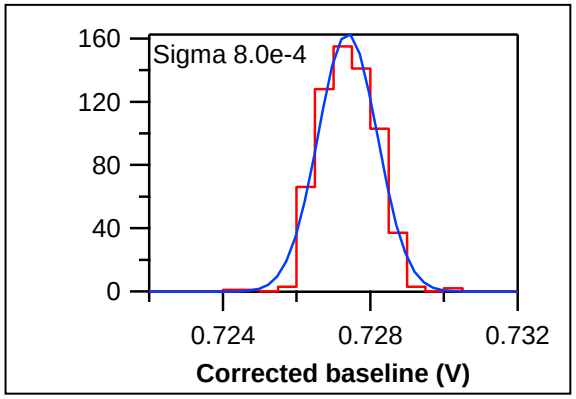

busy_in
I_{FB}
C_{FB}
Control Unit
mask
DAC
le_load
te_load
cfg_load
le_reg
te_reg
cfg_reg
time stamp bus
address bus
data bus
busy_out


Pixel 31
Pixel 30
Pixel 29
Pixel 28
Pixel 127
Pixel 126
Pixel 125
Pixel 124
Pixel 0
Address
Data
Time stamp
Busy
Sense amplifiers
Chip Control Unit
Serializer
320 Mb/s

ToPix_v4

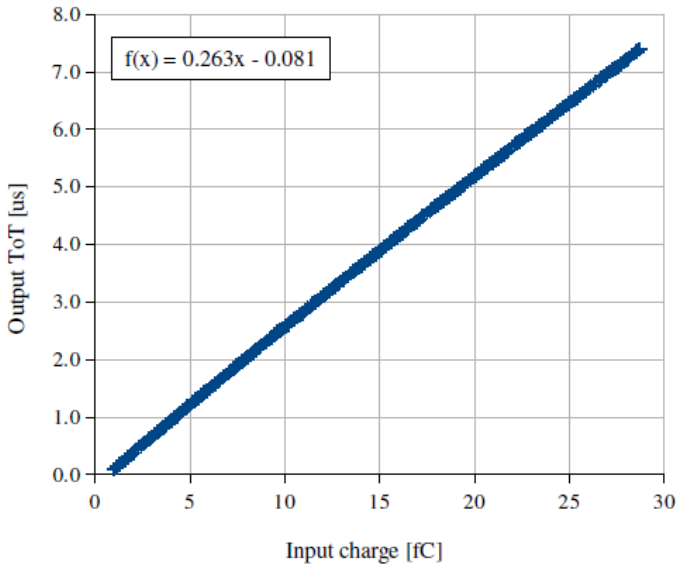


640 pixel DACs completely linear
Easy calibration

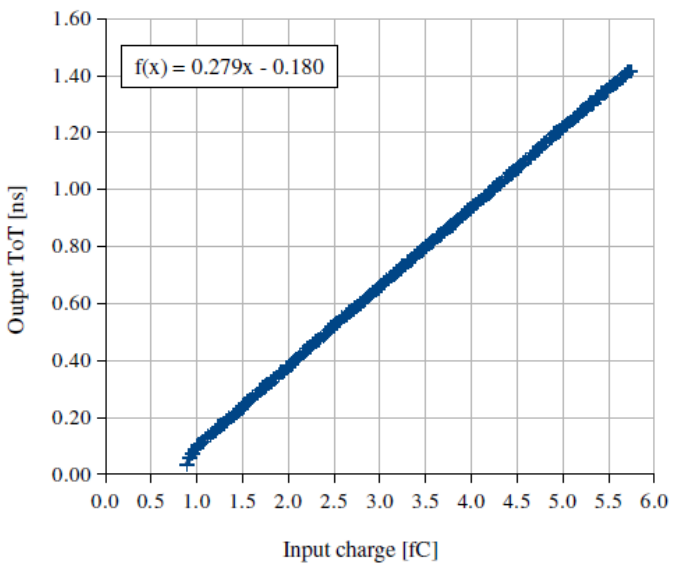


Measured perfomance @ 160 MHz clock

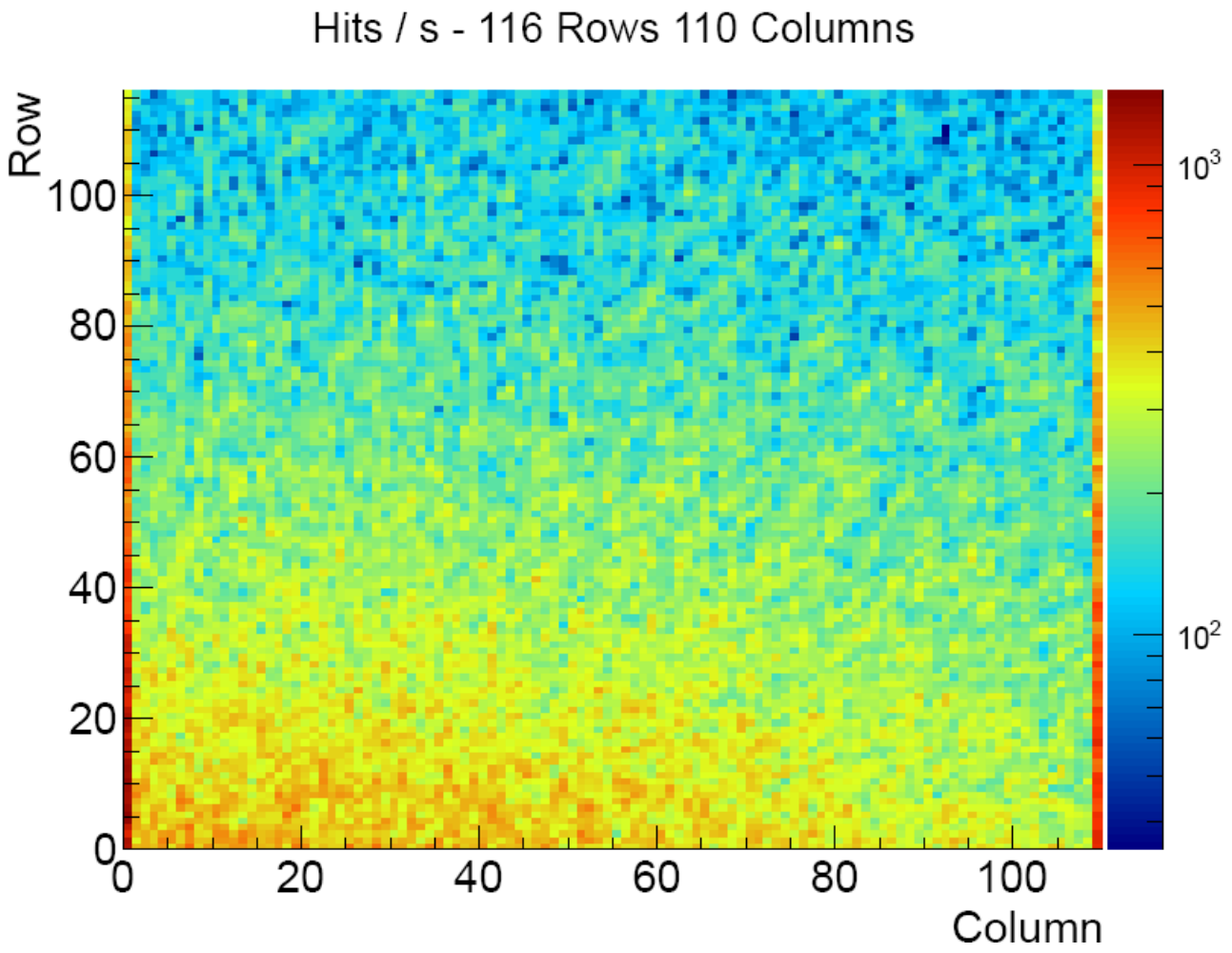
Full range



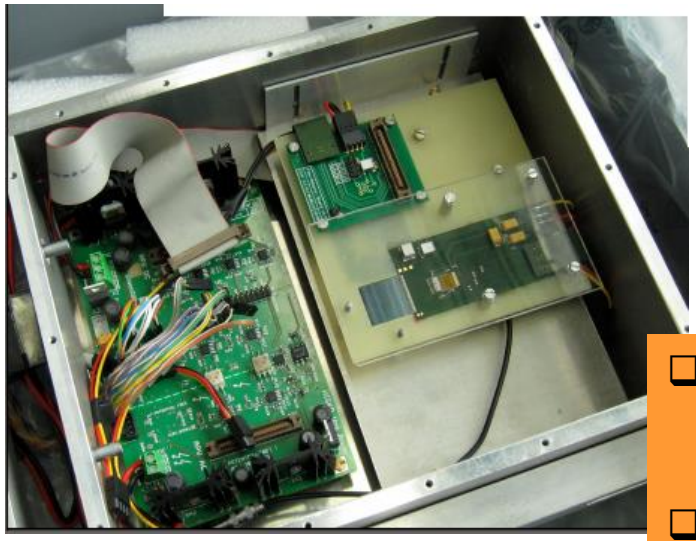
Range 0÷6 fC



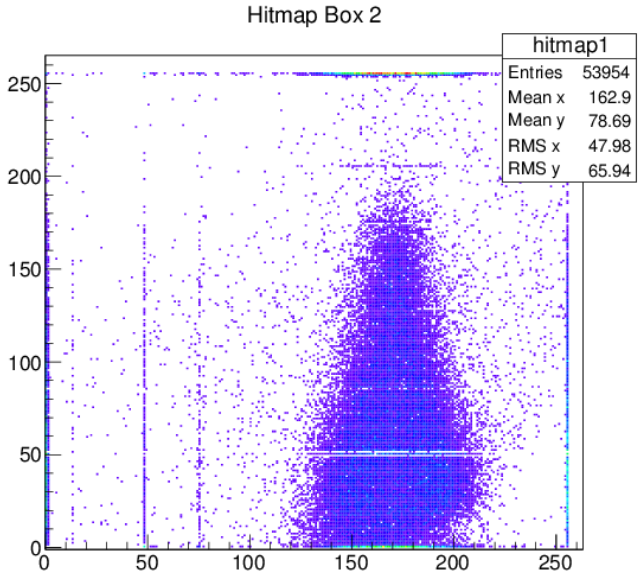
Hit map from simulation

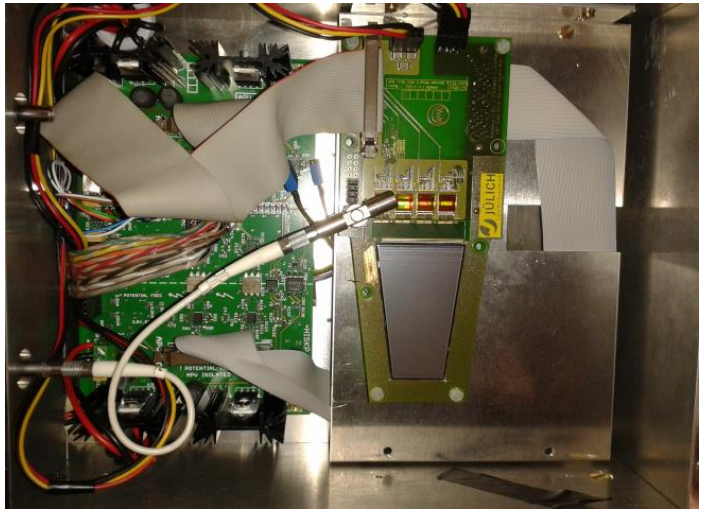


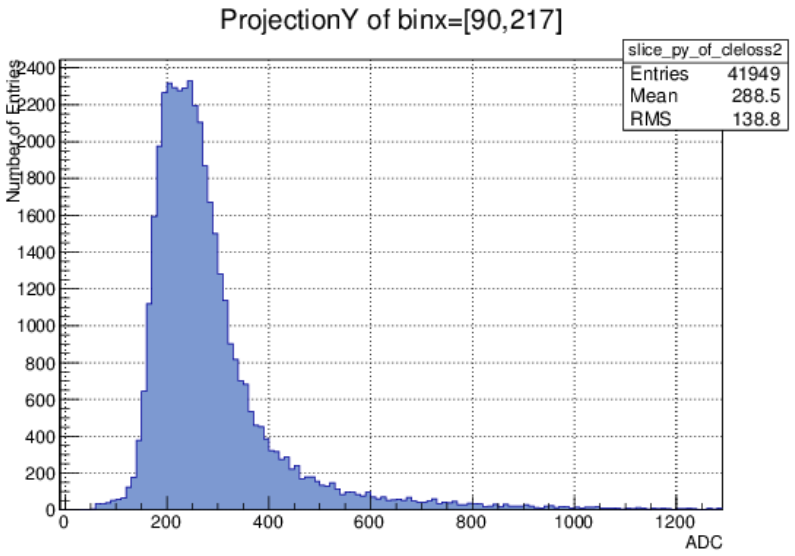
Strip prototypes



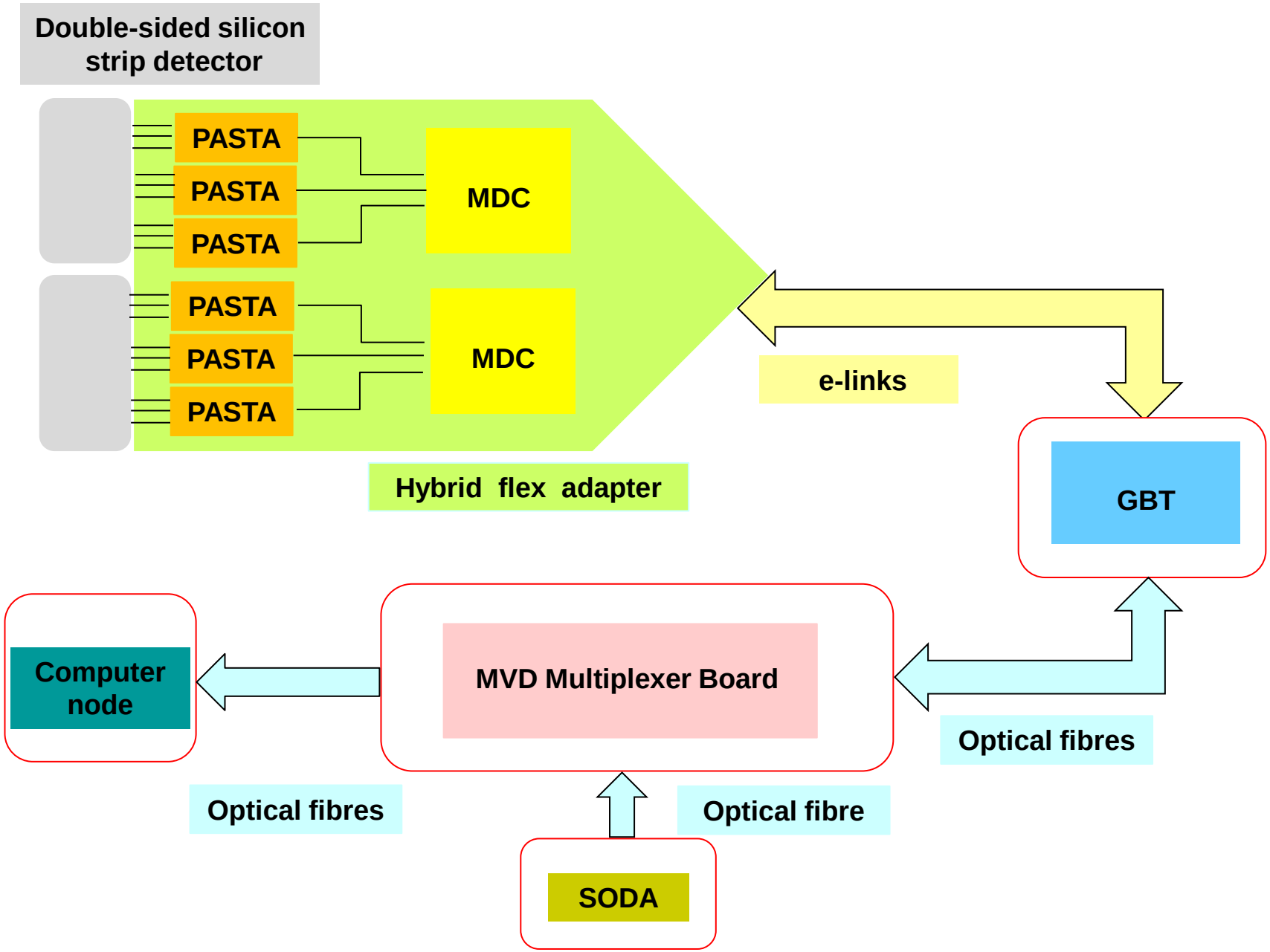
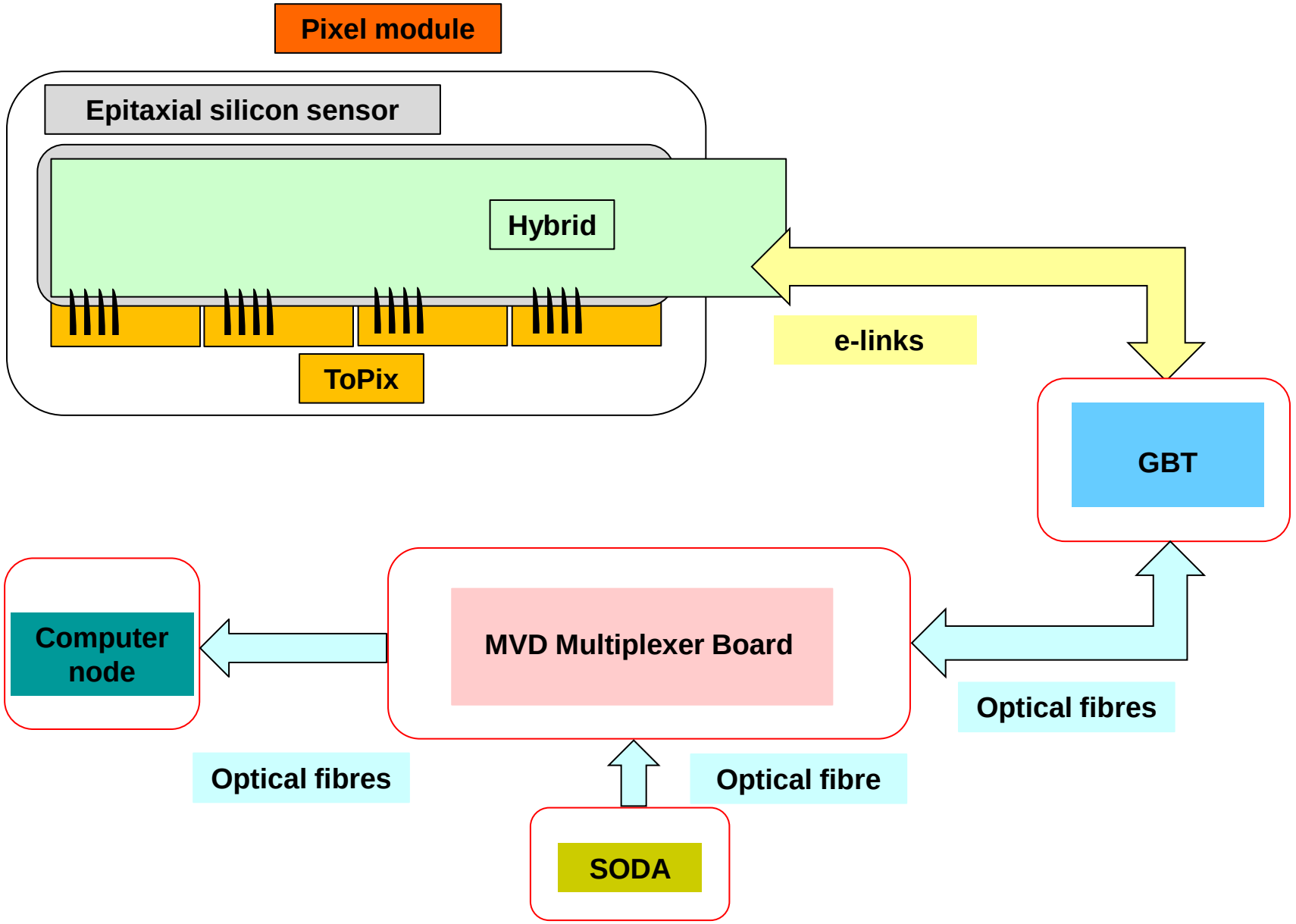
- Flex-PCB and 3.5 cm x 3.5 cm PANDA fullsize sensor (+APV25 chips)
- Trapezoidal sensors







Strip readout architecture



Pixel readout architecture