Electronics, Trigger and Data Acquisition

Summer Student Programme 2015, CERN

Part 3

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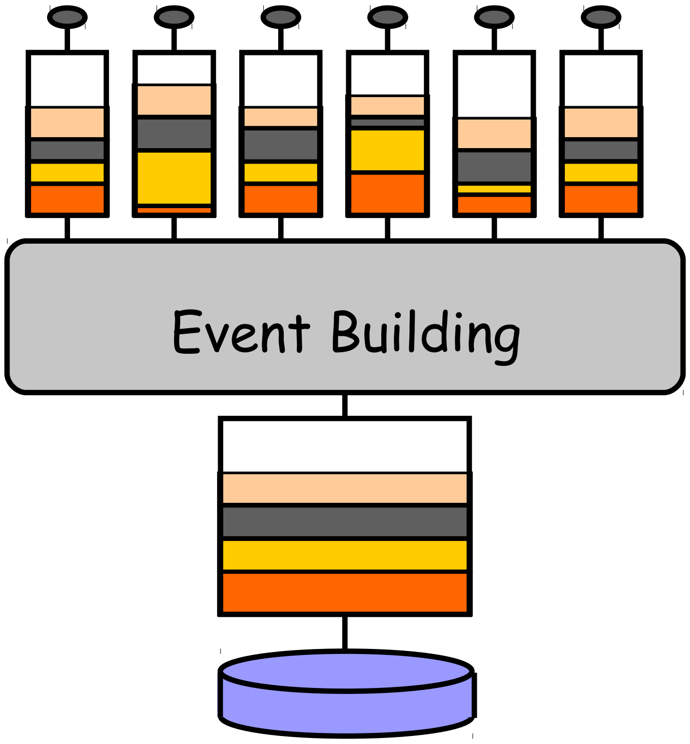
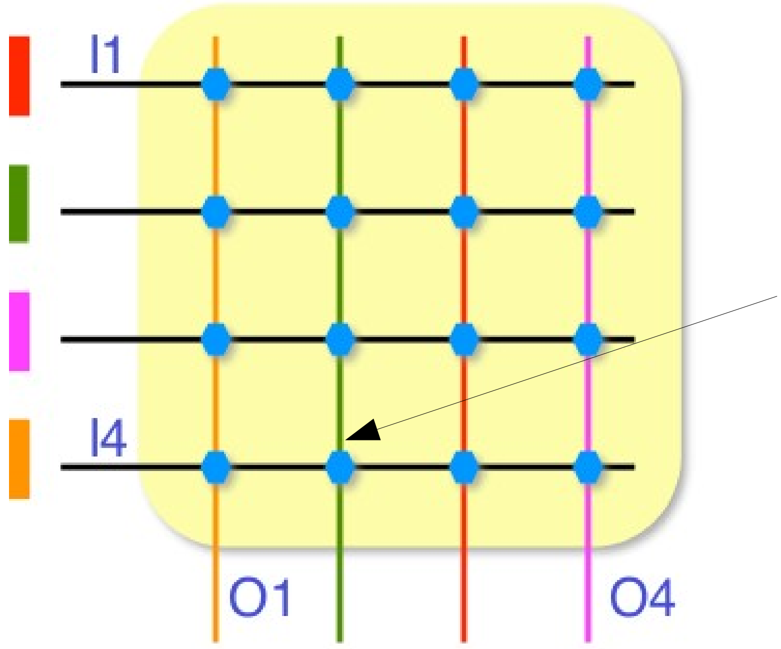
Event Building

Event Building: network perspective

- ➔ Event Building: collection and formatting of all the data elements of an event into a single unit
  - normally last step before high-level trigger or storage
  - can be implemented on buses, can use custom interconnects, can be based on (Ethernet) **network**
- ➔ Network-based EB is choice of all LHC experiments and a case study for networking in DAQ

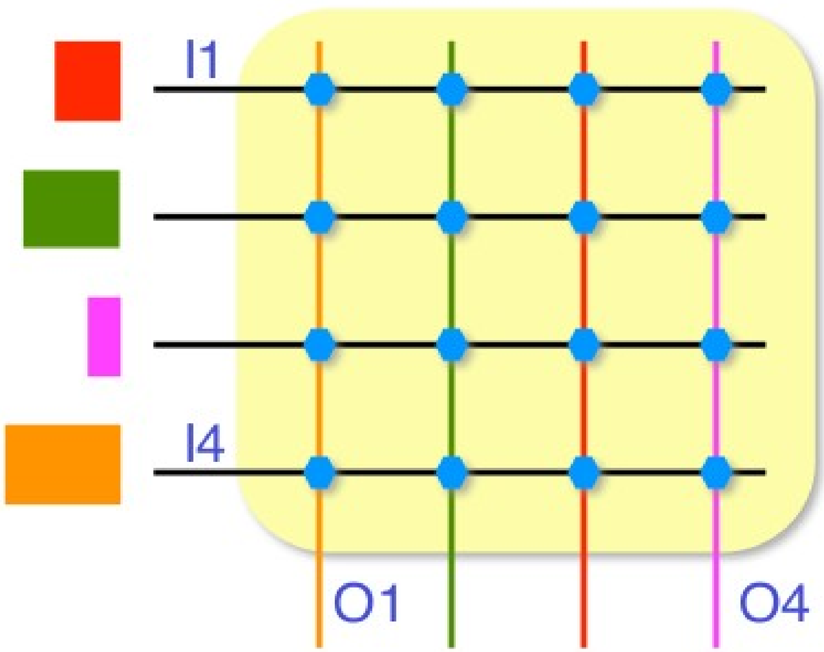


Network switch: crossbar



- ➔ Each input port can potentially be connected to each output port
- ➔ At any given time, only one input port can be connected to a given output port
- ➔ Different output ports can be reached concurrently by different input ports

Network switch: crossbar

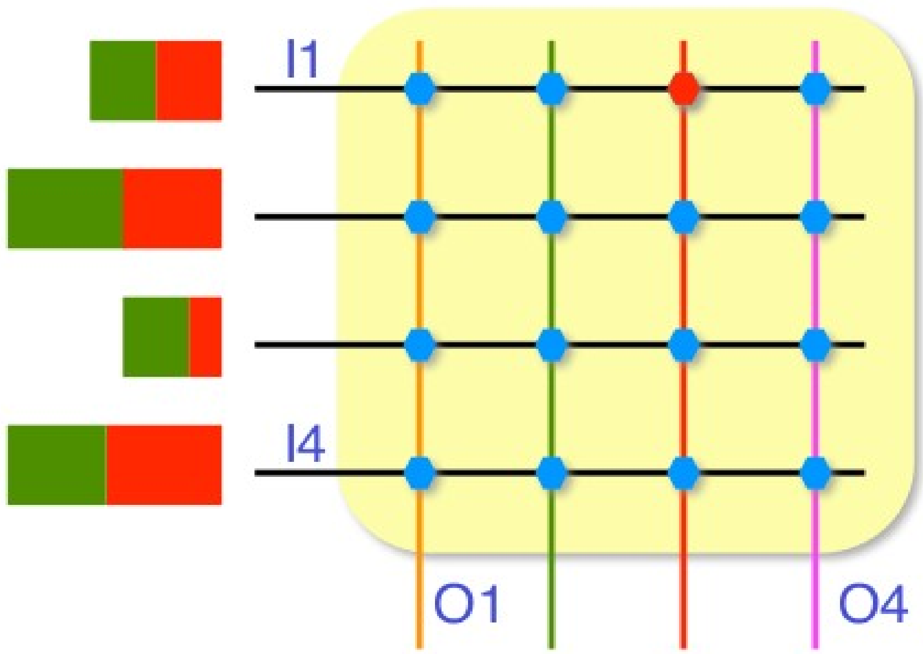


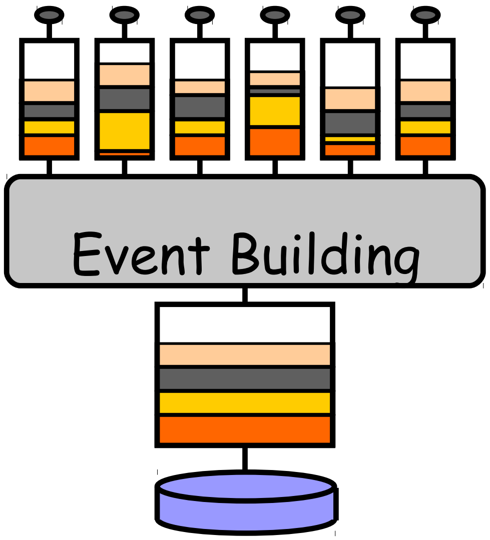
➔ Ideal situation → all inputs send data to different outputs

No interference (Congestion)

All input ports send data concurrently

Crossbar switch: event building





➔ EB workload implies converging data flow

- all inputs want to send to same destination **at the same time**

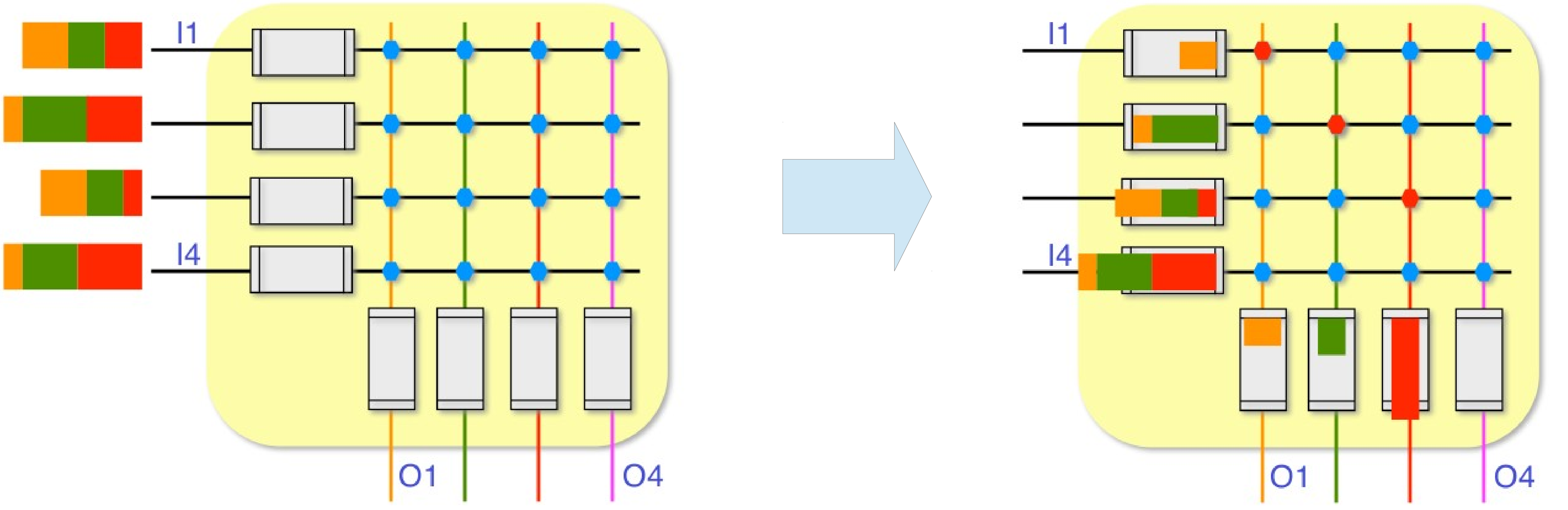
➔ "Head of line blocking"

- congestion

Congestion

- ➔ Well know phenomena ..
  - in Geneva and other cities
- ➔ Differently from road traffic, Ethernet HW is allow to “drop” packets
  - Higher level protocols have to take care of re-sending
  - Possibly important performance impacts

Queuing



→ Adding input and output FIFO dramatically improve the EB pattern handling

→ EB workload anyway problematic

- FIFO size is limited, variable data size
- limited internal switching speed

Traffic shaping
or
Network over-sizing

LHC experiments

Multi-level trigger systems

➔ Sometime impossible to take a proper decision in a single place

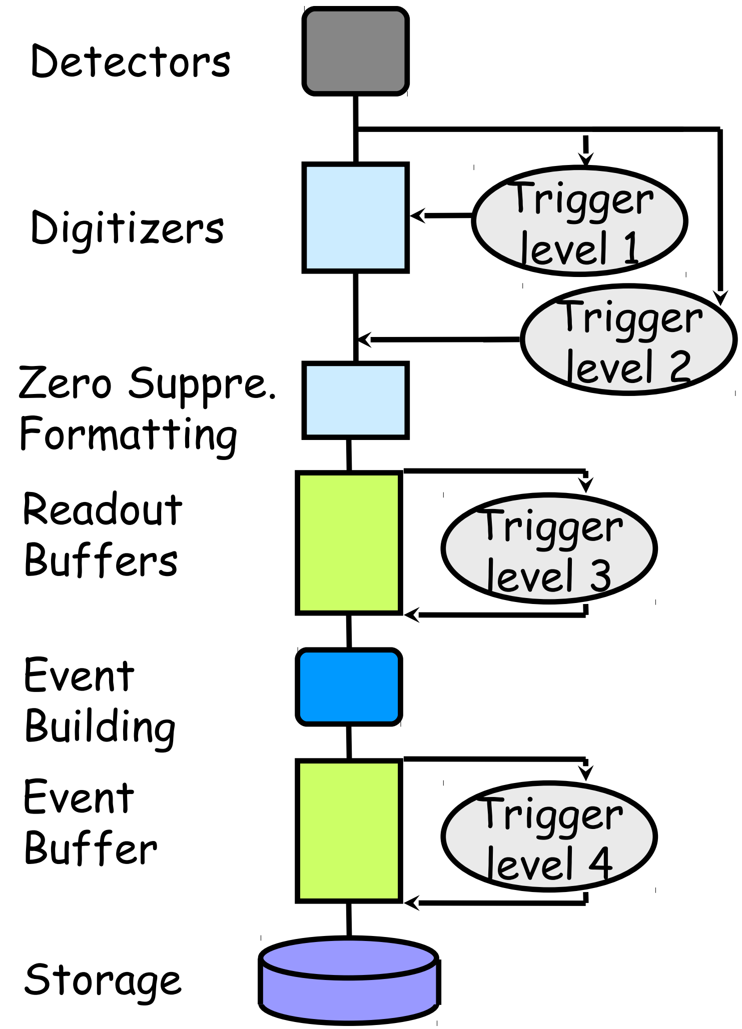
- too long decision time
- too far
- too many inputs

➔ Distribute the decision burden in a hierarchical structure

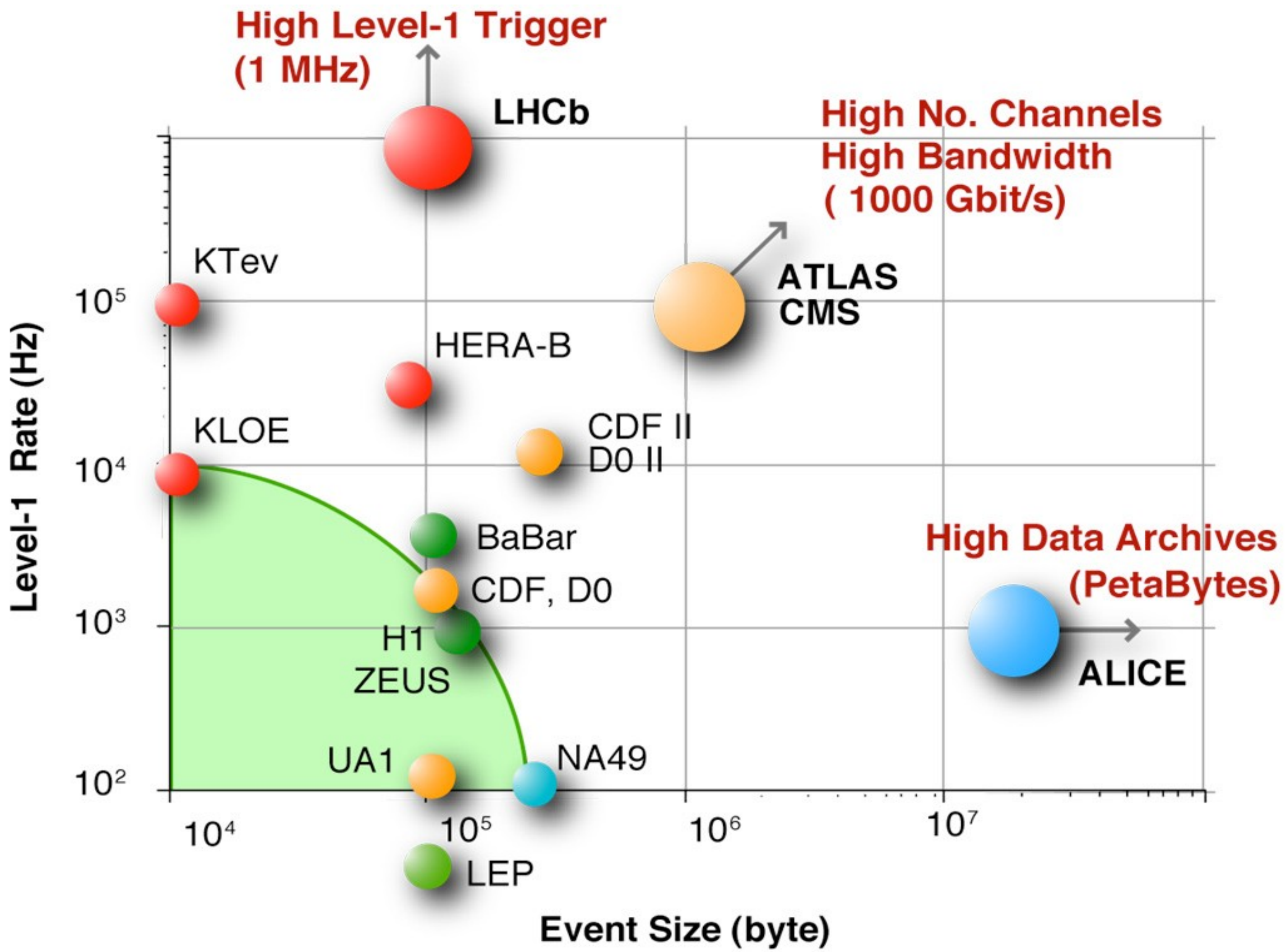
- usually $\tau_{N+1} \gg \tau_N \; , f_{N+1} \ll f_N$

➔ At the DAQ level, proper buffering must be provided for every trigger level

- absorb latency
- de-randomize



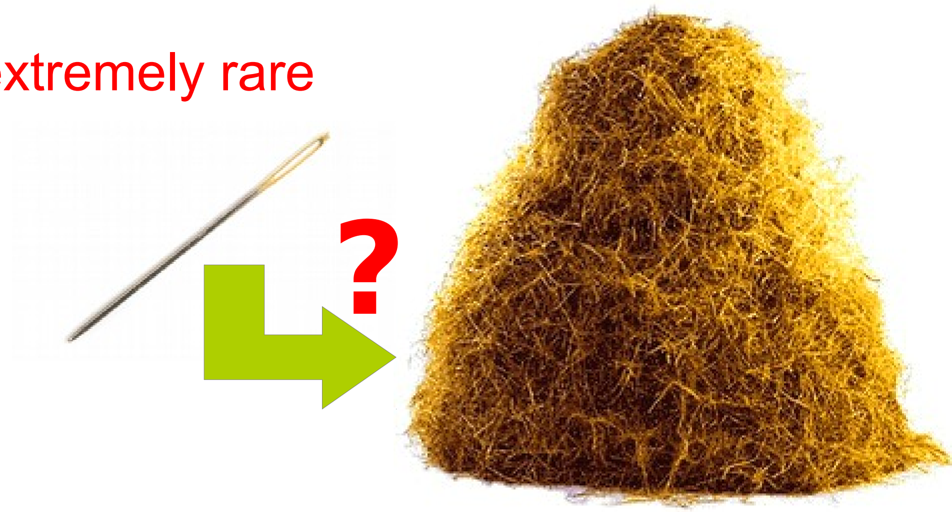
LHC DAQ phase-space



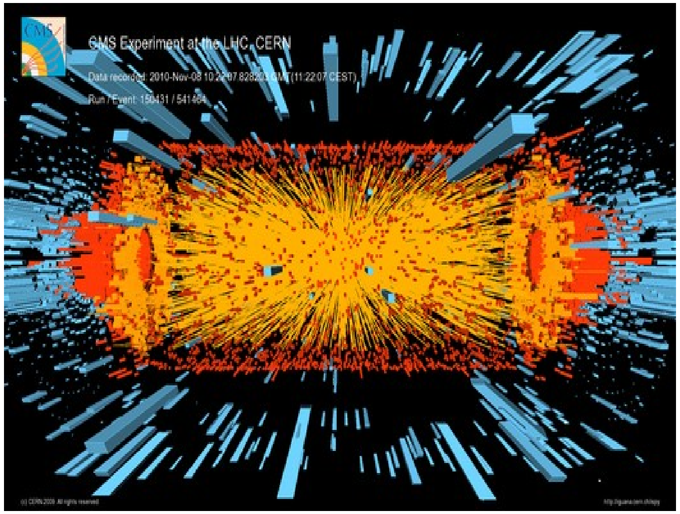
Trigger & DAQ Challenges at the LHC

- ➔ LHC experiments have $O(10^7)$ channels operating at 40 MHz (25 ns) → **40 TB/s**
- ➔ In addition, interesting phenomena are extremely rare

$$\sigma_H/\sigma_{Tot} \sim O(10^{-13})$$



- ➔ Events are complex
  - significant number of overlapping collisions (pile-up μ)
- ➔ Experiments are large (O(10 m))



Multi-level trigger system and …

LHC L1 Trigger and FE electronics

➔Particle time of flight >> 25 ns

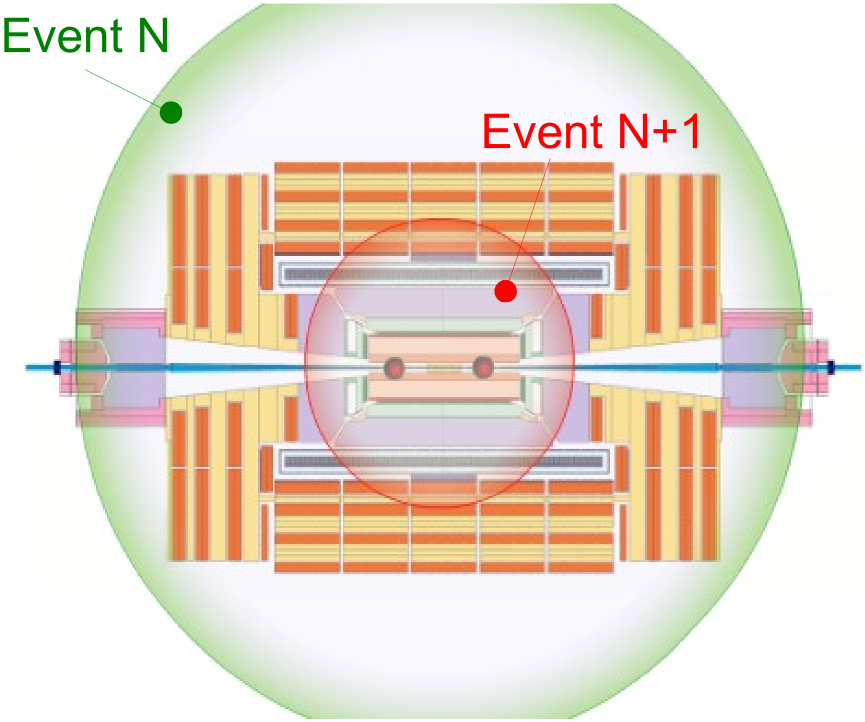
➔Cable delays >> 25 ns

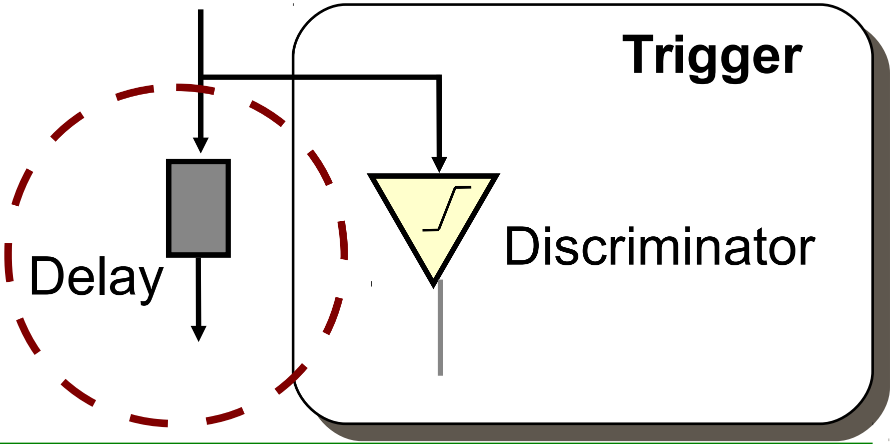
Dedicated synchronization, timing and signal distribution facilities

➔Typical L1 decision latency is O(μs)

- dominated by signal propagation in cables

Digital/analog custom front-end pipelines store information during L1 trigger decision

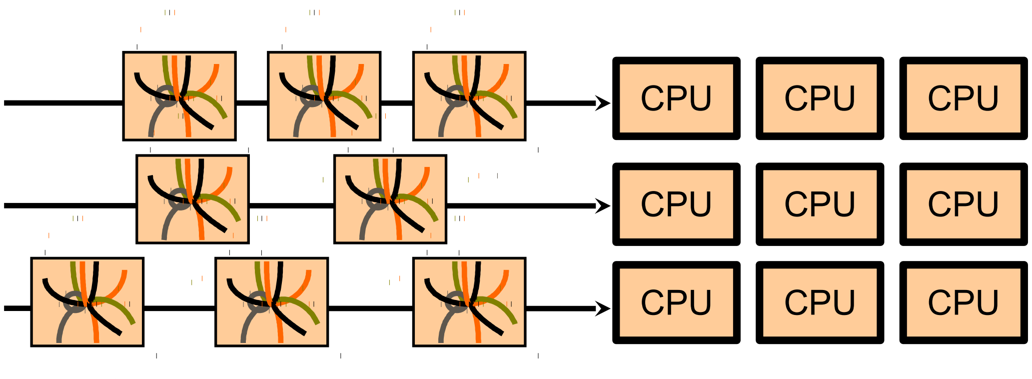




LHC: After L1?

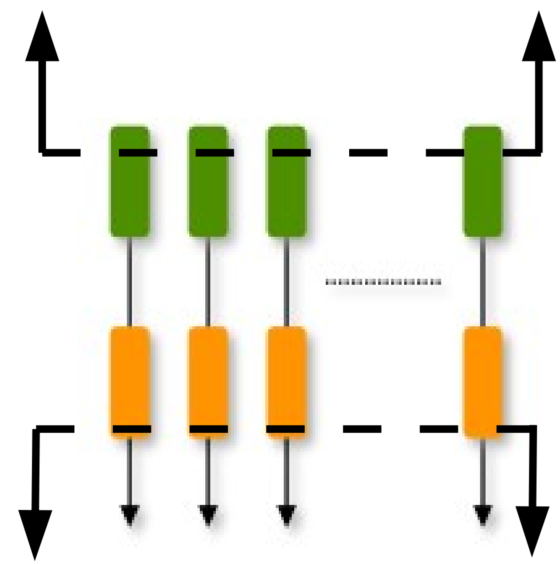
➔ Custom hardware L1 trigger and front-end electronics followed by network-based **High-Level Trigger** farm(s)

- commercially available HW organized in a farm
  - events are independent

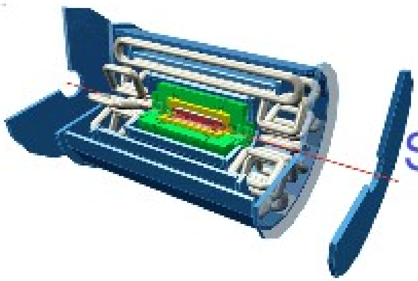
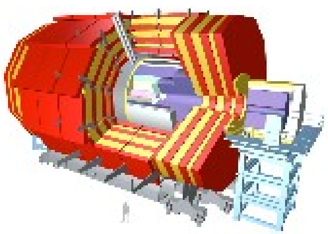
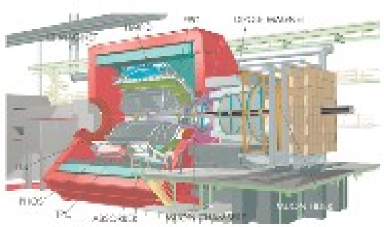
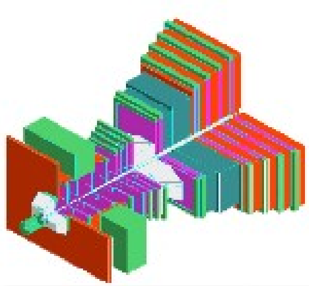


➔ Connection between custom section and the network-based one achieved via dedicated HW and point-to-point connectivity

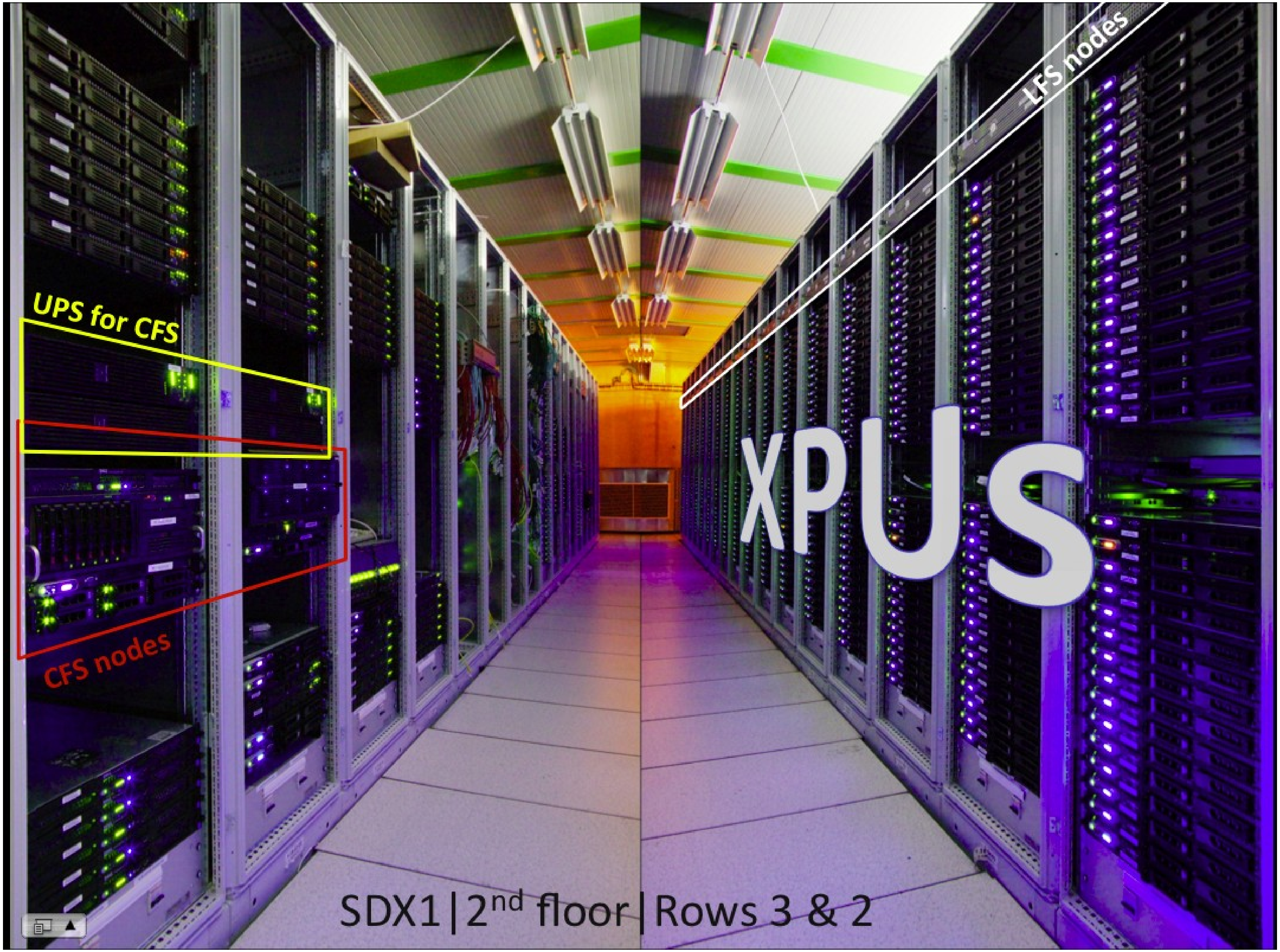
- electrical or optical, standard or custom



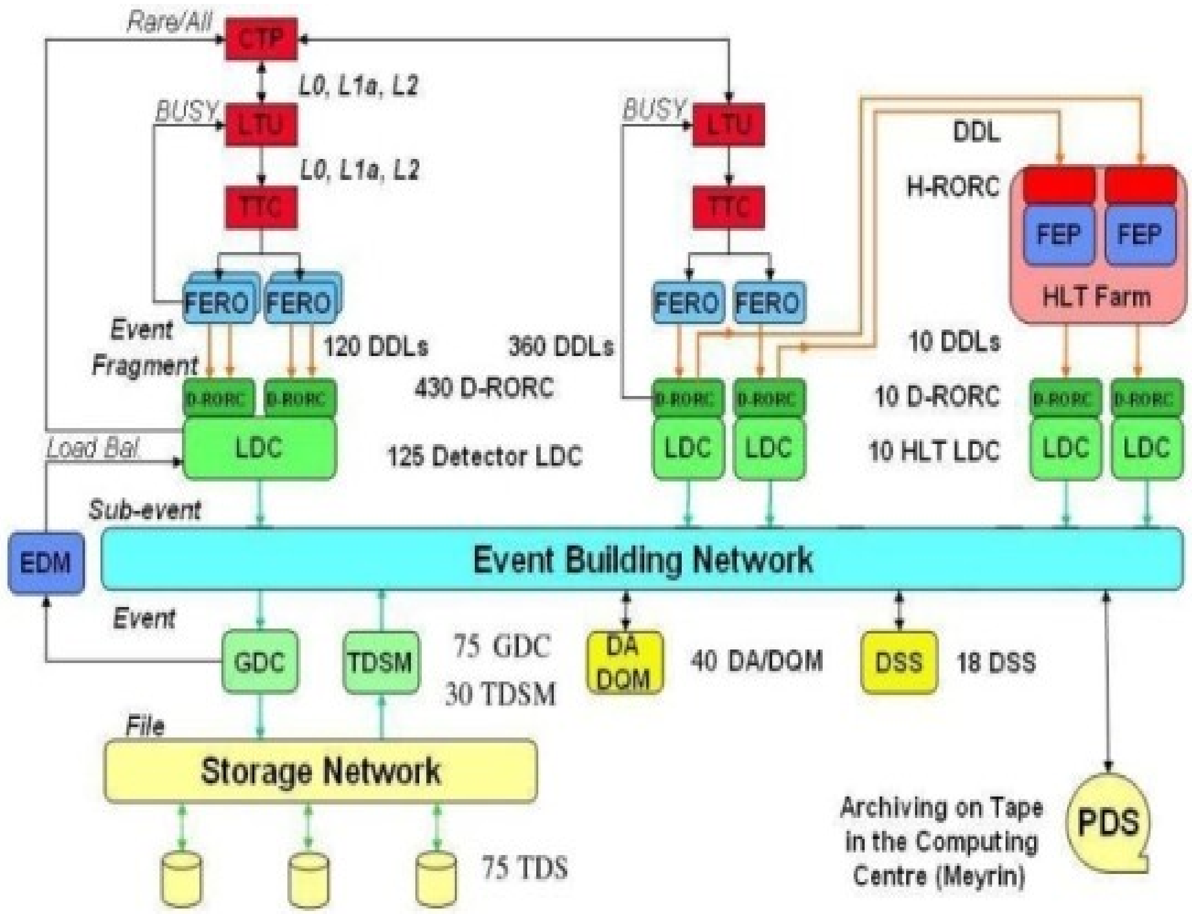
Read-out links at the LHC (in Run 1)

			Flow Control
	SLINK	Optical: 160 MB/s ≈ 1600 Links Receiver card interfaces to PC.	Yes
	SLINK 64	LVDS: 400 MB/s (max. 15m) ≈ 500 links (FE on average: 200 MB/s to readout buffer) Receiver card interfaces to commercial NIC (Network Interface Card)	yes
	DDL	Optical 200 MB/s ≈ 500 links Half duplex: Controls FE (commands, Pedestals,Calibration data) Receiver card interfaces to PC	yes
	TELL-1 & GbE Link	Copper quad GbE Link ≈ 400 links Protocol: IPv4 (direct connection to GbE switch) Forms “Multi Event Fragments” Implements readout buffer	no

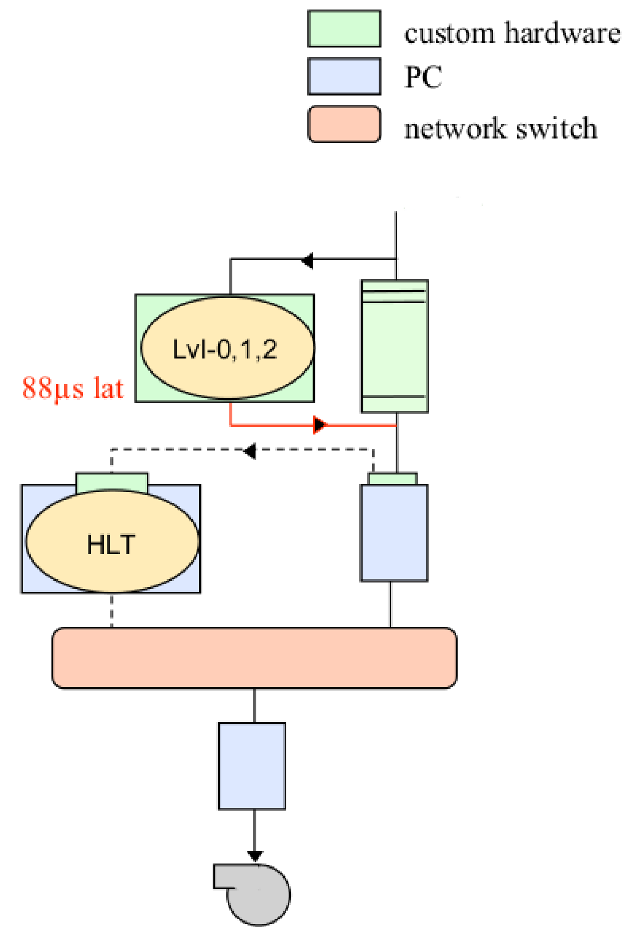
ATLAS HLT Farm



ALICE



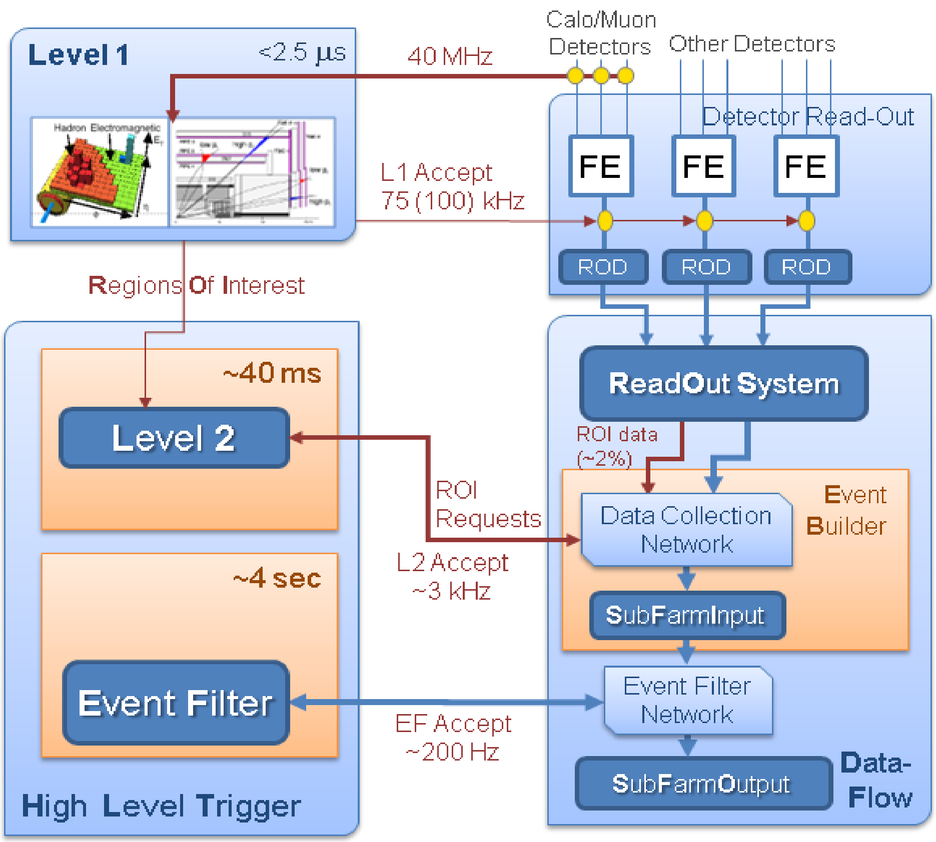
Rare/All
CTP
L0, L1a, L2
BUSY
LTU
L0, L1a, L2
TTC
BUSY
LTU
TTC
DDL
H-RORC
FEP
FEP
HLT Farm
FERO
FERO
FERO
FERO
Event
Fragment
120 DDLs
360 DDLs
10 DDLs
430 D-RORC
10 D-RORC
D-RORC
LDC
125 Detector LDC
10 HLT LDC
Load Bal.
Sub-event
EDM
Event Building Network
Event
GDC
TDSM
75 GDC
30 TDSM
DA
DQM
40 DA/DQM
DSS
18 DSS
File
Storage Network
75 TDS
Archiving on Tape
in the Computing
Centre (Meyrin)
PDS

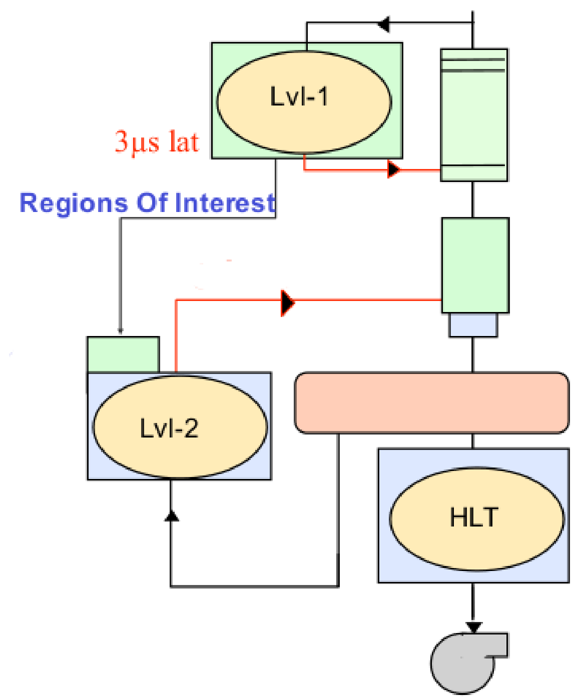


custom hardware
PC
network switch
88μs lat
Lvl-0,1,2
HLT

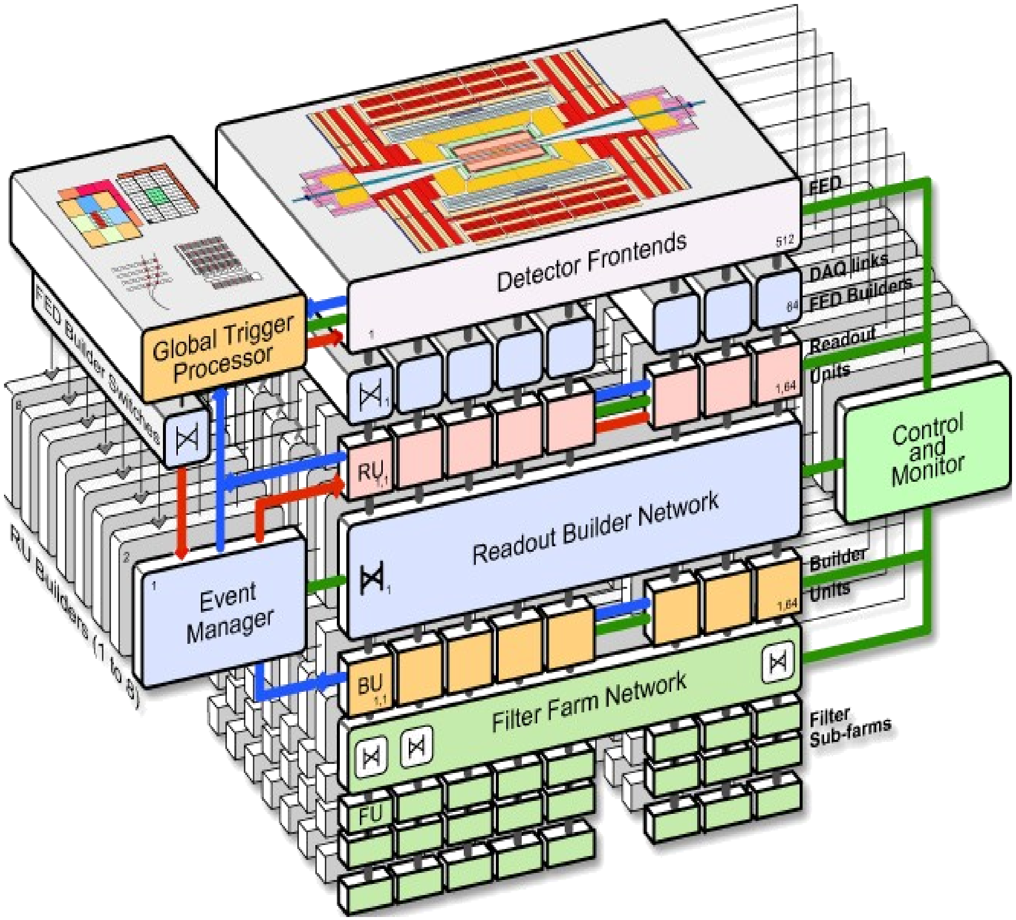
ATLAS

custom hardware
PC
network switch

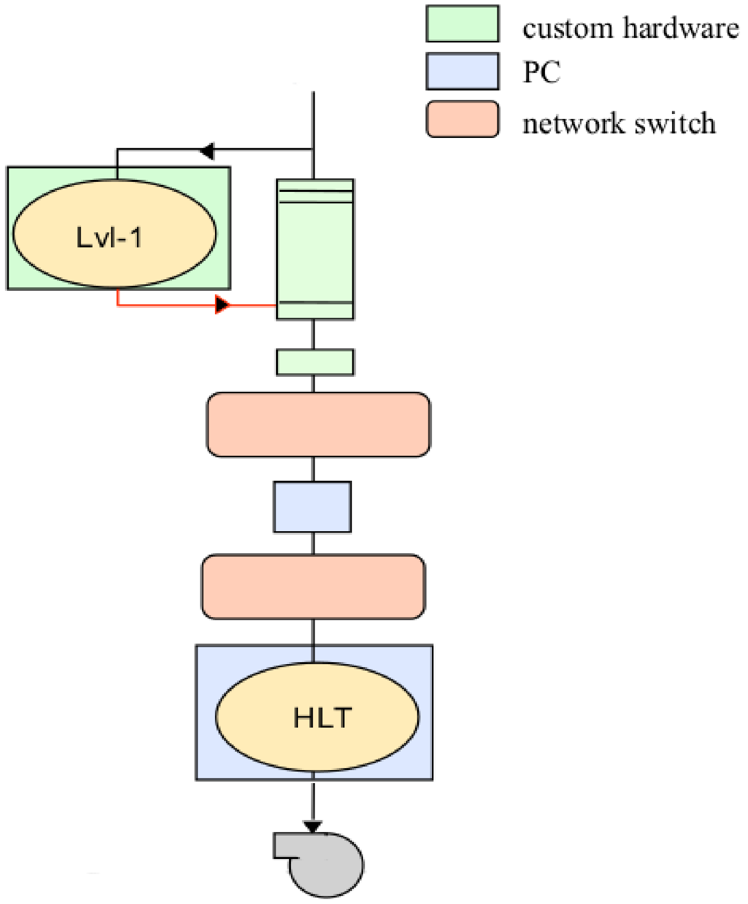




CMS

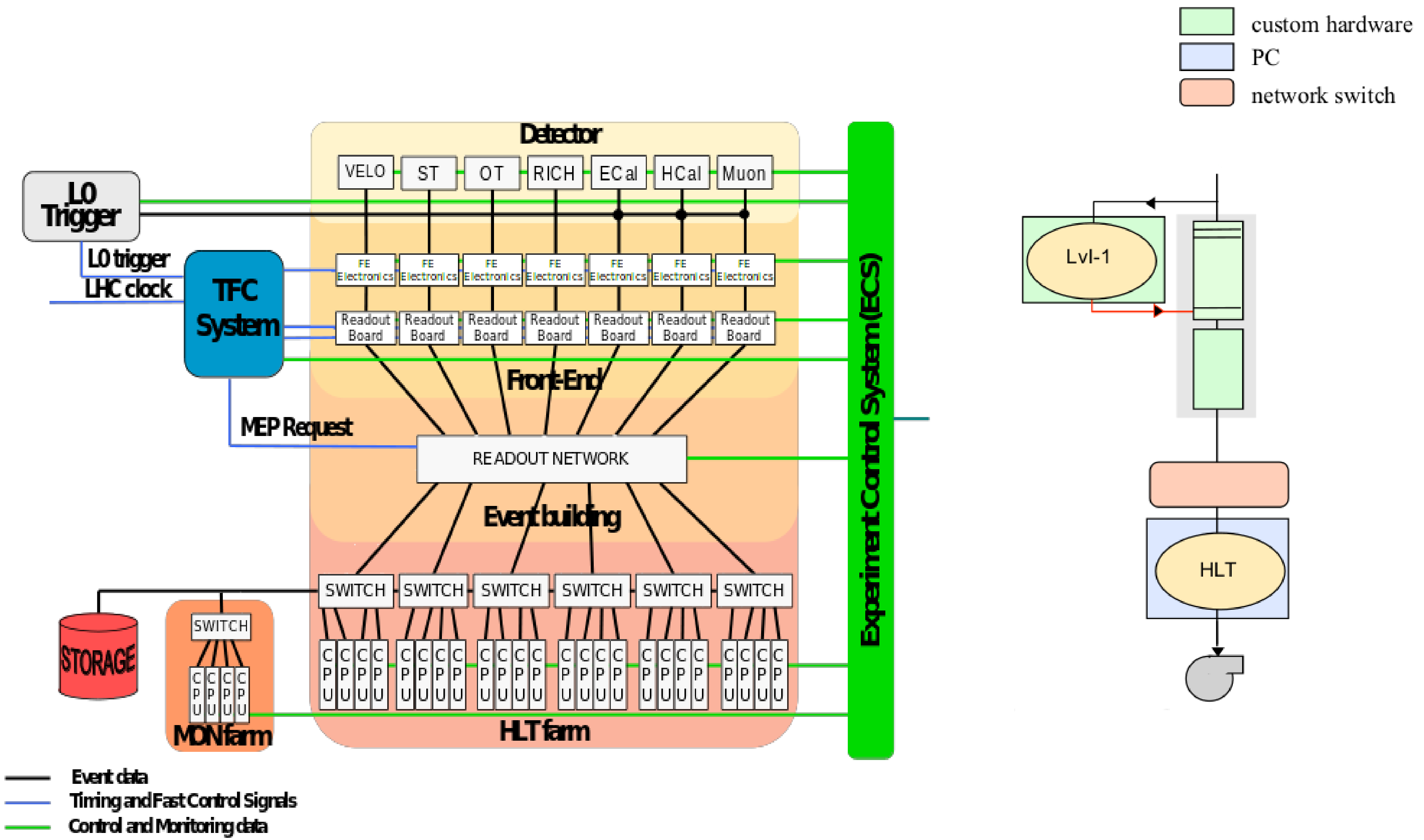


Detector Frontends
Global Trigger Processor
FED Builder Switches
FED
DAQ links
FED Builders
Readout Units
RU
Readout Builder Network
Control and Monitor
Event Manager
RU Builders (1 to 8)
Builder Units
BU
Filter Farm Network
Filter Sub-farms
FU

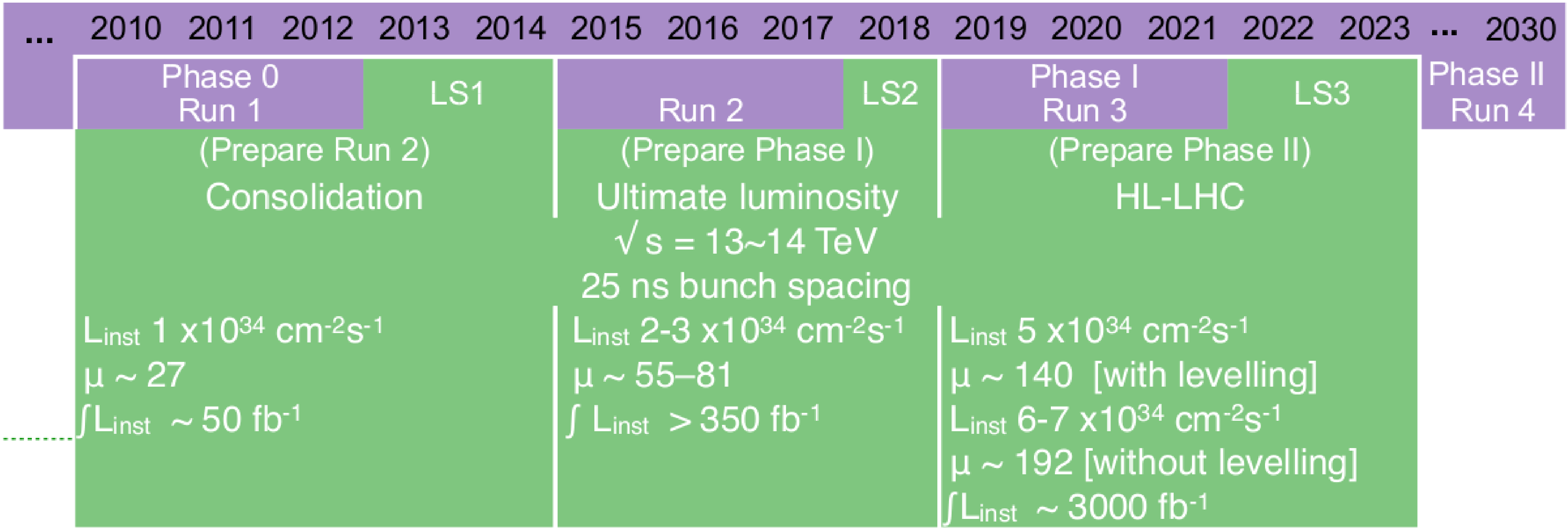


custom hardware
PC
network switch
Lvl-1
HLT

LHCb


custom hardware
PC
network switch
Detector
VELO
ST
OT
RICH
ECal
HCal
Muon
L0 Trigger
L0 trigger
LHC clock
TFC System
FE Electronics
Readout Board
Front-End
MEP Request
READOUT NETWORK
Event building
SWITCH
CPU
STORAGE
MON farm
HLT farm
Experiment Control System (ECS)
Event data
Timing and Fast Control Signals
Control and Monitoring data
Lvl-1
HLT

Long Shutdown 1: TDAQ Perspective



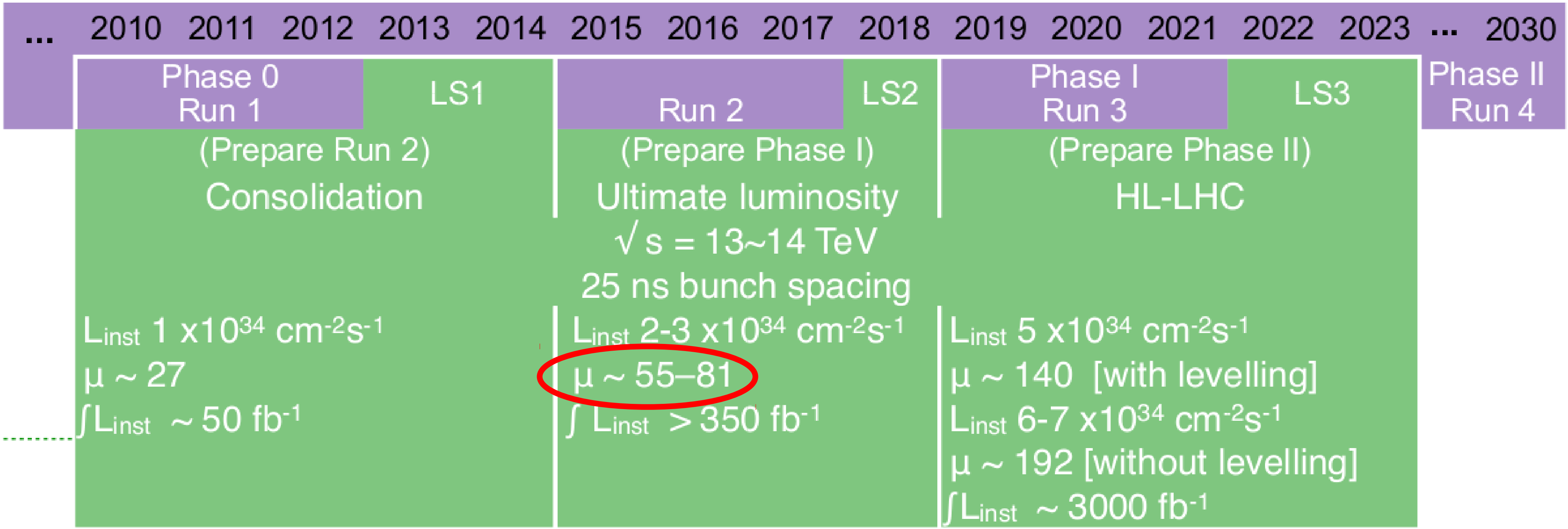
➔ LHC data-acquisition system backbones installed ~2007

- during Run 1 → stability, efficiency, performance reach and optimization

➔ LS1 was occasion to

- upgrade core systems and review architectures
- introduce new technologies, retire obsolete ones
- follow changes on the detector side
- prepare for challenges of Run2 (and Run3)

Long Shutdown 1: TDAQ Perspective



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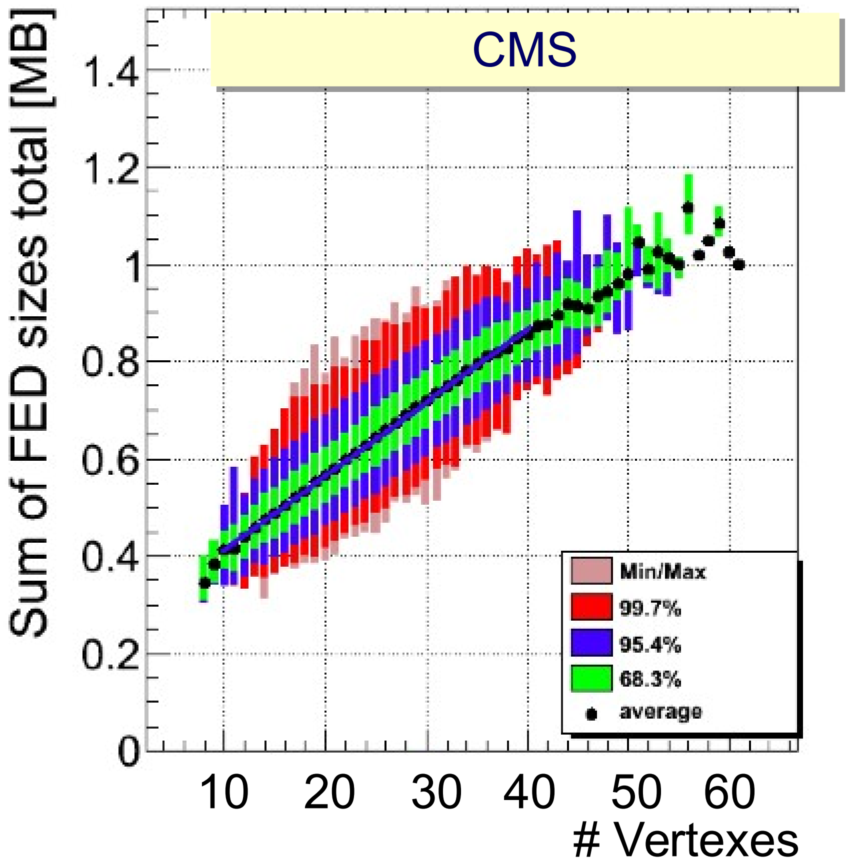
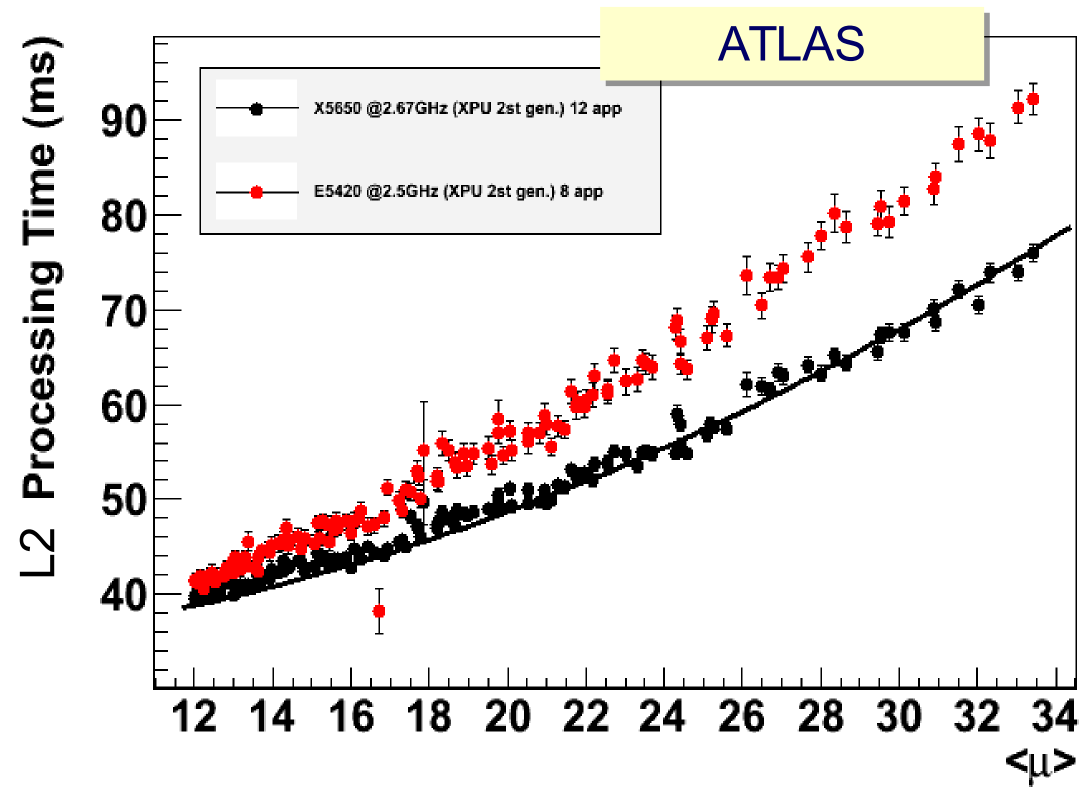
Run 2: Challenges

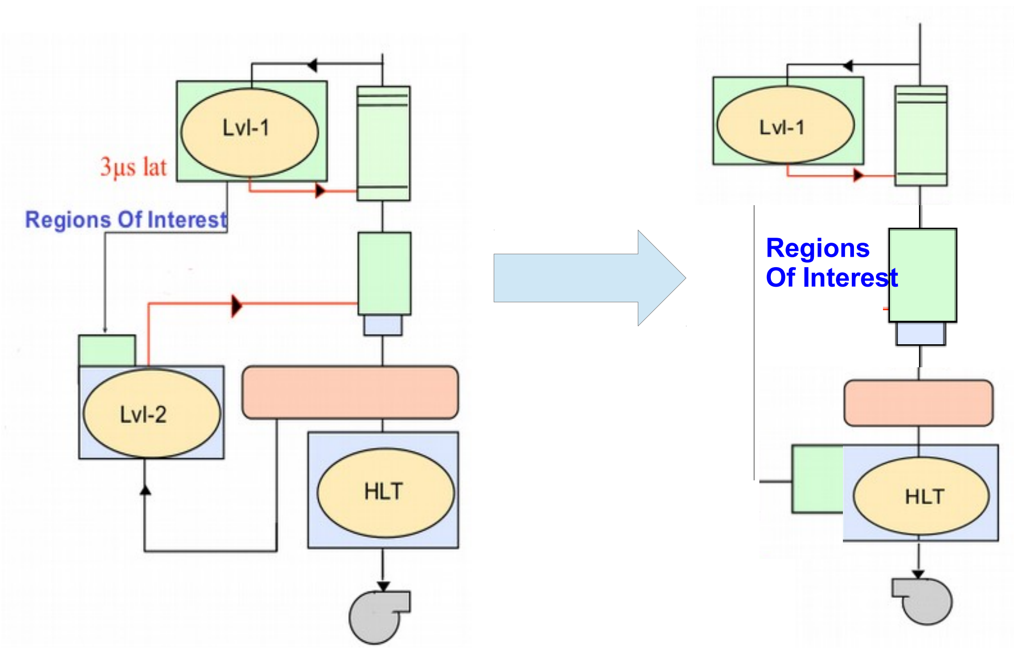
➔ Increased pile-up

- larger data size → bandwidth and storage
- more complex events → increased computing needs, trigger efficiency and rejection power



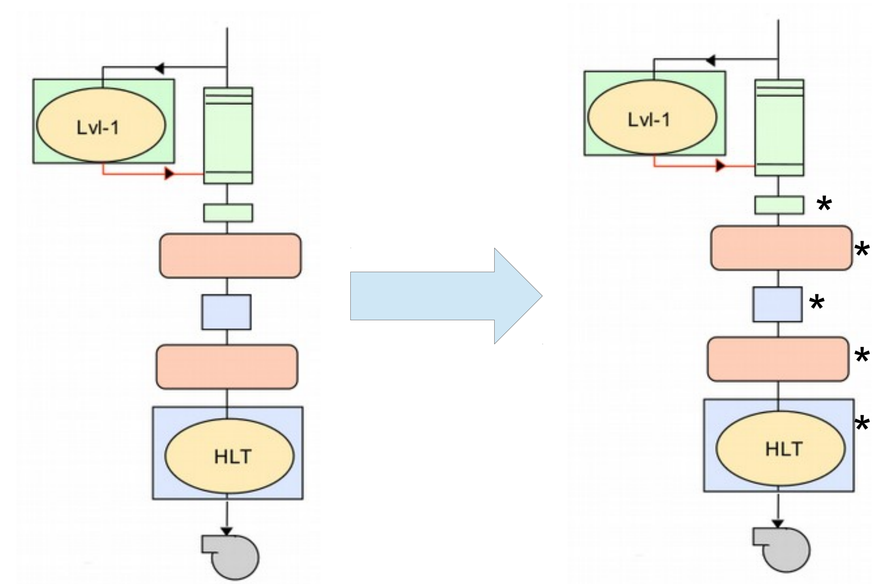


(Some) Run 2 updates



➔ Merge L2 and L3 into a single HLT farm

- preserve Region of Interest, but diluted the farm separation and fragmentation
- increased flexibly, computing power efficiency



➔ No architectural changes, but

- all network technologies replaced
  - Myrinet → Ethernet
  - Ethernet → Infiniband
- file-based event distribution in the farm
  - achieve full decoupling between DAQ and HLT

Looking forward to LS2 and beyond

DAQ@LHC Workshop

On the long term, all experiments looking forward to significant increase in L1 trigger rate and bandwidth. ALICE and LHCb will pioneer this path during LS2

- ➔ First level trigger for Pb-Pb interactions **500 Hz** → **50 kHz**
- ➔ 22 MB/event
  - **1 TB/s readout** → **<u>500 PB/month</u>**
- ➔ Data volume reduction
  - on-line full reconstruction
  - discard raw-data
- ➔ Combined DAQ/HLT/offline farm
  - COTS, FPGA and GPGPU

- ➔ **1 MHz** → **40 MHz** readout and event building → trigger-less
  - trigger support for staged computing power deployment
- ➔ 100 kB/event
  - on-detector zero suppression → rad-hard FPGA
  - 4 TB/s event-building

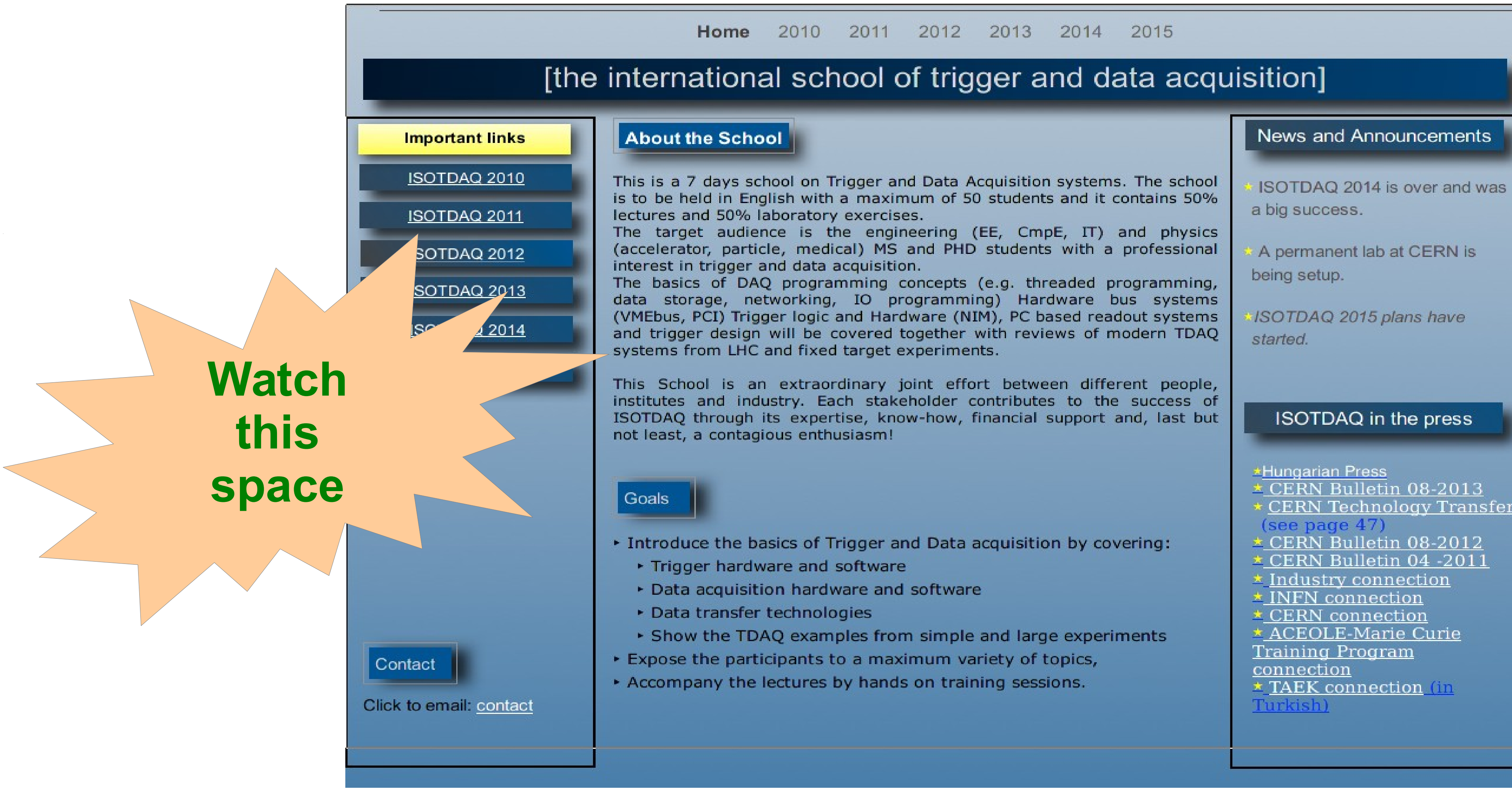
Almost The End

What I did not talk about …

- ➔ Many many topics
  - Run Control → Steering the DAQ, Finite State Machine
  - Configuration → Storing, distributing and archiving SW, HW and trigger configuration
  - Monitoring → The quality of the data, the state of the detector, the functionality of the DAQ

➔ Your chance of hearing about these and much more and learn through practice …

➔ Sixth edition of the **International School of Trigger and Data Acquisition** will be held in February 2016 and hosted by Weizmann Institute



http://isotdaq.web.cern.ch/isotdaq/isotdaq/Home.html

The End

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References

- ➔ Lectures and papers from H. Spieler
  - http://www-physics.lbl.gov/~spieler/
- ➔ Lecture at ISOTDAQ schools
  - http://isotdaq.web.cern.ch/isotdaq/isotdaq/Home.html
- ➔ Of course, previous Summer Student courses
  - http://indico.cern.ch/scripts/SSLPdisplay.py?stdate=2011-07-04&nbweeks=7
- ➔ DAQ@LHC Workshop
  - http://indico.cern.ch/scripts/SSLPdisplay.py?stdate=2011-07-04&nbweeks=7

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