A new read-out architecture for the ATLAS Tile Calorimeter Phase-II Upgrade

Alberto Valero, on behalf of the ATLAS Tile Calorimeter System
Instituto de Física Corpuscular (CSIC - UV)

THE ATLAS TILE CALORIMETER PHASE-II UPGRADE

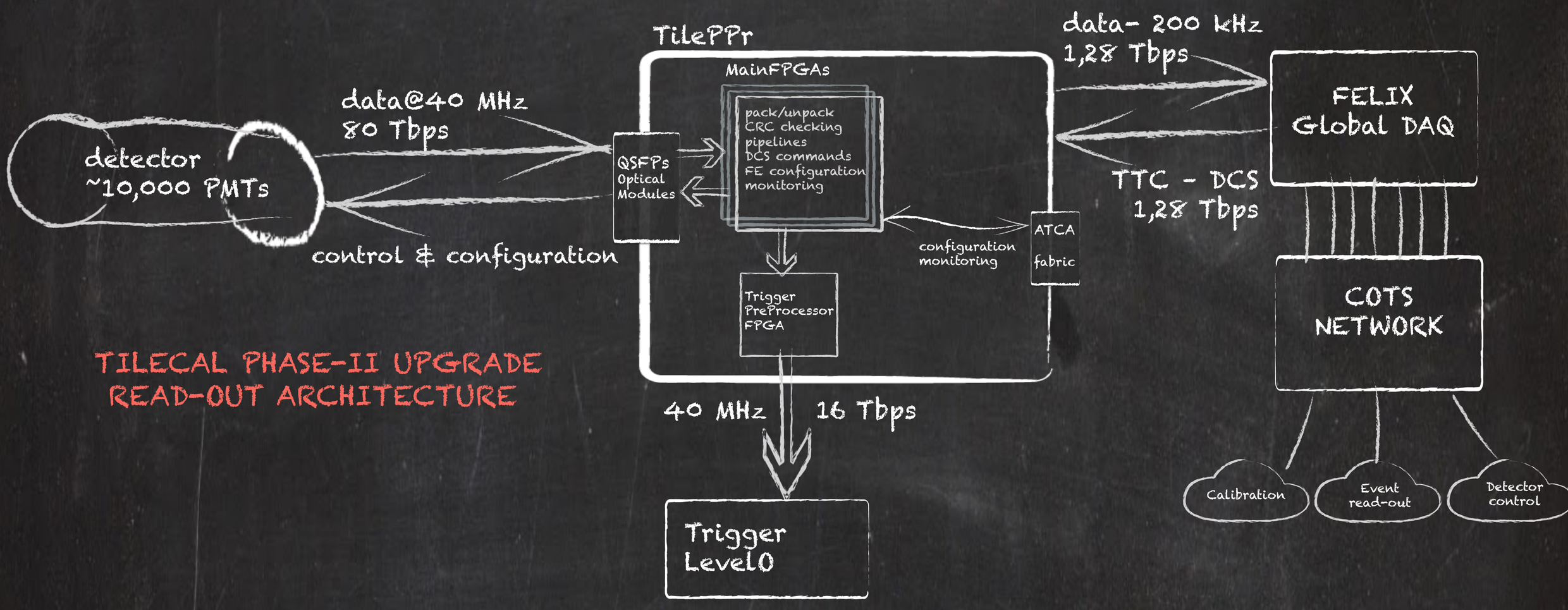
TileCal is the Tile hadronic calorimeter of the ATLAS experiment at the LHC. TileCal is an iron-scintillating sampling detector which is read-out by 9852 photomultiplier tubes (PMTs). The PMT signals are digitized with a 40 MHz clock which is synchronous with the beam crossing. The digital samples are stored in pipeline memories during the Level 1 (L1) trigger latency (2.5 us). Simultaneously, the PMT analog signals are grouped and transmitted to the Level 1 Calorimeter system. The digital samples of the events selected by the Level 1 trigger system are transmitted to the Read-Out Drivers (RODs) located in the back-end system at a maximum average rate of 100 kHz.

The LHC has planned a series of upgrades culminating in the High Luminosity LHC (HL-LHC) which will increase of order five times the LHC nominal instantaneous luminosity. TileCal will undergo an upgrade to accommodate to the HL-LHC parameters. The TileCal read-out electronics will be redesigned introducing a new read-out strategy. The data generated in the detector will be transferred to the PreProcessors (TilePPr) located in off-detector (up link) for every bunch crossing before any event selection is applied. Furthermore, the TilePPr will be responsible of providing preprocessed digital trigger information to the ATLAS Level 0 trigger. In addition, the TilePPr system will implement pipeline memories to cope with the latencies and rates specified in the new trigger schema and in overall it will represent the interface between the data acquisition, trigger and control systems and the on-detector electronics.

TILECAL READ-OUT SYSTEM

Up Link only	Present	Upgrade
Total BW	~ 165 Gbps	~80 Tbps
Nb fibers	256	8192
Fiber BW	640 Mbps	10 Gbps
Nb boards	32	32
Nb crates	4 (VME)	4 (ATCA)
In BW/board	5 Gbps	2,5 Tbps
Out BW/board $_{DAQ}$	2,56 Gbps	40 Gbps
Out BW/board $_{L1}$	Analog FE	500 Gbps

TILECAL PHASE-II UPGRADE READ-OUT ARCHITECTURE

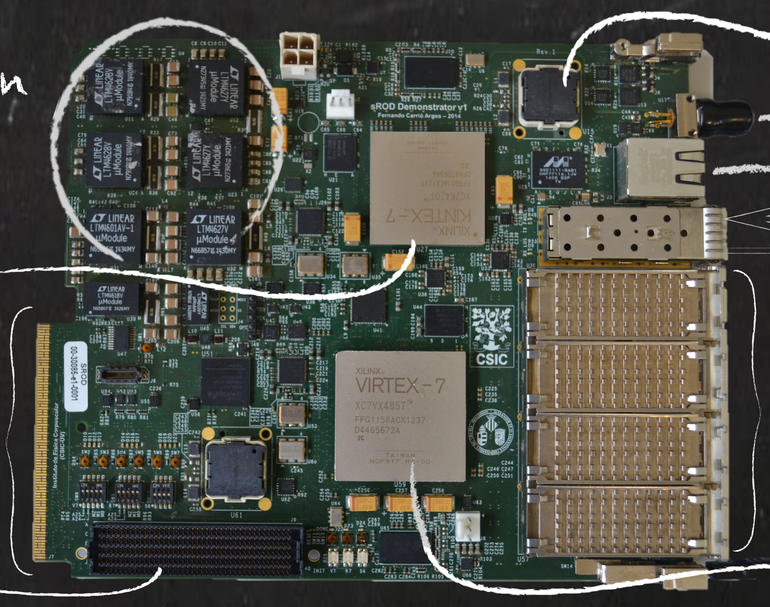


THE TILE PREPROCESSOR DEMONSTRATOR

TileCal has built a demonstrator prototype to evaluate the new electronics and the proposed read-out architecture for Phase-II upgrade. The demonstrator will be evaluated in various test-beam campaigns during 2015-2016 and it will be inserted in the ATLAS detector for data taking at the end of 2016. A PPr prototype has been designed to operate one TileCal demonstrator module which represents 1/8 of the final PPr module. Four QSFP optical modules provide the interface with the front-end electronics. The links data are managed from a Virtex7 *MainFPGA* which implements the communication protocol (GBT) with the front-end, packs and unpacks the data and commands, stores the detector in pipelines memories, receives and decodes legacy TTC information and provides communication with the old ROD system. A second Kintex7 PPrFPGA pre-process and transmits the data to the trigger system through a Parallel Optical Device (POD). The board has a standard double-mid size AMC format and can be operated in an ATCA/uATCA framework which provides power and ethernet communication with both FPGAs for control and monitoring purposes. Power and RJ45 ethernet connectors are included to operate the module in standalone mode. The first two modules have been produced and are fully operative.

Layout and PCB

- Dimensions: 180.6×148.5 mm
- 16 layers - 1200 components
- 8 power/GND planes - 8 signals
- Dielectric NELCO 4000-13 SI



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