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on behalf of the ATLAS-ALFA and TOTEM Roman Pot Teams

with special thanks to Collimation WG, LHC interlock team, Operators, PH-DT, EN-ICE

MPP Meeting 24 April 2015

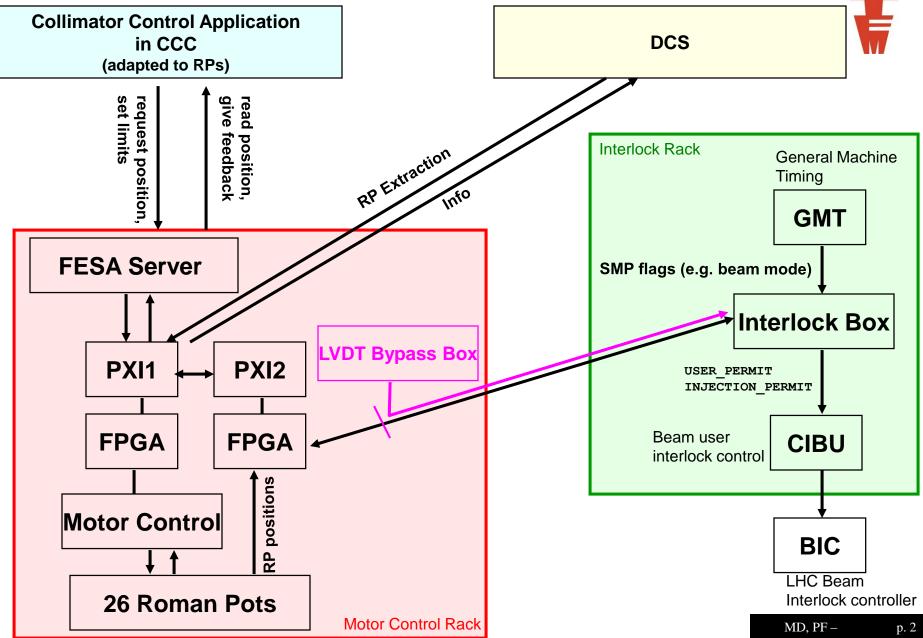
summarising EDMS 1503866 (ALFA) EDMS 1501228 (TOTEM)

Movement System Architecture (strongly simplified)

ERIMENT

http://atlas.ch







Simplified Interlock Functionality

• User Permits (1 per beam):

User Permit is removed if:

(a pot is outside garage in the wrong beam mode) or (a pot is not within position limits) \rightarrow beam dump and retraction of all RPs with the springs

• Injection Permits (1 per beam):

Injection Permit is removed if a pot is outside garage (defined by electrical link from HOME switch)

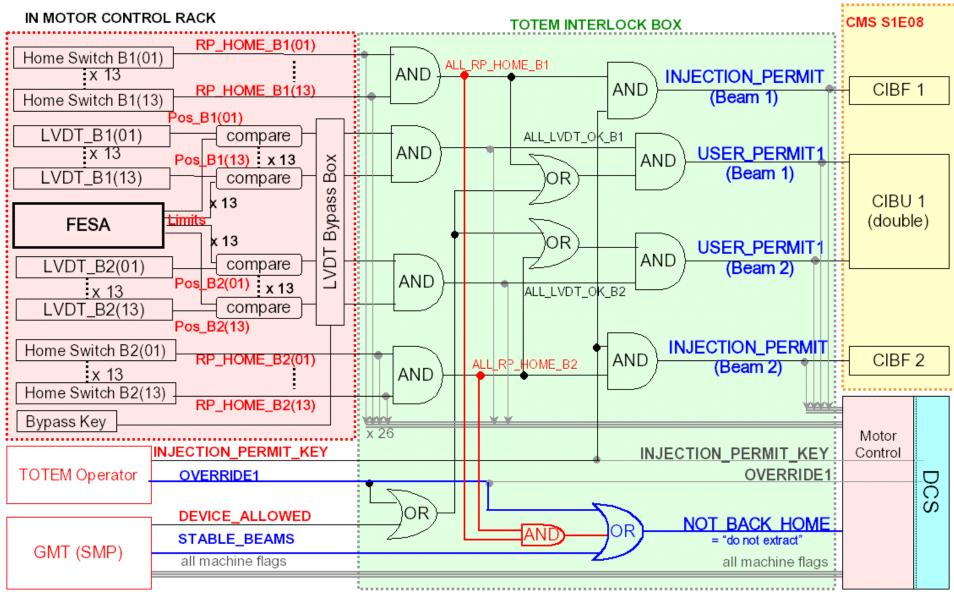
... apart from an Override key and an LVDT bypass key (consult the full logic)

Logic implemented on a programmable circuit ("Interlock Box")

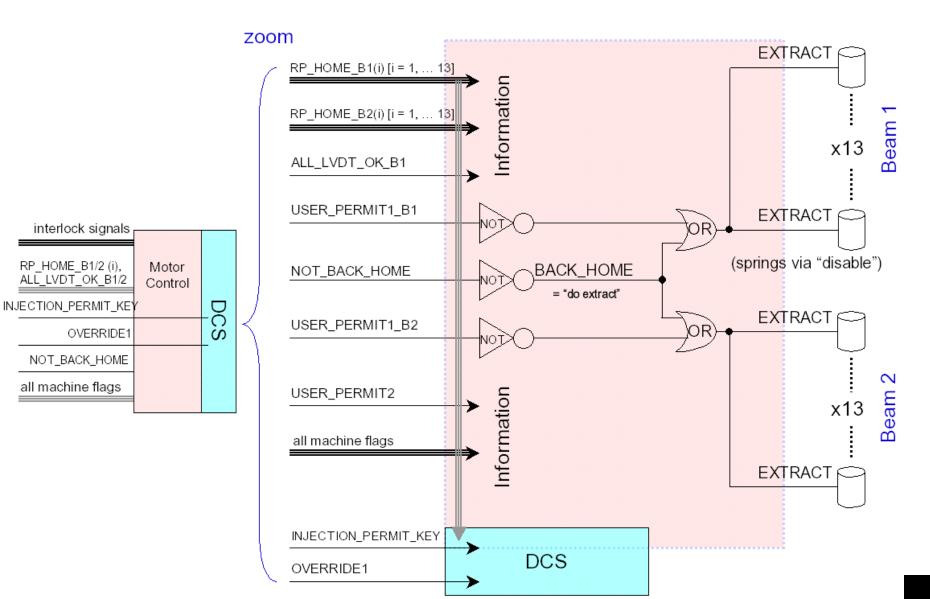
New in 2015:

- Separation of active movement control and position interlock functionalities: 2 PXI computers
- TOTEM: addition of 2 single horizontal pots, now total of 26 pots
 - \rightarrow interlock box circuit board completely redone (allows for up to 32 pots!)
- But: logic unchanged !

Interlock Logic 2015



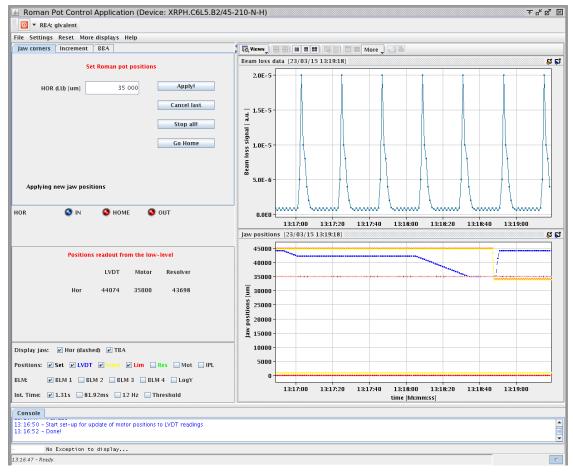
Interlock Logic 2015 (Zoom on the motor control)





Top Level Control (Collimator Application in the CCC)

- developed and maintained by G. Valentino (BE-ABP)
- strongly improved during LS1:
 - * all limits displayed (now also new inner limits)
 - * nomenclature of switches corrected
 - * preview line before applying a movement command







Test Strategy



ALFA Interlock validation test 4 test sequences:

1. Injection Permits

- Rest of ATLAS was at "Ready for injection" (including injection key)
- Then ALFA breaks the injection permit by moving in a Roman Pot.
- Done for all 8 pots

2. Beam mode test

- Test of ALFA reaction vs Beam Modes and "moveable devices allowed"
- About 1 hour needed for each beam.
- All worked as expected.
- Done for one pot per beam.

3. Systematic check of limits (old/new inner limits)

- A few errors found and corrected.
- Final validation made on all Roman Pots with final firmware.
- Done separately for each beam, all pots.

4. LVDT bypass key see EDMS 1203969

- Test of key reactions in case of hardware failure (to allow LHC operation).
- All worked as expected



Beam-Mode Dependent Test Sequence



Innuto	1	Comb	oinations to	be tested	(labelled by th	ie smali biue n	umber <u>ş</u>)	6
Inputs	1	2	3	4			Э	D
ALL_LVDT_OK_Bi	1	1	1	1	1	1	1	1
ALL_RP_HOME_Bi	1	1	1	1	1	1	1	1
DEVICE_ALLOWED	1	1	1	1	0	0	0	0
STABLE_BEAMS	1	1	0	0	1	1	0	0
OVERRIDE1	1	0	1	0	1	0	1	0
USER_PERMIT1(Bi)	1	1	1	1	N/A	N/A	1	1
EXTRACT	0	0	0	0	N/A	N/A	0	0
	_							
Inputs	7	8	9	10			11	12
ALL_LVDT_OK_Bi	1	1	1	1	1	1	1	1
ALL_RP_HOME_Bi	0	0	0	0	0	0	0	0
DEVICE_ALLOWED	1	1	1	1	0	0	0	0
STABLE_BEAM	1	1	0	0	1	1	0	0
OVERRIDE1	1	0	1	0	1	0	1	0
USER_PERMIT1(Bi)	1	1	1	1	N/A	N/A	1	0
EXTRACT	0	0	0	1	N/A	N/A	0	1
Inputs	13	14	15	16			17	18
ALL_LVDT_OK_Bi	0	0	0	0	0	0	0	0
ALL_RP_HOME_Bi	1	1	1	1	1	1	1	1
DEVICE_ALLOWED	1	1	1	1	0	0	0	0
STABLE_BEAM	1	1	0	0	1	1	0	0
OVERRIDE1	1	0	1	0	1	0	1	0
USER_PERMIT1(Bi)	0	0	0	0	N/A	N/A	0	0
EXTRACT	1	1	1	1	N/A	N/A	1	1
	_							
Inputs	19	20	21	22			23	24
ALL_LVDT_OK_Bi	0	0	0	0	0	0	0	0
ALL_RP_HOME_Bi	0	0	0	0	0	0	0	0

5 input signals $\rightarrow 2^5 = 32$ combinations

Test sequence = optimised path reaching each of the conditions (input combinations; blue numbers) at least once.

Inputs	19	20	21	22			23	24
ALL_LVDT_OK_Bi	0	0	0	0	0	0	0	0
ALL_RP_HOME_Bi	0	0	0	0	0	0	0	0
DEVICE_ALLOWED	1	1	1	1	0	0	0	0
STABLE_BEAM	1	1	0	0	1	1	0	0
OVERRIDE1	1	0	1	0	1	0	1	0
USER_PERMIT1(Bi)	0	0	0	0	N/A	N/A	0	0
EXTRACT	1	1	1	1	N/A	N/A	1	1

Exceptions:

configurations with orange result fields = unreachable

		1		1	(STABLE_BEAMS without DEVICE_ALLOWED)			,
		1	· ['	· [· · · · · · · · · · · · · · · · · ·	· · · · · · · · · · · · · · · · · · ·	,	19.03.	
	2	STABLE_BEAMS		all pots at home motor reset	open limits: inner warning = 34 mm, inner dump = 33 mm	USER_PERMIT = 1	17:06 17:08	17:43 17:45
	2 to 8	1	1 '	move pot to 35 mm	1	USER_PERMIT = 1	17:10	17:45
f	8 to 10	to UNSTABLE_BEAMS	1 '	((USER_PERMIT = 1	17:11	17:47
:	10 to 4	1	1 '	automatic extraction	1	USER_PERMIT = 1	17:11	17:48
	4 to 2	to STABLE_BEAMS	1	motor reset		USER_PERMIT = 1	17:14 17:15	17:50 17:51
	2 to 8	1	1 '	move pot to 35 mm	1	USER_PERMIT = 1	17:15	17:51
1	8 to 20	1	1 '	(illegal limits: inner warning = 37 mm, inner dump = 36 mm	USER_PERMIT = 0	17:17	17:52

Impossible modes

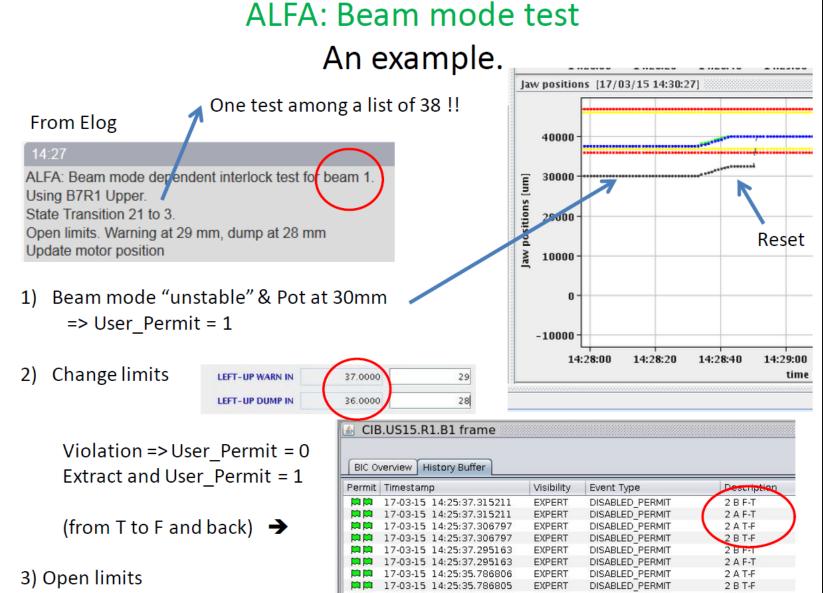
MD, PF –



Examples

(more in the e-log; links in EDMS docs)

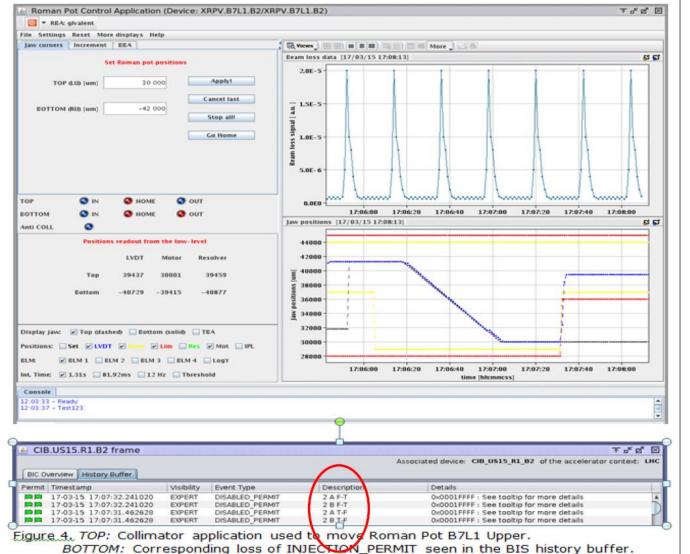






Examples











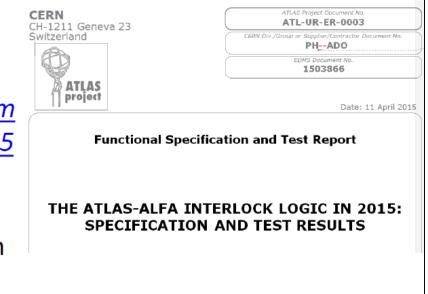
ALFA - summary

- Full set of tests done in two days (16th and 17th March). Total time order of 5-6 hours, when all fine.
- All tests successful but:
 - Since we had a very small change on DCS side (Enabling/Disabling & fast extraction) which is not yet tested
 - PXI crashed

EDMS note is done at 95% (see above).

https://edms.cern.ch/edmsui/#!m aster/navigator/document?D:195 8749382:1958749382:subDocs

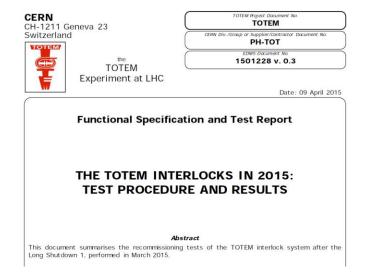
EDMS note will go for circulation right after





TOTEM Summary

- Beam-mode dependent tests successful at the second attempt (problem with transmission of the DEVICE_ALLOWED signal on the TOTEM side at the first attempt)
- Final validation done after all bug fixes in FPGA logics
- Still some PXI crashes; no impact on the interlock logic
- RP extraction via DCS not yet functional (communication problem between DCS and PXI), but emergency extraction via hardware button in TOTEM CR tested.
- EDMS test report waiting for comments https://edms.cern.ch/document/1501228
- Spare interlock box:
 - being programmed
 - test to be performed in the lab with simulated input flags







The End



BEFORE LS1



ALFA POSITION CONTROL SYSTEM PXI CRATE

Before LS1 one single FPGA card for controlling stepper motors, LVDT and Resolver position readout, microswitches and signals and interlocks position processing









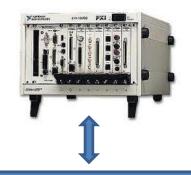
Interlocks and LHC signals Drives

Motor, Resolver and switches

LVDT's

Motor Drives

AFTER LS1



ALFA POSITION CONTROL SYSTEM PXI CRATE. ACCORDING COLLIMATORS ARCHITECURE



one FPGA card for controlling stepper motors, resolver position readout, microswitches, motor drives and LHC signals exchange



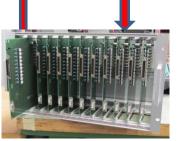
second FPGA card for safety position readout by means of the LVDT's and safety position interlock and LVDT_FAULT signal generation







LHC signal exchange



Signal Position interlock Interface crate



LVDT safety position readout

Motor, Resolver and switches

Motor Drives

LVDT Position Fault Interlock To detector Interlock Box

S.Ravat X. Pons PH-DT 2014