



Contribution ID: 136

Type: Oral presentation

Upgrade of the TOTEM data acquisition system for the LHC's Run Two

Tuesday, June 7, 2016 11:00 AM (20 minutes)

The TOTEM (TOTal cross section, Elastic scattering and diffraction dissociation Measurement at the LHC) experiment at LHC, has been designed to measure the total proton-proton cross-section with a luminosity independent method, based on the optical theorem, and to study the elastic and diffractive scattering at the LHC energy. To cope with the increased intensity of the LHC run 2 phase, and the increase on statistics required by the extension of the TOTEM physics program, approved for the 2016 run campaign, the previous VME based DAQ has been substituted by a new one based on the Scalable Readout System (SRS). The system is composed of 16 SRS-FECs, and one SRS-SRU; it features a throughput of $\sim 120\text{MB/s}$, saturating the SRS-FEC 1Gb/s link, for an overall 2GB/s data transfer rate into the online PC farm. This guarantee a baseline maximum trigger rate of $\sim 24\text{kHz}$, to be compared with the 1kHz of the previous VME based system. This trigger rate will be further improved, up to 100kHz trigger rate, implementing second level trigger algorithm in the SRS-SRU. The new system design fulfills the requirements for an increased efficiency, providing higher bandwidth, and increasing the purity of the data recorded supporting both a zero suppression algorithm and a second-level trigger based on pattern recognition algorithms implemented in hardware. Moreover a full compatibility with the legacy front-end hardware has been guaranteed, as well as the interface with the CMS experiment DAQ and the LHC Timing Trigger and Control (TTC) system. A complete re-design of the firmware, leveraging the usage of industrial strength firmware technologies, has been undertaken to provide a set of common interfaces and services between the standard system modules to the specific one of the user's application. This to allow an efficient development and easier insertion of different zero suppression and second-level trigger algorithms and a share of firmware blocks between different SRS components. Furthermore, to avoid packet losses and improve reliability of the UDP data transmission, a solution has been adopted that uses the Ethernet Flow control and New API (NAPI) mode driver, featuring a ticketing algorithms at the application layer. In this contribution we will describe in details the full system and performances during the commissioning phase at the LHC Interaction Point 5 (IP5).

Primary author: QUINTO, Michele (Universita e INFN-Bari (IT))

Co-authors: FIERGOLSKI, Adrian (CERN); RADICIONI, Emilio (Universita e INFN, Bari (IT)); CAFAGNA, Francesco (Universita e INFN, Bari (IT))

Presenter: QUINTO, Michele (Universita e INFN-Bari (IT))

Session Classification: Upgrades 3

Track Classification: Upgrades