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A Modular Data Acquisition System using the 10 GSa/s PSEC4 Waveform Recording Chip

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A data acquisition system using the 10 Gigasample-per-second waveform-recording PSEC4 chip is described. The system architecture incorporates two levels of hardware, FPGA-embedded system control, and data processing. The front-end unit is a 30 channel circuit board that holds five PSEC4 ASICs, a clock jitter cleaner, and a control FPGA. The analog bandwidth of the front-end signal path is 1.5 GHz. Each channel has an on-chip threshold-level discriminator that is monitored in the FPGA, from which a flexible on-board trigger decision can be formed. To instrument larger channel counts, a 'back-end' 6U VME32 central card was designed. This central card incorporates a single large FPGA that manages up to 8 front-end cards using one or two network (CAT5) cables per board, which transmits the clock and communicates data packets over a custom serial protocol. Data can be read off the board via USB, Ethernet, or dual SFP links in addition to the VME interface. To scale to larger systems, the central card architecture allows this board to serve also as a 'crate master' board, which receives data from up to 8 central cards (with each managing 8 front-end cards), allowing a single VME crate to control up to 1920 channels of the PSEC4 chip.

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