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Design and test of a GBTx based board for the upgrade of the ALICE TOF readout electronics

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During CERN LHC Long Shutdown 2 foreseen in 2018-2019, the ALICE Time of Flight (TOF) readout electronics is going to be upgraded in order to be able to cope with the target trigger rate of 200 KHz with proton-proton collisions and 50 KHz with lead-lead collisions. For this reason, the Digital Readout Module (DRM) board is currently being redesigned with improved features and more up to date technologies. As a first step towards the new DRM board, an intermediate test board with all the newer features has been designed, realized and tested. This communication will focus on the design of the test board and the test results obtained.
Since the board is going to work in a moderately hostile environment (0.13 krads expected in 10 years of data taking), a Microsemi Igloo2 FPGA has been chosen as the heart of the board. Being Flash memory based, it is basically immune to Single Event Upsets (SEUs) for what concerns the Configuration Memory. For what concerns the logic and memory, a triple modular redundancy scheme will be implemented in order to reduce the SEU rate. The GBTx radiation hard ASIC and a Versatile Link module VTRx (a rad-hard optical transceiver) from CERN will be used to implement both the interfaces towards the Data Acquisition (DAQ) and towards the trigger system. The GBTx implements a bidirectional 4.8 Gbps link between the detector area where the DRM sits and the counting room used for sending detector data in the uplink direction and for getting triggers and trigger information in the downlink direction.
For configuring the GBTx registers and the front-end cards, the test board also hosts an ARM processor based piggy-back card, which provides a TCP-IP connection to an external computer. In order to fit the existing slow control environment currently in place with the DRM ALICE TOF cards, a CAEN proprietary CONET2 optical link protocol was implemented with a SFP+ transceiver connected to the Igloo2 internal SERDES. The configuration of the GBTx registers can also be done via a National Instruments USB controller driving the GBTx I2C port via a dedicated Virtual Instrument.
The quality of the GBTx link has been tested in three ways: with an optical loopback, by connecting two different test boards together and also by means of a Xilinx KC705 evaluation board with a Kintex FPGA featuring a GBTx core provided by CERN. The Xilinx board was used to send triggers to the test board, which then sends back predefined data patterns stored into the static RAM. These configurations have been used to evaluate the BER of the GBTx optical connection both in the uplink and in the downlink directions: a BER as low as 10e(-14) has been measured with a 80 meters long multi-mode optical fiber.
The capability to pair a Microsemi FPGA with the GBTx ASIC was extensively tested.

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