

A Digital On-line Implementation of a Pulse-Shape Analysis Algorithm for Neutron-gamma Discrimination in the NEDA Detector

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Abstract—The detection of rare events close to the proton drip-line involve the utilization of high-efficient neutron detectors with excellent neutron-gamma discrimination (NGD) performance. Even though in the literature, several off-line algorithms focus on the maximization of the NGD accuracy, our aim is to look for an on-line efficient implementation capable to discard a majority of the gamma-rays, therefore allowing the system to work to counting rates up to 50 kHz, optimizing hence the overall electronics infrastructure in terms of data throughput. In this paper we analyze two of the most widespread techniques for NGD based on PSA, i.e. the charge-comparison method (CC) and the zero crossover (ZCO). Then, based on the NGD performance and FPGA resource utilization, we select one to be implemented in an FPGA. Finally we present the preliminary results obtained up to now.

I. INTRODUCTION

MODERN experiments in the field of experimental nuclear physics involve an increasingly ion-beam intensity to be capable to collect enough rare events in order to perform

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gamma-ray spectroscopy with enough statistics. Some of the nuclei of interest are near the proton drip-line where the reaction taking place emits one of several simultaneous neutrons, reason for which an efficient ancillary neutron detector must be coupled to a high-resolution gamma-ray spectrometer, such as GALILEO, [1,2] AGATA [3] and EXOGAM [4] obtaining hence information regarding the reaction channel taking place. The framework of the discussed algorithm will be based for the NEDA [5, 6] (Neutron Detector Array) detector, a new-generation neutron detector array that will be coupled with aforementioned spectrometers.

The NEDA detector has been designed in order to maximize the neutron collection efficiency and neutron-gamma discrimination by means of large volume BC-501A liquid-scintillator detectors and the usage of digital electronics [7]. The maximization of the NGD [8] performance is achieved both by employing pulse-shape analysis techniques as well as the selection of the PMT that provides the best time resolution [9]. The final setup will be composed of an array of 355 hexagonal detectors filled with BC-501A liquid scintillator, coupled to fast PMTs adjusted to work approximately at 1 V/MeVee. Then, the output signal from the PMTs is driven using 15-m long coaxial cables to an intermediate single-ended-to-differential card, which adapts the coaxial connectors to HDMI while preserving the gain settings before sending them to the digitizer. The rest of the electronics are implemented digitally by means of continuous-sampling FADCs [10,11] at 200 Msps with 11.7 ENOB and the usage of FPGAs digital-signal processing and readout by means of the NUMEXO2 digitizer.

The NUMEXO2 [12] card includes a motherboard with two large FPGAs (a V6 and a V5) and four FADC Mezzanines that perform the A/D conversion for 16 channels. Our framework for the NGD algorithm is set on the V6 in the DSP part, in charge to perform the data collection from the FADCs, DSP and data readout.

II. NEUTRON-GAMMA DISCRIMINATION ALGORITHMS

Two main algorithms have been analyzed, the Charge-Comparison (CC) and the Zero-Cross Over (ZCO), analyzing both the discrimination performance, the amount of resources that would be used in the FPGA as well as the implications to

implement them on-line. The NGD performance of the algorithms is further explained in [13]

On the one hand, the CC algorithm bases its principle after comparing two regions under the pulse, named as fast component and slow component. The discrimination clue can be appreciated from the Fig. 1 since for pulses with the same amplitude, the decay components of the gamma-rays decay at a much faster rate than neutrons. By taking the appropriate integration windows, the discrimination parameter can be obtained as a ration between the slow and fast integrals.

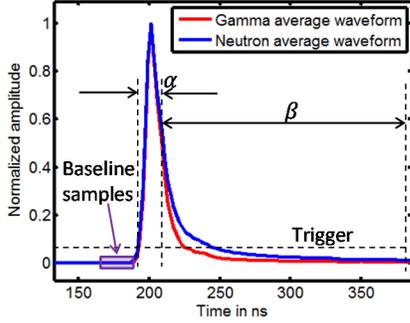


Fig.1: Comparison between amplitude-normalized neutron and gamma-rays signals. Besides, the

On the other hand, the ZCO technique bases its discrimination parameter on the time measurement between an amplitude threshold detector and bipolar-shaped version of the pulse undergoes a sign change as seen in Fig. 2.

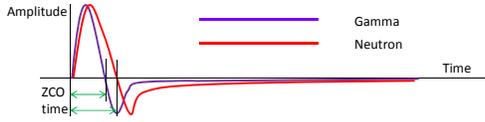


Fig.2: Schematic view of gamma-ray and neutron waveforms after bipolar shaping ready for ZCO time measurement.

By comparing both algorithms, it is true than in terms of NGD performance, both of them perform similarly according to [13]. However, the measurements were performed recorded off-line data where the time gates could be adjusted at sub-clock resolution. Sub-clock resolution techniques in the case of the ZCO would imply to use TDCs while in the case of the CC it would increase dramatically the amount of resources, improving only marginally the algorithm performance. However, in case of the ZCO, a good discrimination is obtained only by adjusting the time within a resolution less than 5 ns fact for which the robustness obtained in CC is larger.

III. IMPLEMENTATION OF THE CC ALGORITHM IN FPGA

After having selected the charge-comparison algorithm, the next step consists of its implementation using the device XC6VLX130T from Xilinx. For optimal operation, the block diagram has been designed according to Fig. 3.

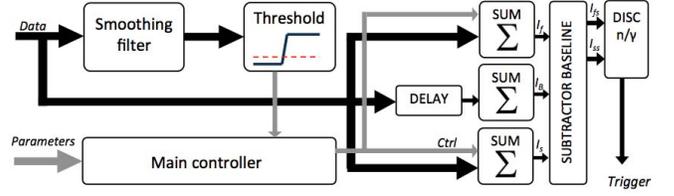


Fig.3: Block diagram used for the FPGA implementation of the CC algorithm

The samples arrive at 200 Msps in interlaced mode using a local clock at 100 Msps. The first part the signal passes by is an smoothing filter that can be either selected or disabled and a threshold detector which starts the computatios. Based on the pre-selected time-gates α (fast part) and β (slow part), the main controller is used to correctly time the integrators and wait until all numbers are ready where I_F refers to the fast integral, I_S does it for the slow integral and I_B takes into account the B samples before the threshold shoots.

$$I_F = \sum_{n=0}^{\alpha} v(n) \quad (1)$$

$$I_S = \sum_{n=\alpha+1}^{\alpha+\beta} v(n) \quad (2)$$

$$I_B = \sum_{n=-B}^0 v(n) \quad (3)$$

A second unit takes the calculated integrals and subtracts the term corresponding to the baseline, obtaining hence the terms I_{FS} and I_{SS} .

$$I_{FS} = I_F - \frac{\alpha}{B} I_B \quad (4)$$

$$I_{SS} = I_S - \frac{\beta}{B} I_B \quad (5)$$

For the ease of implementation, avoiding to use dividers, the numbers across wich the baseline is integrated is always a power of 2. The products αI_B and βI_B are computed using one of the DSP48E1 blocks in the FPGA. Finally, a comparison operation between both corrected integrals is carried out before delivering the n/γ signal to the trigger system. Instead of using a division to perform the ratio between I_{FS} and I_{SS} , one of the terms is multiplied by an integer factor δ (commonly I_{FS}) while the term is shifted left by a power of two avoiding hence the use of decimals. Regarding the data width, the input raw data is 14 bits. After the integration, a total amount of 22 bits is foreseen with a maximal integration time of 1.28 μ s (256 samples at 200 Msps). Then, taking into account the multiplication by the factor δ factor, at least the length in bits of this parameters must be added to the total length. In total 30 bits are used for the calculation of I_{FS} and I_{SS} .

The time invested in calculating the algorithm integrals is of paramount importance for the trigger system and it depends on the parameters α and β . Since the integrators are placed in

parallel and the baseline calculation is performed in parallel with the other two, the maximal time spent during the integrations if $\alpha + \beta > B$

$$T_{LAT} = \left\lceil \frac{\alpha}{2} \right\rceil + \left\lceil \frac{\beta}{2} \right\rceil + 11 \quad (6)$$

, quite a realistic assumption for our case. Finally, the total time invested in the subtraction and comparison unit is of 11 cycles with the depicted architecture, using a pipeline multiplier which takes 3 clock cycles.

IV. PRELIMINARY RESULTS

A first preliminary test has been carried out using the arbitrary waveform generator 33522A from Agilent, using pre-recorded samples obtained from a XC4512 PMT. Both the samples obtained for gamma-rays and neutrons have been normalized and averaged. The waveforms were adapted to be used by the waveform generator, where only periodic-mode behavior has been tested up to now.

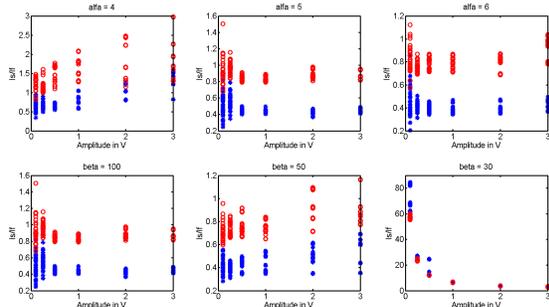


Fig.4: Plot showing the values for I_{SS}/I_{FS} for several values of amplitude, α , and β . Red dots depict neutron events while blue refer to gamma-rays.

Each waveform applied contains 500 samples that has been applied using several windows of and amplitudes. Fig. 4 shows some of these results for α and β , noticing a clear discrimination between the gamma-rays (blue) and neutrons (red) at higher amplitudes which degrades as soon as the input amplitude decreases. In fact this test was mainly aimed to verify the algorithm consistency by applying known pulses before starting to use real ^{252}Cf sources. The tests involving

the radioactive source in order to perform the final tests of the algorithm will be carried out during the incoming months.

CONCLUSIONS

An FPGA implementation of the Charge Comparison algorithm has been carried out, taking into account issues related with NGD performance, robustness, portability to the digital domain and FPGA and resource usage. The algorithm was successfully tested using periodic waveforms up to the desired counting rate, although still some of the pile-up validation/rejection methods should be refined. Further tests using a ^{252}Cf source will be performed along this year in order to prove the confirmation in an experimental environment.

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